50 A, VRPower® Integrated Power Stage

DESCRIPTION

The SiC781 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency and high power density performance. Packaged in Vishay's proprietary MLP 6 mm x 6 mm package, SiC781 enables voltage regulator designs to deliver currents up to 50 A per phase.

The internal power MOSFETs utilize Vishay's state-of-the-art trench MOSFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC781 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and a thermal warning (THWn) that alerts the system of excessive junction temperature. This driver is compatible with wide range of PWM controllers and supports tri-state PWM logic (5 V) as well as zero current detection to improve light load efficiency.

FEATURES

- Thermally enhanced PowerPAK® MLP66-40L package
- Industry benchmark MOSFET with integrated Schottky diode
- Delivers up to 50 A continuous current
- Pin and functionally compatible with NCP5369N
- High frequency operation up to 1 MHz
- Optimized for 12 V input rail applications
- 5 V PWM logic with tri-state threshold
- Zero current detection and low side MOSFET turn off during discontinuous mode
- Short PWM propagation delay (< 20 ns)
- Supports Intel PS2 requirement with ON Semiconductor's NCP5133 and NCP6133 controllers
- Thermal monitor flag
- Faster enable / disable
- V_{CIN} under voltage lock out (UVLO)

APPLICATIONS

- Synchronous buck converters
- Multi-phase VRDs for CPU, GPU and memory
- DC/DC POL modules

TYPICAL APPLICATION DIAGRAM

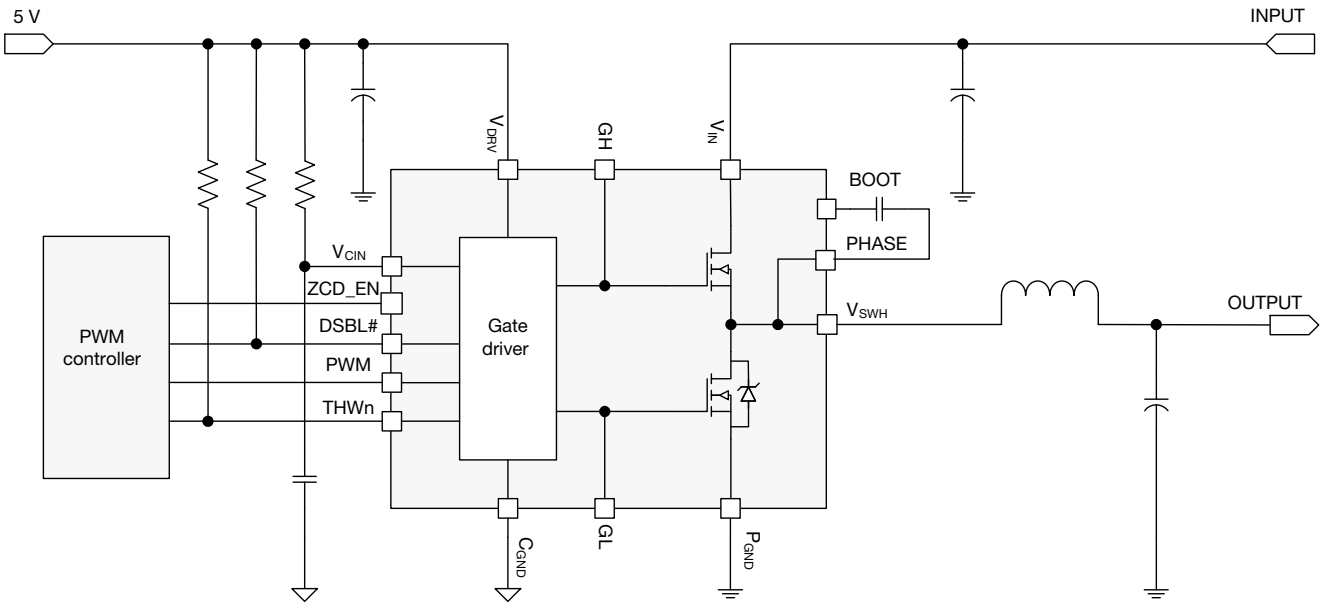


Fig. 1 - SiC781 Typical Application Diagram

PINOUT CONFIGURATION

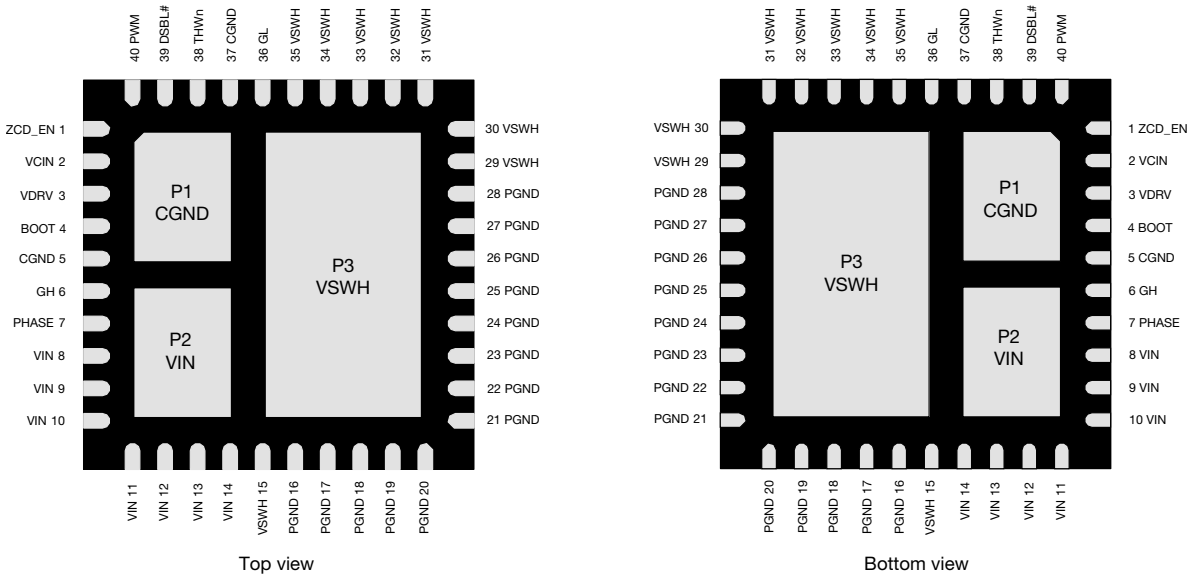


Fig. 2 - SiC781 Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	**NAME**	**FUNCTION**
1	ZCD_EN	ZCD control. Active high
2	V_{CIN}	Supply voltage for internal logic circuitry
3	V_{DRV}	Supply voltage for internal gate driver
4	BOOT	High-side driver bootstrap voltage
5, 37, P1	C_{GND}	Analog ground for the driver IC
6	GH	High-side gate signal
7	PHASE	Return path of high-side gate driver
8 to 14, P2	V_{IN}	Power stage input voltage. Drain of high-side MOSFET
15, 29 to 35, P3	V_{SWH}	Switch node of the power stage
16 to 28	P_{GND}	Power ground
36	GL	Low-side gate signal
38	THWn	Thermal warning open drain output
39	DSBL#	Disable pin. Active low
40	PWM	PWM control input

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING CODE**
SiC781CD-T1-GE3	PowerPAK MLP66-40L	SiC781
SiC781DB	Reference Board	

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**SYMBOL**	**LIMITS**	**UNIT**
Input Voltage	V_{IN}	-0.3 to +20	V
Control Logic Supply Voltage	V_{CIN}	-0.3 to +7	
Drive Supply Voltage	V_{DRV}	-0.3 to +7	
Switch Node (DC voltage)	V_{SWH}	-0.3 to +20	
Switch Node (AC voltage) (1)		-7 to +27	
BOOT Voltage (DC voltage)	V_{BOOT}	27	
BOOT Voltage (AC voltage) (2)		34	
BOOT to PHASE (DC voltage)	V_{BOOT_PHASE}	-0.3 to +7	
BOOT to PHASE (AC voltage) (3)		-0.3 to +8	
All Logic Inputs and Outputs (PWM, DSBL#, ZCD_EN and THWn)		-0.3 to V_{CIN} + 0.3	
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_A	-40 to +125	
Storage Temperature	T_{stg}	-65 to +150	
Electrostatic Discharge Protection	Human body model, JESD22-A114	4000	V
	Charged device model, JESD22-C101	1000	

Notes

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) The specification values indicate “AC voltage” is V_{SWH} to P_{GND}, -7 V (< 50 ns, 10 µJ), minimum and 27 V (< 50 ns), maximum.

(2) The specification value indicates “AC voltage” is V_{BOOT} to P_{GND}, 34 V (< 50 ns) maximum.

(3) The specification value indicates “AC voltage” is V_{BOOT} to V_{PHASE}, 8 V (< 20 ns) maximum.

RECOMMENDED OPERATING RANGE				
ELECTRICAL	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input Voltage (V_{IN})	4.5	-	16	V
Drive Supply Voltage (V_{DRV})	4.5	5	5.5	
Control Logic Supply Voltage (V_{CIN})	4.5	5	5.5	
Switch Node (V_{SWH}, DC voltage)	-	-	20	
BOOT to PHASE (V_{BOOT_PHASE}, DC voltage)	4	4.5	5.5	
Thermal Resistance				
Thermal Resistance from Junction to Case	-	2.5	-	°C/W
Thermal Resistance from Junction to PAD	-	1	-	

ELECTRICAL SPECIFICATIONS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** (DSBL# = ZCD_EN = 5 V, V_{IN} = 12 V, V_{DRV} = V_{CIN} = 5 V, T_A = 25 °C)	**MIN.**	**TYP. (1)**	**MAX.**	**UNIT**
POWER SUPPLIES						
Control Logic Supply Current	I_{VCIN}	$V_{DSBL\#}$ = 0 V, no switching	-	85	-	µA
		$V_{DSBL\#}$ = 5 V, no switching	-	275	-	
		$V_{DSBL\#}$ = 5 V, f_s = 300 kHz, D = 0.1	-	300	-	
Drive Supply Current	I_{VDRV}	f_s = 300 kHz, D = 0.1	-	15	24	mA
		f_s = 1 MHz, D = 0.1	-	45	-	
		$V_{DSBL\#}$ = 0 V, no switching	-	35	-	µA
		$V_{DSBL\#}$ = 5 V, no switching	-	45	-	
BOOTSTRAP SUPPLY						
Bootstrap Switch Forward Voltage	V_F	I_F = 2 mA	-	-	0.4	V
PWM CONTROL INPUT						
Rising Threshold	$V_{TH\_PWM\_R}$		3.4	3.7	4.2	V
Falling Threshold	$V_{TH\_PWM\_F}$		0.7	0.9	1.2	
Tri-state Rising Threshold	$V_{TH\_TRI\_R}$		0.9	1.2	1.5	
Tri-state Falling Threshold	$V_{TH\_TRI\_F}$		3	3.4	3.7	
Tri-state Rising Threshold Hysteresis	$V_{HYS\_TRI\_R}$		-	250	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS\_TRI\_F}$		-	350	-	
DRIVER TIMING						
Tri-state to GH/GL Rising Propagation Delay	$t_{PD\_TRI\_R}$		-	30	-	ns
Tri-state GH Hold-Off Time	t_{TSHO_GH}	PWM high to tri-state	-	35	-	
Tri-state GL Hold-Off Time	t_{TSHO_GL}	PWM low to tri-state	-	120	-	
GH - Turn Off Propagation Delay	$t_{PD\_OFF\_GH}$		-	20	-	
GH - Turn On Propagation Delay (Dead time rising)	$t_{PD\_ON\_GH}$		-	8	-	
GL - Turn Off Propagation Delay	$t_{PD\_OFF\_GL}$		-	12	-	
GL - Turn On Propagation Delay (Dead time falling)	$t_{PD\_ON\_GL}$		-	8	-	
DSBL# High to GH/GL Rising Propagation Delay	$t_{PD\_DSBL\#\_R}$	Fig. 5	-	20	-	
DSBL# Low to GH/GL Falling Propagation Delay	$t_{PD\_DSBL\#\_F}$		-	15	-	
DSBL#, ZCD_EN INPUT						
DSBL# Logic Input Voltage	$V_{IH\_DSBL\#}$	Input logic high	2	-	-	V
	$V_{IL\_DSBL\#}$	Input logic low	-	-	0.8	
ZCD_EN Logic Input Voltage	$V_{IH\_ZCD\_EN}$	Input logic high	2	-	-	
	$V_{IL\_ZCD\_EN}$	Input logic low	-	-	0.8	

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED (DSBL# = ZCD_EN = 5 V, V_{IN} = 12 V, V_{DRV} = V_{CIN} = 5 V, T_A = 25 °C)	MIN.	TYP. (1)	MAX.	UNIT
PROTECTION						
Under Voltage Lockout	V_{UVLO}	V_{CIN} rising, on threshold	-	3.7	4.3	V
		V_{CIN} falling, off threshold	2.7	3.2	-	
Under Voltage Lockout Hysteresis	V_{UVLO_HYST}		-	500	-	mV
THWn Flag Set (2)	T_{THWn_SET}		-	160	-	°C
THWn Flag Clear (2)	T_{THWn_CLEAR}		-	135	-	
THWn Flag Hysteresis (2)	T_{THWn_HYST}		-	25	-	
THWn Output Low	V_{OL_THWn}	I_{THWn} = 2 mA	-	0.02	-	V

Notes

(1) Typical limits are established by characterization and are not production tested.

(2) Guaranteed by design.

DEVICE TRUTH TABLE

DSBL#	ZCD_EN	PWM	GH	GL
Open	X	X	L	L
L	X	X	L	L
H	L	H	H	L
H	L	Tri-state	L	L
H	L	L	L	L
H	H	H	H	L
H	H	H to tri-state (1)	L	H, I_L > 0 A L, I_L < 0 A
H	H	L	L	H
H	H	L to tri-state	L	L

Note

(1) In this condition (PS2 mode), controller will deliver PWM signal switching between 5 V and 2 V. See the timing diagram in fig. 3.

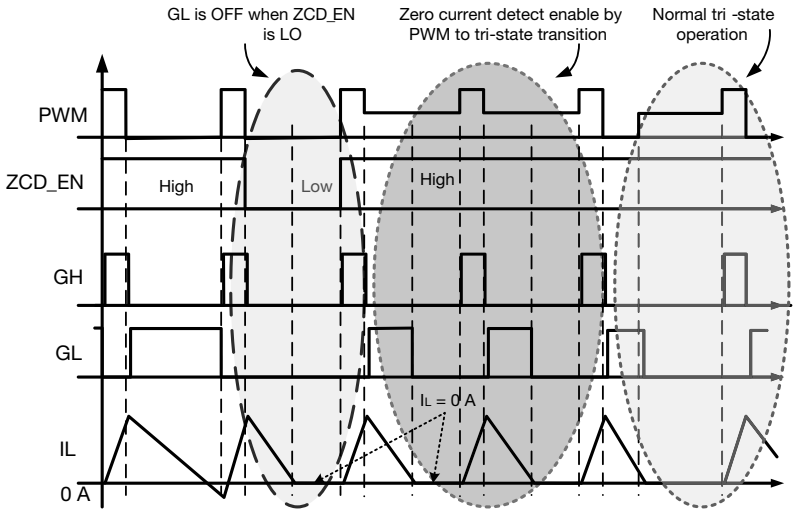


Fig. 3 - Timing Diagram

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. PWM input operates as follows for two state logic. When PWM is driven above $V_{TH\_PWM\_R}$ the low-side is turned off and the high-side is turned on. When PWM input is driven below $V_{TH\_PWM\_F}$ the high-side turns off and the low-side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, if the PWM input stays tri-state for the tri-state hold-off period, t_{TSHO}, both high-side and low-side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering.

The SiC781CD incorporates PWM voltage thresholds that are compatible with 5 V logic.

Disable (DSBL#)

In the low-state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFETs. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to C_{GND} and shut down the IC.

Diode Emulation Mode (ZCD_EN)

When ZCD_EN pin is high and PWM signal switches from High to tri-state, GL is forced on (after normal BBM time) for the duration of tri-state period. During this time, it is under control of the ZCD (zero crossing detect) comparator. If, after the internal blanking delay, the inductor current becomes zero, GL is turned off. This improves light load efficiency by avoiding discharge of output capacitors.

If PWM enters tri-state from Low, then device will go into normal tri-state mode after tri-state delay. If ZCD_EN pin is Low the GL output will be turned off regardless of Inductor current, this is an alternative method of improving light load efficiency by reducing switching losses.

This mode of operation is critical to meet improved efficiencies required in Intel's PS2 mode of operation for memory and processor applications.

Thermal Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 kΩ to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC781 does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter.

The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate driver noise into the IC.

Bootstrap Circuit (BOOT)

An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a bootstrap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC781 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned on at the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on from tuning on until the other's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC781 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

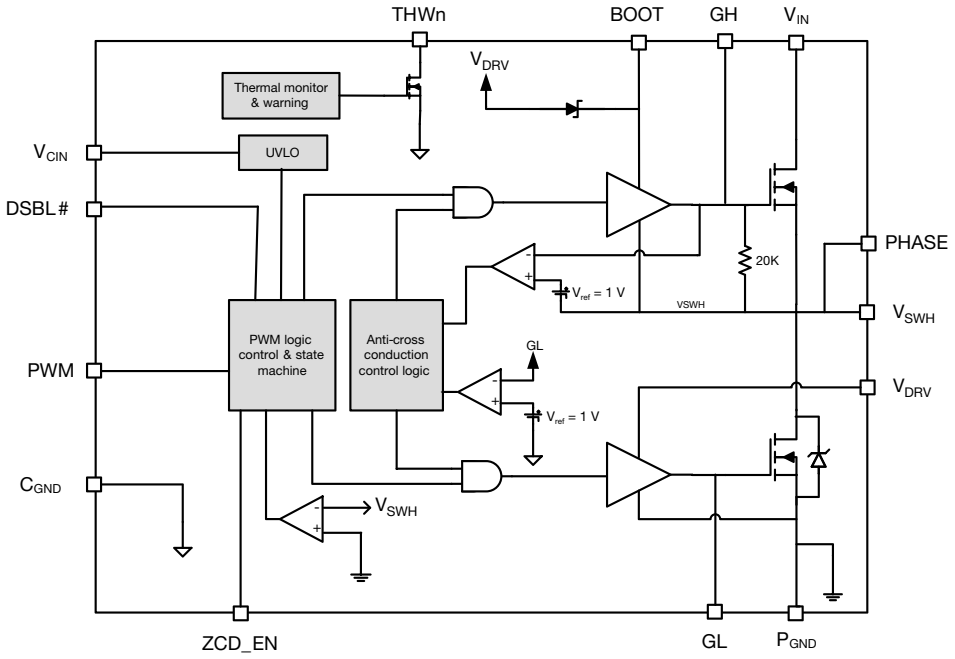


Fig. 4 - SiC781 Functional Block Diagram

OPERATION TIMING DIAGRAM: DSBL#

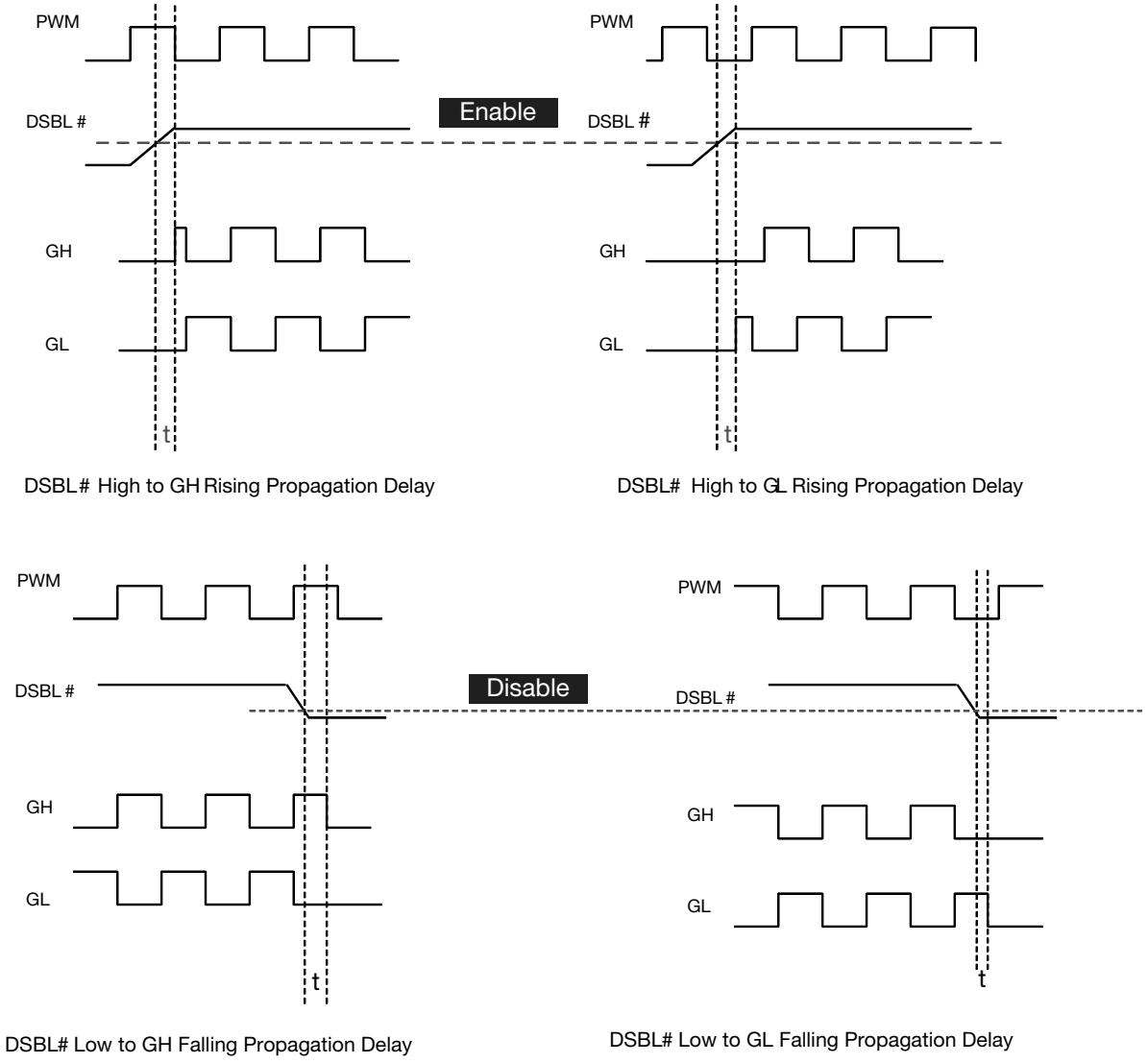


Fig. 5 - DSBL# Propagation Delay

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, F_{SW} = 500 kHz, V_{DRV} = V_{CIN} = 5 V, unless noted otherwise), $L_{O/P}$ = 0.33 µH / DCR 0.83 mΩ (IHLP5050FD0R33-01)

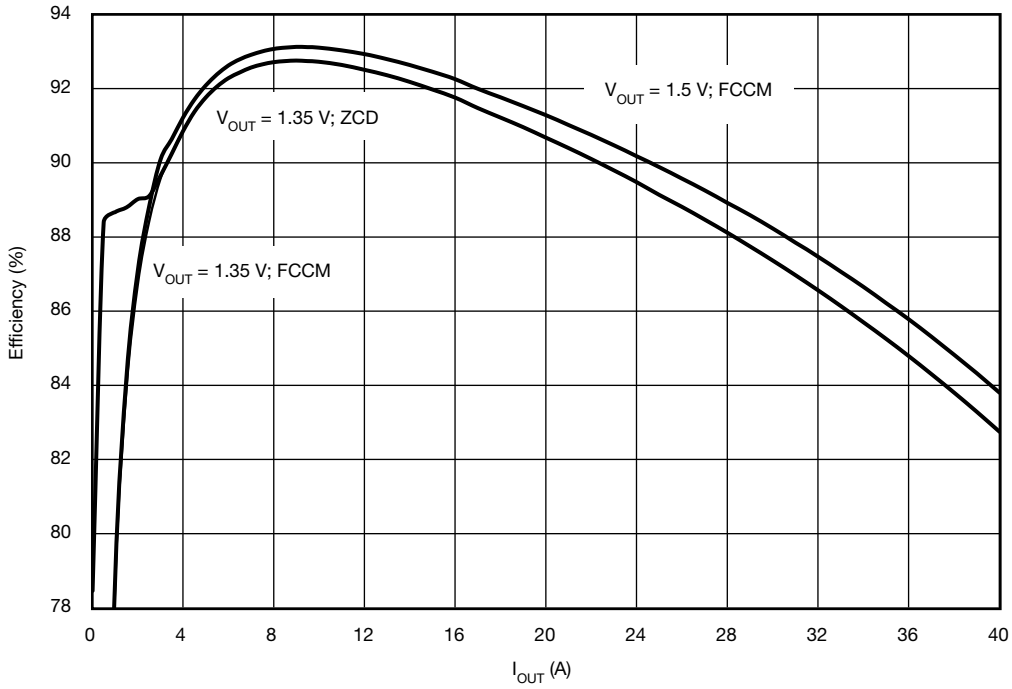


Fig. 6 - Efficiency vs. I_{OUT}
(Complete converter efficiency, P_{IN} = [V_{IN} x I_{IN} + 5 V x (I_{DRV} + I_{CIN})], P_{OUT} = V_{OUT} x I_{OUT} measured at output capacitor)

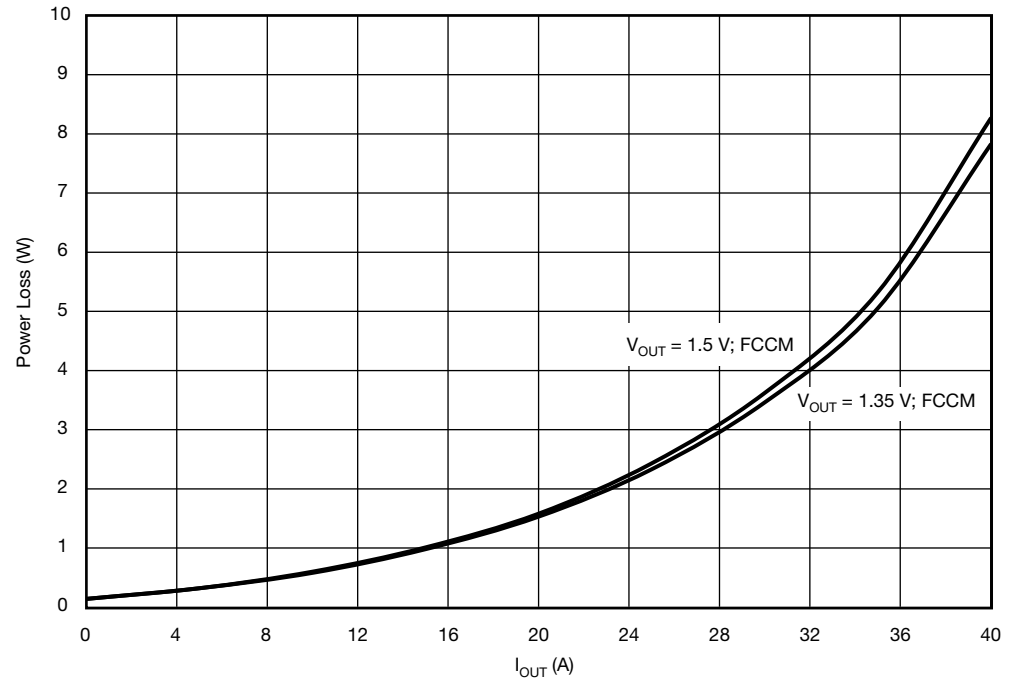


Fig. 7 - Power Losses vs. I_{OUT}
(Includes losses dissipated in the SiC781 only)

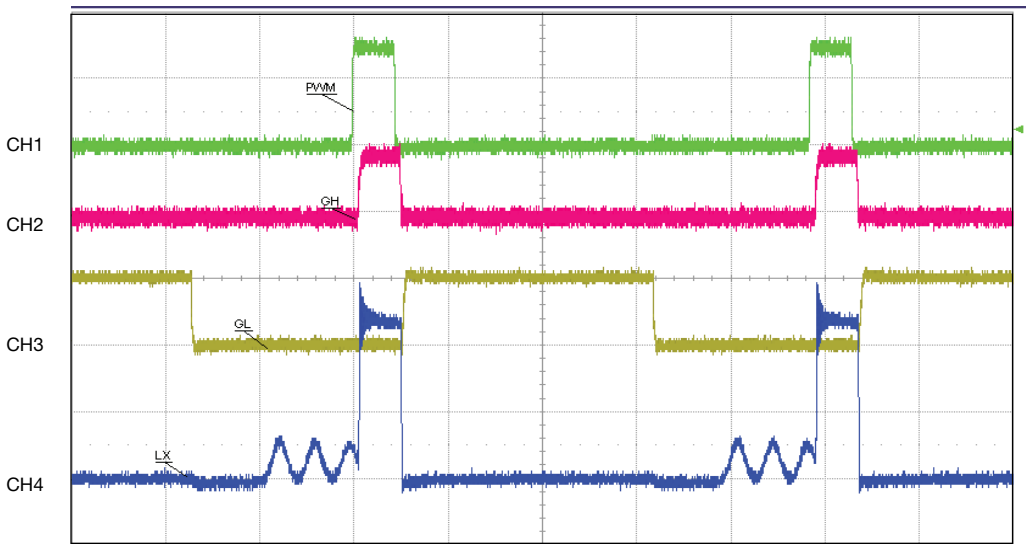
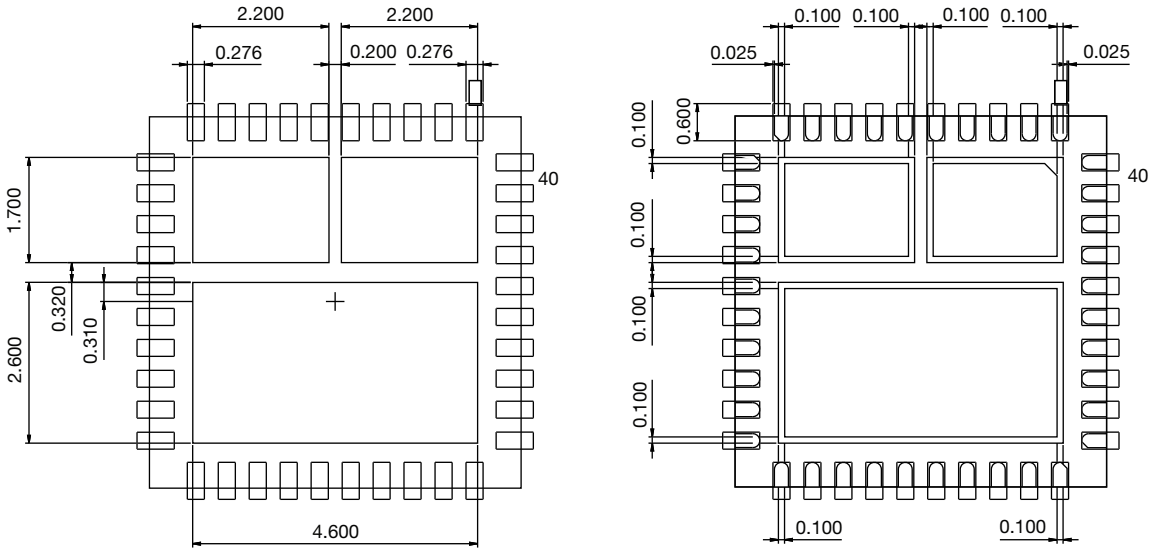


Fig. 8 - PS2 Mode Operation (ZCD)

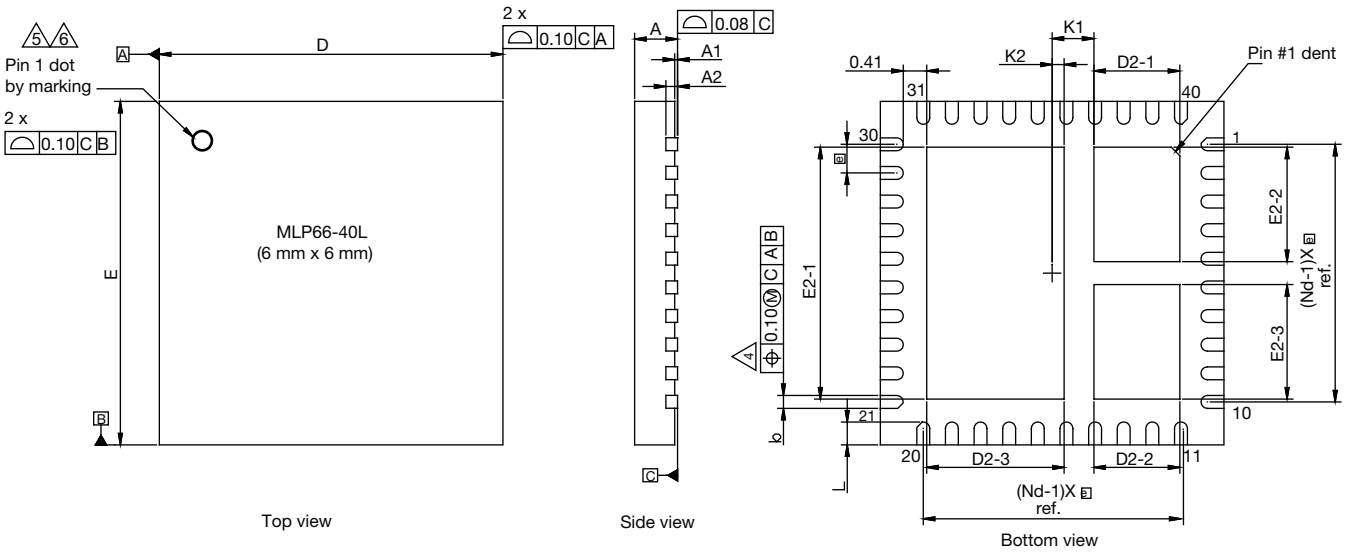
CH1 (green) = PWM (2V/div), CH2 (red) = GH (5V/div), CH3 (yellow) = GL (5V/div), CH4 (blue) = V_{SWH} (5V/div)

RECOMMENDED LAND PATTERN PowerPAK MLP66-40L



All Dimensions are in milimeters

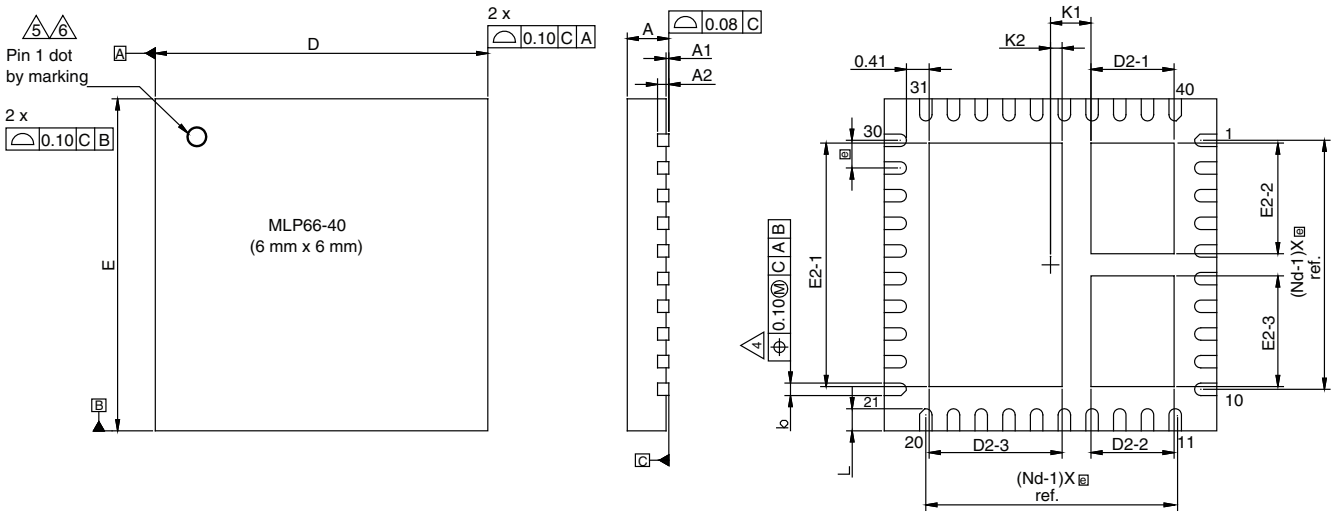
PACKAGE OUTLINE DRAWING



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b	0.20	0.25	0.30	0.078	0.098	0.011
D		6.00 BSC			0.236 BSC	
e		0.50 BSC			0.019 BSC	
E		6.00 BSC			0.236 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N		40			40	
Nd		10			10	
Ne		10			10	
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1		0.73 BSC			0.028 BSC	
K2		0.21 BSC			0.008 BSC	

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62950.

PowerPAK® MLP66-40 Case Outline



Top View

Side View

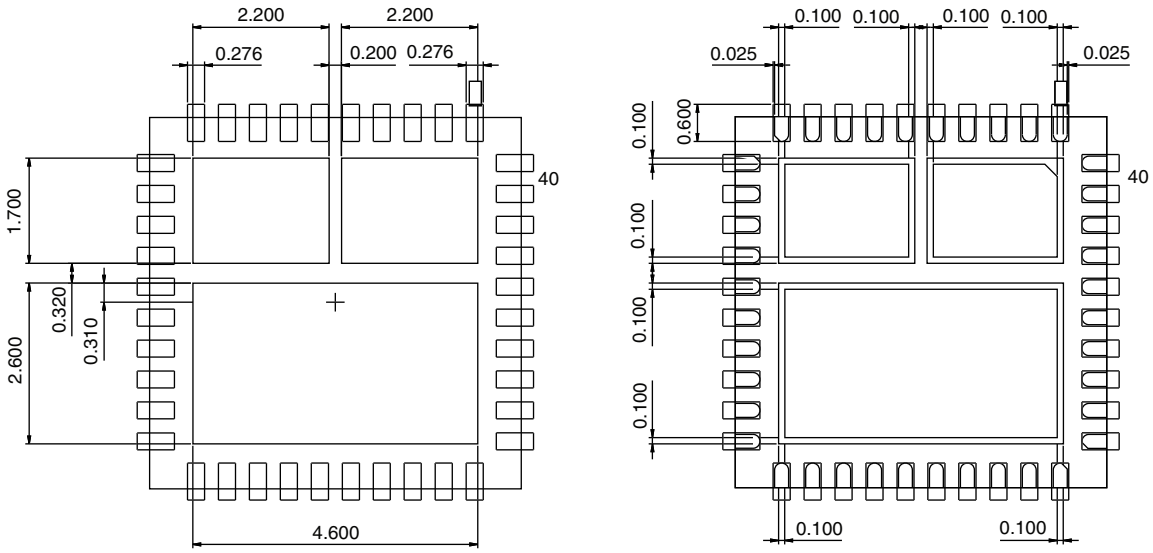
Bottom View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.078	0.098	0.011
D		6.00 BSC			0.236 BSC	
e		0.50 BSC			0.019 BSC	
E		6.00 BSC			0.236 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		40			40	
Nd (3)		10			10	
Ne (3)		10			10	
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1		0.73 BSC			0.028 BSC	
K2		0.21 BSC			0.008 BSC	
ECN: T14-0826-Rev. B, 12-Jan-15 DWG: 5986						

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

Recommended Land Pattern PowerPAK® MLP66-40L



All Dimensions are in milimeters

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