N-Channel Half-Bridge Driver

FEATURES

- Single Input for High-Side and Low-Side MOSFETs
- 20- to 40-V Supply
- Static (dc) Operation
- Cross-Conduction Protected
- Undervoltage Lockout
- ESD and Short Circuit Protected
- Fault Feedback

APPLICATIONS

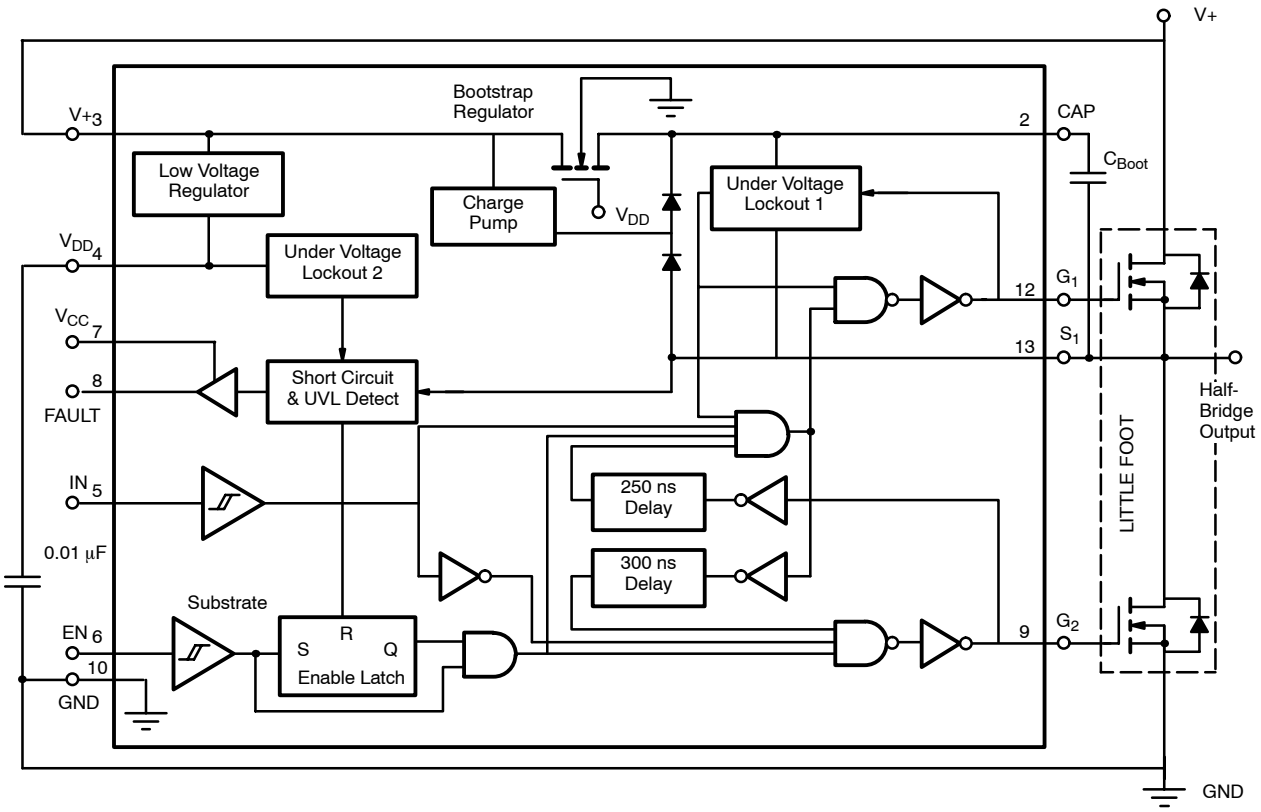
- Power Supplies
- Motor Drives
- Office Automation
- Computer Peripherals
- Industrial Controllers
- Robotics
- Medical Equipment

DESCRIPTION

The Si9976 is an integrated driver for an n-channel MOSFET half-bridge. Schmitt trigger inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply of 20 to 40 volts. Both half-bridge n-channel gates are driven directly with low-impedance outputs. Addition of one external capacitor allows an internal circuit to level shift both the power supply and logic signal for the half-bridge high-side n-channel gate drive. An internal charge pump replaces leakage current lost in the high-side driver circuit to provide “static” (dc) operation in any output condition. Protection features include an undervoltage lockout, cross-conduction prevention logic, and a short circuit monitor.

The Si9976 is available in both standard and lead (Pb)-free, 14-pin SOIC (surface mount) packages, specified to operate over the industrial (−40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on IN, EN (pins 5, 6)
with respect to ground ..... −0.3 to V_{DD} +0.3 V
Voltage on V_{CC} (pin 7) ..... −0.3 to +18 V
Voltage on V+, S1 (pins 3, 13) ..... −0.3 to +50 V
Voltage on CAP, G1[a] (pins 2, 12) ..... −0.3 to +60 V
Peak Output Current ..... 0.5 A
Operating Temperature (T_A) ..... −40 to 85°C
Storage Temperature ..... −50 to 150°C

Maximum Junction Temperature (T_J) ..... 125°C
Power Dissipation[b] ..... 1 W
Θ_{JA} ..... 100°C/W[b]

Notes
a. Internally generated voltage for reference only.
b. Derate 10 mW/°C above 25°C.
c. PC board mounted with no forced air flow.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V T_A = Operating Temperature Range	Limits D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Input						
Input Voltage High (EN and IN)	V_{INH}		4.0			V
Input Voltage Low (EN and IN)	V_{INL}				1.0	
Input Hysteresis Voltage	V_H			0.5		
Input Current—Input Voltage High	I_{INH}	(EN and IN) V_{IN} = 15 V			1	µA
Input Current—Input Voltage Low	I_{INL}	(EN and IN) V_{IN} = 0 V	−1			
Output						
Output Voltage High, G1[d]	V_{OUTH}	S1 = V+, I_{OUT} = −10 mA	10	12		V
Output Voltage High, G2[e]		S1 = GND, I_{OUT} = −10 mA	12	15		
Output Voltage Low, G1 and G2	V_{OUTL}	S1 = GND, I_{OUT} = 60 mA		1.2	3	
Fault Output Voltage High	V_{OH}	V_{CC} = 4.5 V, I_{OUT} = −0.2 mA	3.5	4		
Fault Output Voltage Low	V_{OL}	V_{CC} = 4.5 V, I_{OUT} = 0.6 mA		0.3	1.0	
Undervoltage Lockout 1	UVL1			11		
Undervoltage Lockout 2	UVL2			14		
Capacitor Voltage[g]	V_{CAP}	V+ = 40V		55		
Capacitor Current	I_{CAP}	S1 = GND, V_{CAP} = 0 V			−10	mA
		S1 = GND, V_{CAP} = 9 V			−2	
Supply						
V+ Supply Range			20		40	V
V+ Supply Current	I+ (H)	G2 High, No Load		1.7	3.5	mA
	I+ (L)	G2 Low, No Load, S1 = GND		2	4.5	
V_{CC} Supply Range			4.5		16.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 16.5 V			10	µA
V_{DD} Supply Voltage[f]	V_{DD}		15	16	17.5	V

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified V+ = 20 to 40 V T_A = Operating Temperature Range		Limits D Suffix –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Dynamic							
Propogation Delay Time Low to High Level	t_{PLH}	50% IN to V_{OUT} = 5 V, C_L = 600 pF	G1		350		ns
			G2		400		
Propogation Delay Time High to Low Level	t_{PHL}		G1		150		
			G2		50		
Propogation Delay Time, Low to High Level, Enable-to-Fault Output		50% IN to FAULT = 2 V, S1 shorted to GND or V+			500		
Output Rise Time (G1, G2)	t_r	1 to 10 V, C_L = 600 pf			110		
Output Fall Time (G1, G2)	t_f	10 to 1 V, C_L = 600 pf			50		
Short Circuit Pulse Width	t_{SC}	50% to 50% of V_{OUT}			350		

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
d. To supply the output current of 10 mA on a dc basis, an external 13-V supply must be connected between the CAP pin and the S1 pin with the negative terminal of the supply connected to S1. This is not needed in an actual application because output currents are supplied by the C_{BOOT} capacitor. Voltage specified with respect to V+.
e. For testing purposes, the 10-mA load current must be supplied by an external current source to the V_{DD} pin to avoid pulling down the V_{DD} supply.
f. Internally generated voltage for reference only.
g. $V_{CAP} = (V+) + (V_{DD})$

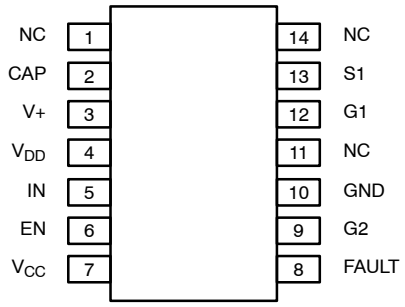
TRUTH TABLE

EN	IN	Condition	FAULT OUTPUT	G1 OUT	G2 OUT
1	0	Normal Operation	0	Low	High
1	1	Normal Operation	0	High	Low
0	X	Disabled	X[a]	Low	Low
1	0	Load Shorted to V+	1[b]	Low	Low
1	1	Load Shorted to Ground	1[b]	Low	Low
1	1	Undervoltage on C_{BOOT}	0	Low	Low
1	0	Undervoltage on C_{BOOT}	0	Low	High
X	X	Undervoltage on V_{DD}[c]	1	Low	Low

Notes
a. FAULT output retains previous state until ENABLE rising edge.
b. Latch FAULT condition, reset by ENABLE rising edge.
c. V_{DD} is an internally generated low-voltage supply.

PIN CONFIGURATION AND ORDERING INFORMATION

SOIC-14



Top View

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9976DY	–40 to 85°C	SOIC-14
Si9976DY-T1		
Si9976DY-T1—E3		

PIN DESCRIPTION

Pin 1

No connection.

Pin 2: CAP

Connection for the positive terminal of the bootstrap capacitor C_{BOOT}. A 0.01-µF C_{BOOT} capacitor can be used for most applications.

Pin 3: V+

This is the only external power supply required for the Si9976, and must be the same supply used to power the half-bridge it is driving. The Si9976 powers it's low-voltage logic, low-side gate driver, and bootstrap/charge pump circuits from self-contained voltage regulators which require only a bootstrap capacitor on the CAP pin and a bypass capacitor on the V_{DD} pin.

No voltage sensing circuitry monitors V+ directly; however, the low-voltage, internally generated V_{DD} supply and the bootstrap voltage (which are derived from V+) are directly protected by undervoltage monitors.

Pin 4: V_{DD}

Connection to the internally generated low-voltage supply which must be bypassed to ground with a 0.01-µF capacitor.

Pin 5: IN

Logic input. A low level input turns off the high-side half-bridge MOSFET and, after an internally set dead time, turns the low-side half-bridge MOSFET on. A high input level has the opposite effect. The input is compatible with 5-, 12- or 15-V logic outputs.

Pin 6: EN

Enable input. A low EN input level prevents turn on of either half-bridge MOSFET. If the Si9976 is internally disabled as a result of an output short-circuit condition, a low-to-high transition on EN is required to clear the fault and resume operation. The input logic levels are the same as IN.

Pin 7: V_{CC}

If the FAULT output is used, the V_{CC} pin must be connected to the logic supply voltage in order to set the high level of the FAULT output. If the FAULT output is not used, this pin may be left open with no effect on internal fault sensing or protection circuitry.

Pin 8: FAULT

The Fault output is latched high when a short-circuit output condition is detected. FAULT will return low when the circuit is reset using the EN pin. The FAULT output also indicates the status of the undervoltage sense circuit on V_{DD}, however the fault condition is cleared automatically when the undervoltage condition clears.

Pin 9: G2

This pin drives the gate of the external low-side power transistor.

Pin 10: GND

The ground return for V+, logic reference, and connection for source of external low-side power transistor.

Pin 11

No connection.

Pin 12: G1

This pin drives the gate of the external high side power transistor.

Pin 13: S1

Connection for the source of the external high-side power transistor, the drain of the external low-side power transistor, the negative terminal of the bootstrap capacitor, and the system load. The voltage on this pin is sensed by the circuitry that monitors the load for shorts.

Pin 14

No connection.

DETAILED DESCRIPTION

Power On Conditioning

Bootstrap-type floating supplies require that the bootstrap capacitor be charged at power on. In the case of the Si9976, this is accomplished by pulsing the IN line low with the EN line held high, thus turning on the low-side MOSFET and providing the charging path for the capacitor.

Operating Voltage: 20 to 40 V

The Si9976 is intended to be powered by a single power supply within the range of 20 to 40 V and is designed to drive a totem pole pair of NMOS power transistors such as those within the Si9955. The power transistors must be powered by the same power supply as this driver. In addition to the high-voltage power supply (20 to 40 V), the Si9976 must have a power supply connected to the V_{CC} terminal, if a fault output signal is desired. This power supply provides operating voltage for the fault output and allows the high output voltage level to be compatible with system logic that monitors the fault condition. The value of this power supply must be within the range of 4.5 to 16.5 V to ensure functionality of the output. Internal fault circuitry, which is used for shorted-load protection, is not affected by this power supply.

Cross-Conduction Protection

The high-side power transistor can only be turned on after a fixed time delay following the return to ground of the low-side power transistor's gate. The low-side transistor can only be turned on after a fixed time delay following the high-side transistor turn-off signal.

Undervoltage Lockout

During power up, both power transistors are held off until the internal regulated power supply, V_{DD}, is approximately one V_{be} from the final value, nominally 16 V. After power up, the undervoltage lockout circuitry continues to monitor V_{DD}. If an undervoltage condition occurs, both the high-side and low-side transistors will be turned off and the fault output will be set high. When the undervoltage condition no longer exists, normal function will resume automatically. Separate voltage sensing of the bootstrap capacitor voltage allows a turn-on signal to be sent to the high-side drive circuit if either the bootstrap capacitor has full voltage, or the load voltage is high (driven high by an inductive load or shorted high). The voltage sensing circuit will allow the high-side power transistor to turn on if an on signal is present and the voltage on the bootstrap capacitor rises from undervoltage to operating voltage.

Short Circuit Protection

This device is intended to be used only in a half-bridge which drives inductive loads. A shorted load is presumed if the load voltage does not make the intended transition within an allotted time. Separate timing is provided for the two transitions. A longer time is allowed for the high-side to turn on (300 ns vs. 200 ns) since the propagation delays are longer. Excessive capacitive loading can be interpreted as a short. The value of capacitance that is needed to produce the indication of a short depends on the load driving capability of the power transistors.

ESD Protection

Electrostatic discharge protection devices are between V_{DD} and GND, V_{CC} and GND, and from terminals IN, EN, G2, and FAULT to both V_{DD} and GND. V+, CAP, S1, and G1 are not ESD protected.

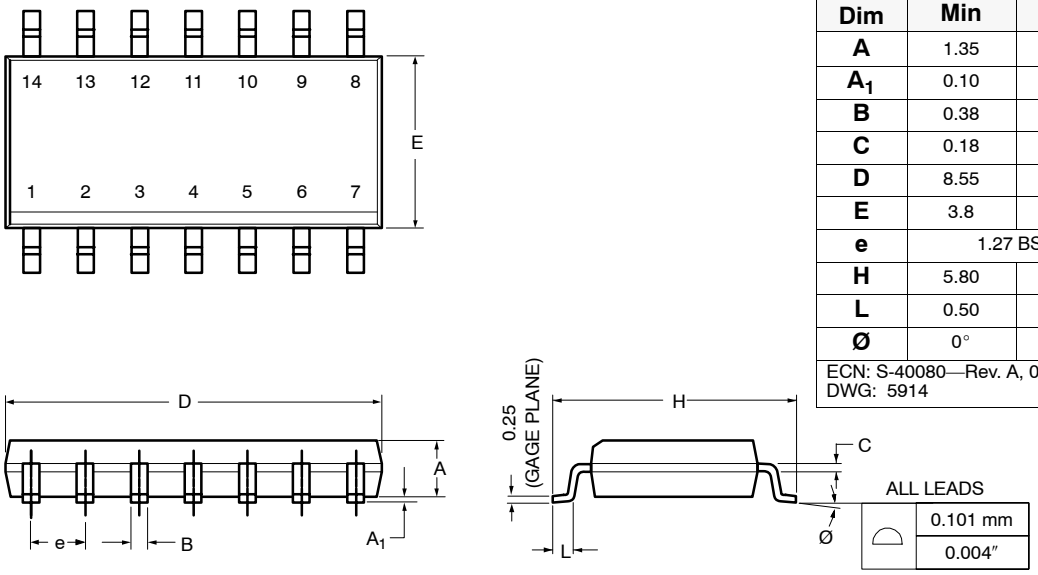
Fault Feedback

Detection of a shorted load sets a latch which turns off both the high-side and the low-side power transistors. If V_{CC} is present, a one level will be present on the FAULT output. To reset the system, the enable input, EN, must be lowered to a logic zero and then raised to a logic one. The logic level of the input, IN, will determine which power transistor will be turned on first after reset. An undervoltage condition on V_{DD} is not latched, but causes a one level on the FAULT output, if V_{CC} is present.

Static (dc) Operation

All components of a charge pump, except the holding (bootstrap) capacitor, are included in the circuit. This charge pump will provide current that is sufficient to overcome any leakage currents which would reduce the enhancement voltage of the high-side power transistor while it is on. This allows the high-side power transistor to be on continuously. When the low-side power transistor is turned on, additional charge is restored to the bootstrap capacitor, if needed. The maximum switching speed of the system at 50% duty cycle is limited by the on time of the low-side power transistor. During this time, the bootstrap capacitor charge must be restored. However, if the duty cycle is skewed so that the on time of the high-side power transistor is long enough for the charge pump to completely restore the charge lost during switching, then the on time of the low-side power transistor is not restricted.

SOIC (NARROW): 14-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	8.55	8.75	0.336	0.344
E	3.8	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: S-40080—Rev. A, 02-Feb-04
DWG: 5914

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