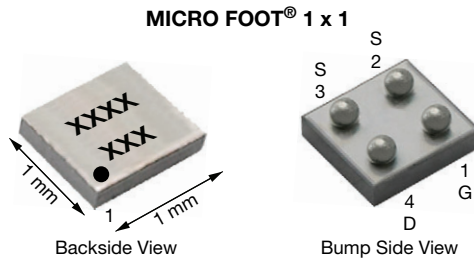


## N-Channel 8 V (D-S) MOSFET



Marking code: xxxx = 8466

PRODUCT SUMMARY	
$V_{DS}$ (V)	8
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.043
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5$ V	0.046
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 1.5$ V	0.060
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 1.2$ V	0.090
$Q_g$ typ. (nC)	6.8
$I_D$ (A) <sup>a, e</sup>	5.4
Configuration	Single

### FEATURES

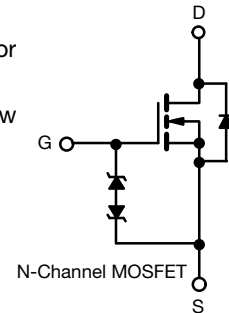
- TrenchFET<sup>®</sup> power MOSFET
- Typical ESD protection 3000 V HBM
- Ultra small 1 mm x 1 mm maximum outline
- Ultra thin 0.548 mm maximum height
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Low on-resistance load switch for portable devices
  - Low power consumption, low voltage drop
  - Increased battery life
  - Space savings on PCB



ORDERING INFORMATION	
Package	MICRO FOOT
Lead (Pb)-free and halogen-free	Si8466EDB-T2-E1

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	8	V
Gate-source voltage	$V_{GS}$	$\pm 5$	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_A = 25$ °C	5.4 <sup>a</sup>
		$T_A = 70$ °C	4.4 <sup>a</sup>
		$T_A = 25$ °C	3.6 <sup>b</sup>
		$T_A = 70$ °C	2.9 <sup>b</sup>
Pulsed drain current ( $t = 300$ $\mu$ s)	$I_{DM}$	20	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	0.65 <sup>b</sup>
Maximum power dissipation	$P_D$	$T_A = 25$ °C	1.8 <sup>a</sup>
		$T_A = 70$ °C	1.1 <sup>a</sup>
		$T_A = 25$ °C	0.78 <sup>b</sup>
		$T_A = 70$ °C	0.5 <sup>b</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Package reflow conditions <sup>c</sup>	VPR	260	
	IR/convection	260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>f, g</sup>	$t = 10$ s	$R_{thJA}$	55	70	°C/W
Maximum junction-to-ambient <sup>h, i</sup>	$t = 10$ s		125	160	

### Notes

- Surface mounted on 1" x 1" FR4 board with full copper,  $t = 10$  s
- Surface mounted on 1" x 1" FR4 board with minimum copper,  $t = 10$  s
- Refer to IPC/JEDEC<sup>®</sup> (J-STD-020), no manual or hand soldering
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump
- Based on  $T_A = 25$  °C
- Surface mounted on 1" x 1" FR4 board with full copper
- Maximum under steady state conditions is 100 °C/W
- Surface mounted on 1" x 1" FR4 board with minimum copper
- Maximum under steady state conditions is 190 °C/W

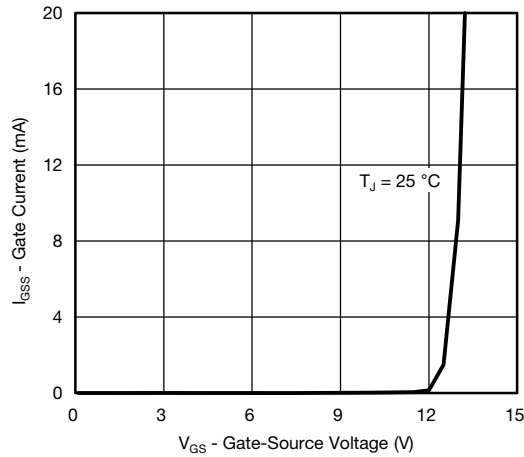
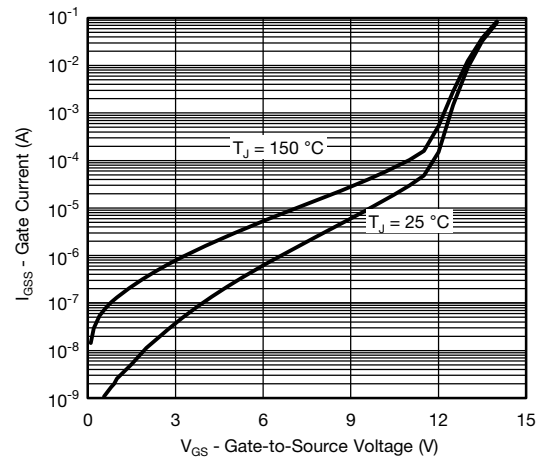
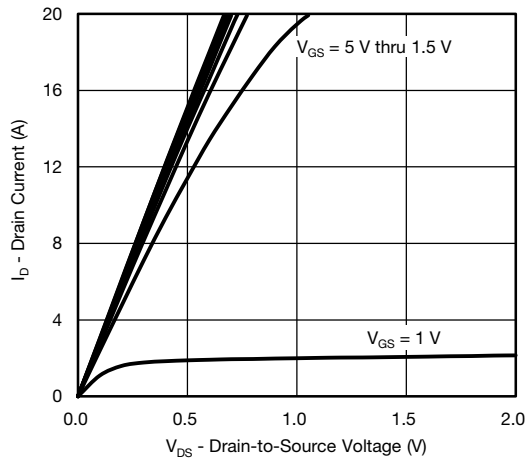
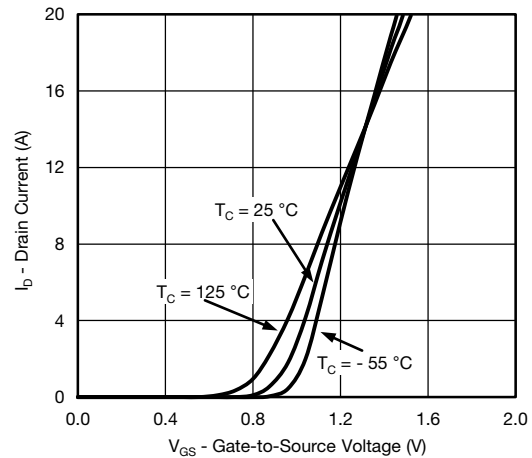
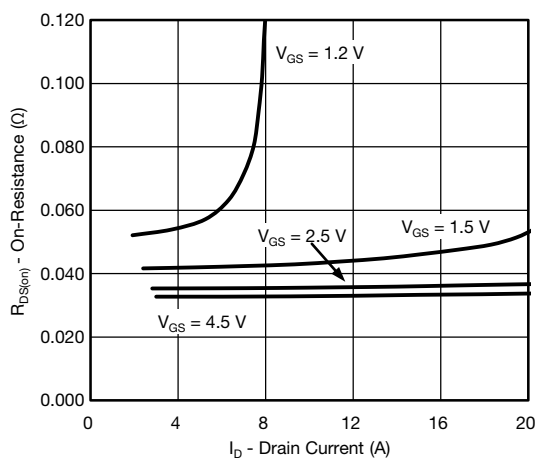
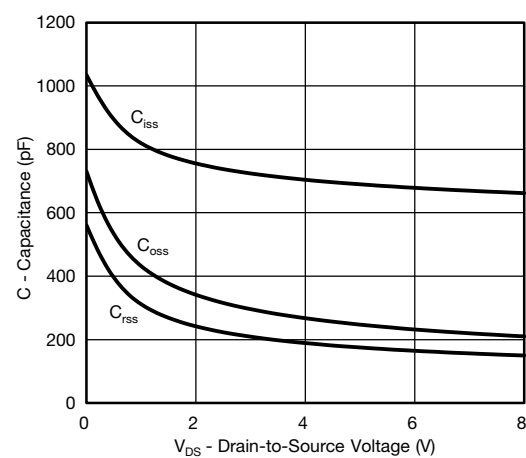


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	8	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	3.5	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	-3	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.35	-	0.7	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 5 V	-	-	± 3	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 8 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 8 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	10	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	10	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2 A	-	0.035	0.043	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1 A	-	0.037	0.046	
		V <sub>GS</sub> = 1.5 V, I <sub>D</sub> = 1 A	-	0.045	0.060	
		V <sub>GS</sub> = 1.2 V, I <sub>D</sub> = 0.5 A	-	0.055	0.090	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 4 V, I <sub>D</sub> = 2 A	-	30	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	710	-	pF
Output capacitance	C <sub>OSS</sub>		-	270	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	192	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2 A	-	8.5	13	nC
Gate-source charge	Q <sub>GS</sub>		-	0.9	-	
Gate-drain charge	Q <sub>GD</sub>		-	1.6	-	
Gate resistance	R <sub>g</sub>	V <sub>GS</sub> = 0.1 V, f = 1 MHz	-	6	-	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 4 V, R <sub>L</sub> = 2 Ω, I <sub>D</sub> ≥ 2 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	10	20	ns
Rise time	t <sub>r</sub>		-	15	30	
Turn-off delay time	t <sub>d(off)</sub>		-	40	80	
Fall time	t <sub>f</sub>		-	10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>A</sub> = 25 °C	-	-	1.5	A
Pulse diode forward current	I <sub>SM</sub>		-	-	20	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.5 A, V <sub>GS</sub> = 0 V	-	0.7	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 2 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	30	60	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	7	15	nC
Reverse recovery fall time	t <sub>a</sub>		-	15	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	15	-	

**Notes**

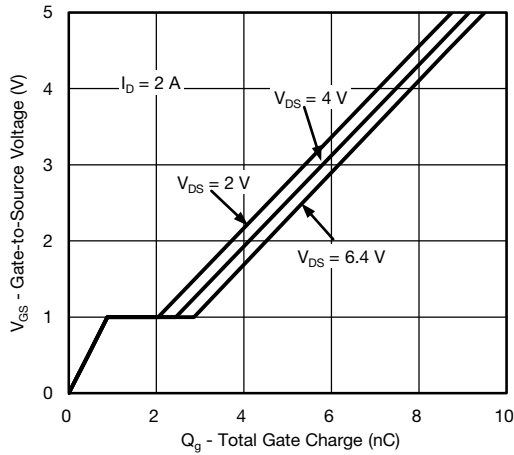
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

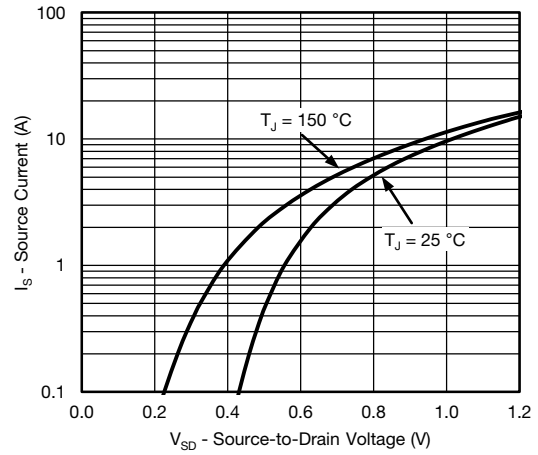
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**



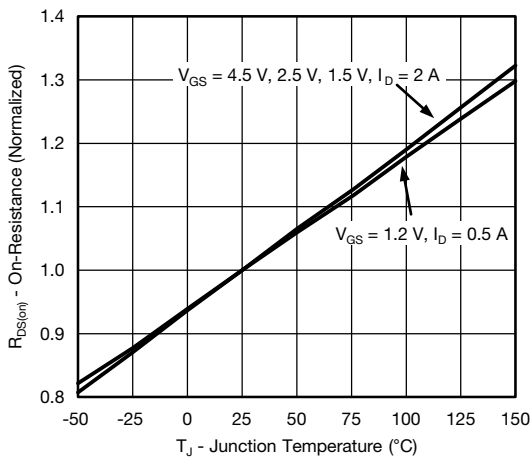
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



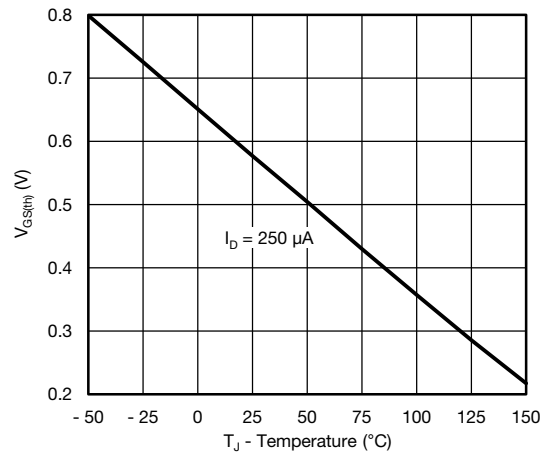
Gate Charge



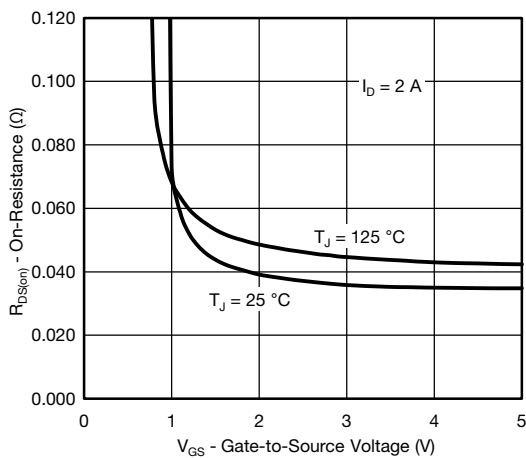
Source-Drain Diode Forward Voltage



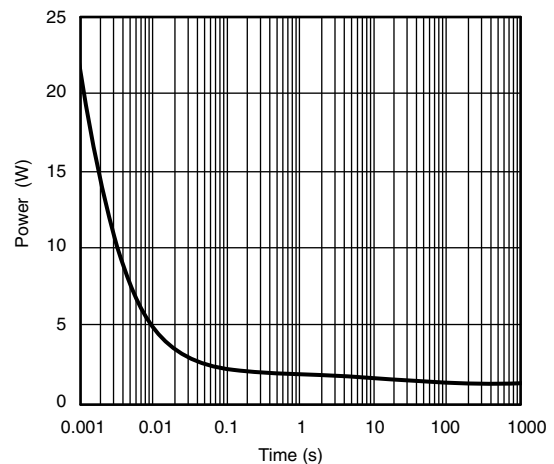
On-Resistance vs. Junction Temperature



Threshold Voltage

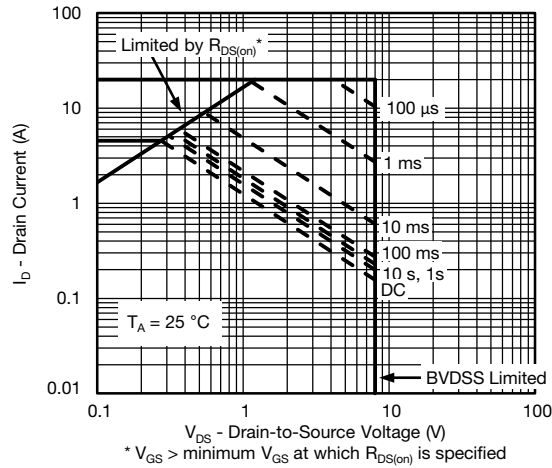


On-Resistance vs. Gate-to-Source Voltage

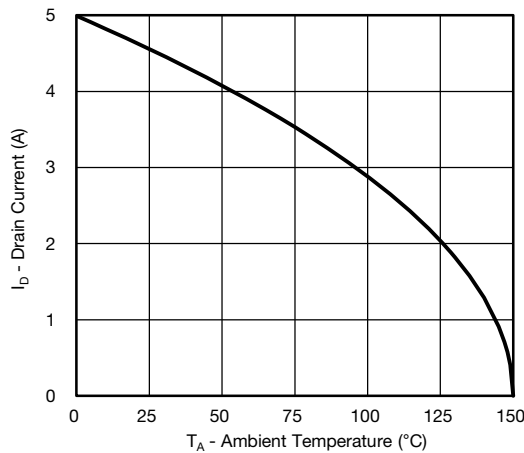


Single Pulse Power, Junction-to-Ambient

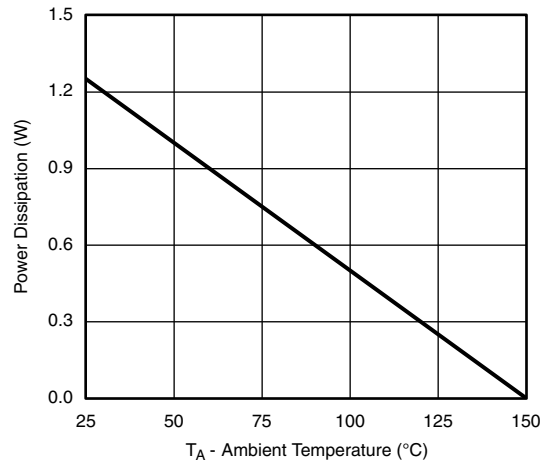
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Safe Operating Area, Junction-to-Ambient**



**Current Derating <sup>a</sup>**



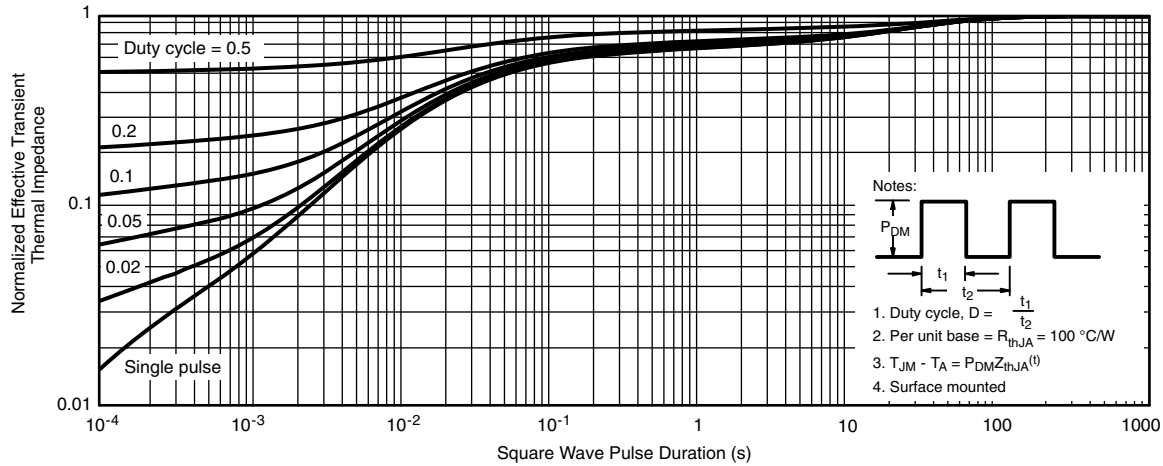
**Power Derating**

**Notes**

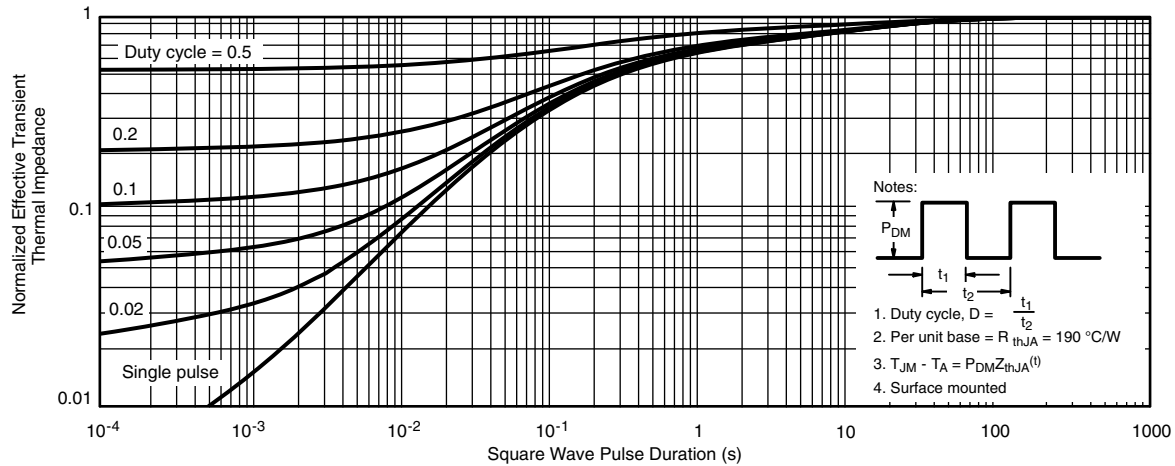
- When mounted on 1" x 1" FR4 with full copper
- a. The power dissipation  $P_D$  is based on  $T_J \text{ max.} = 150 \text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)**



**Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63683](http://www.vishay.com/ppg?63683).

## MICRO FOOT®: 4-Bumps (1 mm x 1 mm, 0.5 mm Pitch, 0.286 mm Bump Height)



### Notes

- Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
- Backside surface is coated with a Ti/Ni/Ag layer.
- Non-solder mask defined copper landing pad.
- Laser mark on the backside surface of die.
- "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.458	0.504	0.550	0.0180	0.0198	0.0217
A1	0.214	0.250	0.286	0.0084	0.0098	0.0113
A2	0.244	0.254	0.264	0.0096	0.0100	0.0104
b	0.297	0.330	0.363	0.0117	0.0130	0.0143
b1	0.250			0.0098		
e	0.500			0.0197		
s	0.210	0.230	0.250	0.0083	0.0091	0.0096
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
K	0.029	0.065	0.102	0.0011	0.0026	0.0040

### Note

- Use millimeters as the primary measurement.

ECN: T15-0176-Rev. A, 27-Apr-15  
DWG: 6039



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