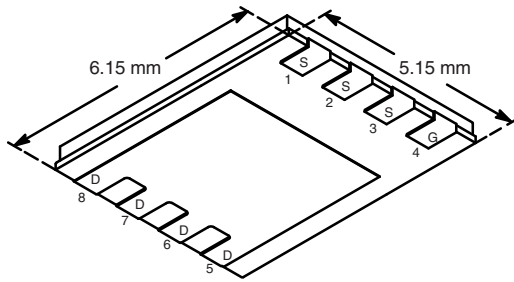


## N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
30	0.0033 at V <sub>GS</sub> = 10 V	40	37 nC
	0.0046 at V <sub>GS</sub> = 4.5 V	40	

PowerPAK SO-8



Bottom View

Ordering Information: Si7674DP-T1-E3 (Lead (Pb)-free)  
Si7674DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

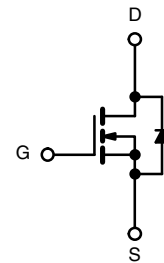
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q<sub>gd</sub> for Switching Losses
- 100 % R<sub>g</sub> Tested
- 100 % Capacitance Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Core DC/DC in Notebooks



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	40	
		T <sub>C</sub> = 70 °C	32	
		T <sub>A</sub> = 25 °C	31 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	25 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	70	A	
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C		40
		T <sub>A</sub> = 25 °C		4.9 <sup>b, c</sup>
Single Pulse Avalanche Current	I <sub>AS</sub>	40		mJ
Single Pulse Avalanche Energy	E <sub>AS</sub>	80		
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	83	
		T <sub>C</sub> = 70 °C	53	
		T <sub>A</sub> = 25 °C	5.4 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.4 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	18	23	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.0	1.5	

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 65 °C/W.

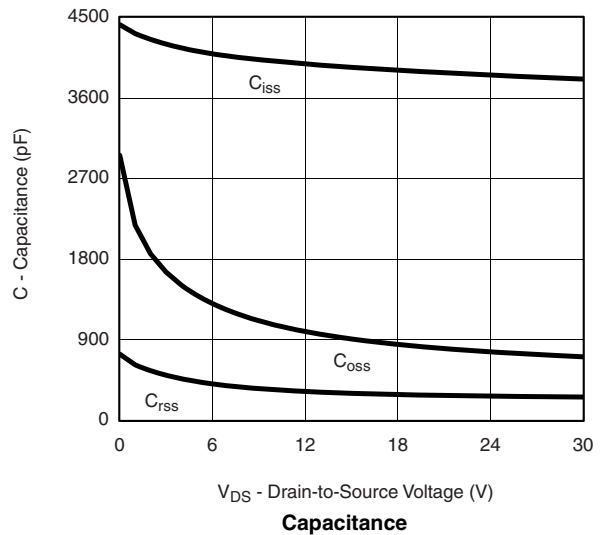
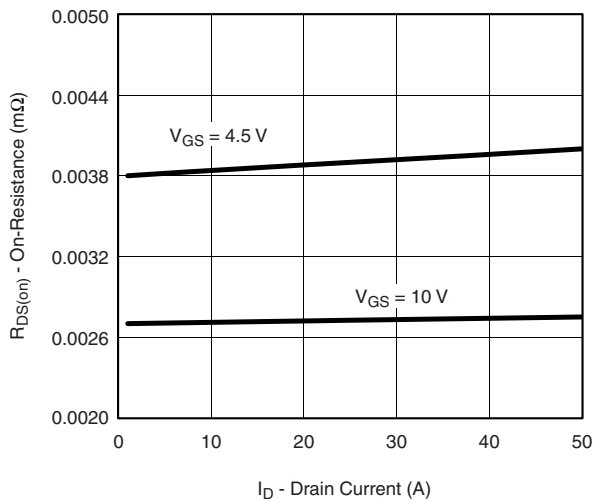
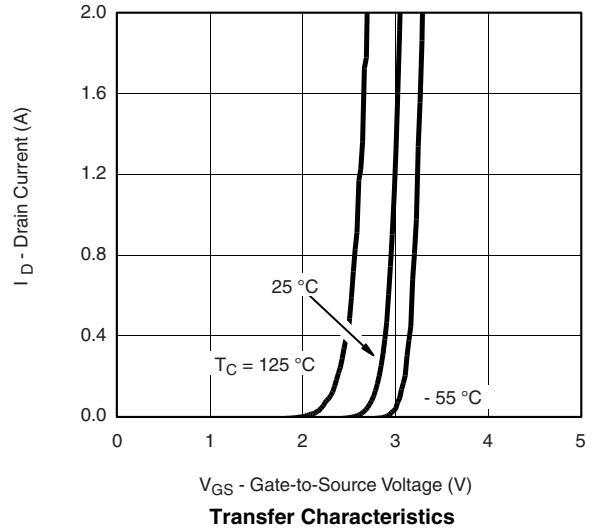
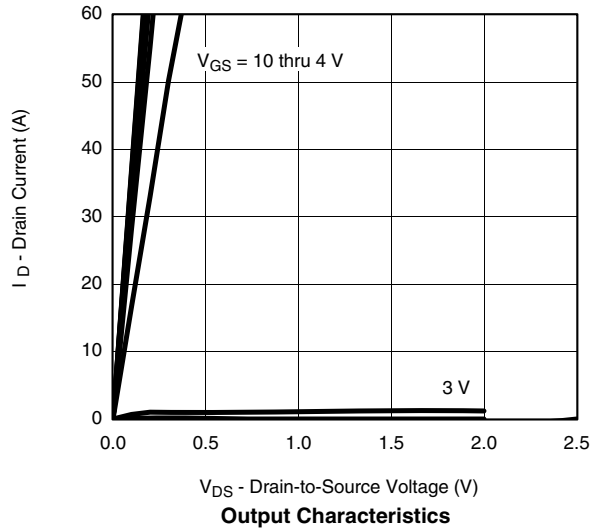
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		33		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		3.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0027	0.0033	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0038	0.0046	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		87		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3940	5910	$\mu\text{F}$
Output Capacitance	$C_{oss}$		910	1365		
Reverse Transfer Capacitance	$C_{rss}$		305	458		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		60	90	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		28	42	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		13.6		
Gate-Drain Charge	$Q_{gd}$			6.8		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		0.95	1.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		16	25	ns
Rise Time	$t_r$			98	150	
Turn-Off Delay Time	$t_{d(off)}$			32	50	
Fall Time	$t_f$			8	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		34	50	
Rise Time	$t_r$			210	315	
Turn-Off Delay Time	$t_{d(off)}$			26	40	
Fall Time	$t_f$			9	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			40	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				70	
Body Diode Voltage	$V_{SD}$	$I_S = 5\text{ A}$		0.75	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		47	70	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			50	80	nC
Reverse Recovery Fall Time	$t_a$			23		ns
Reverse Recovery Rise Time	$t_b$			24		

Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

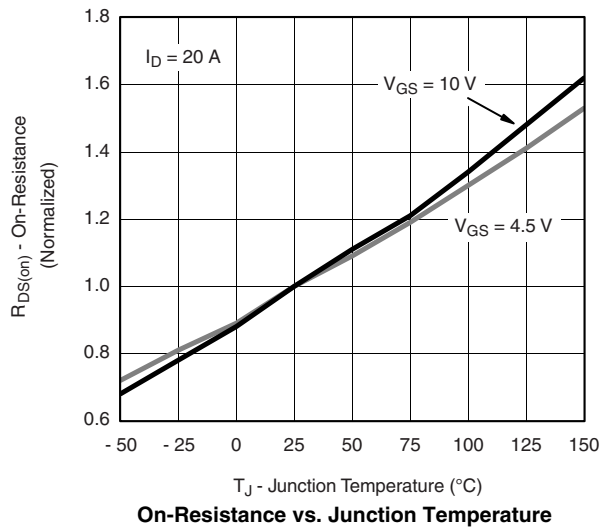
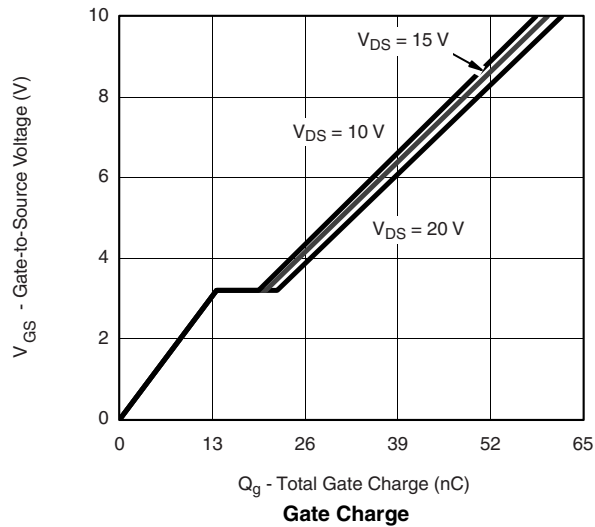
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



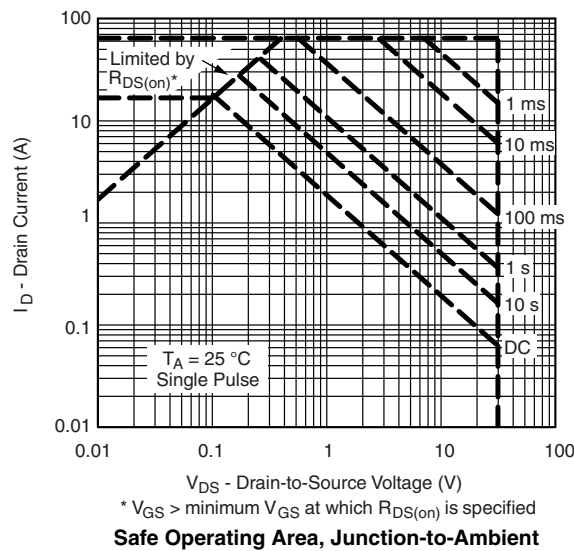
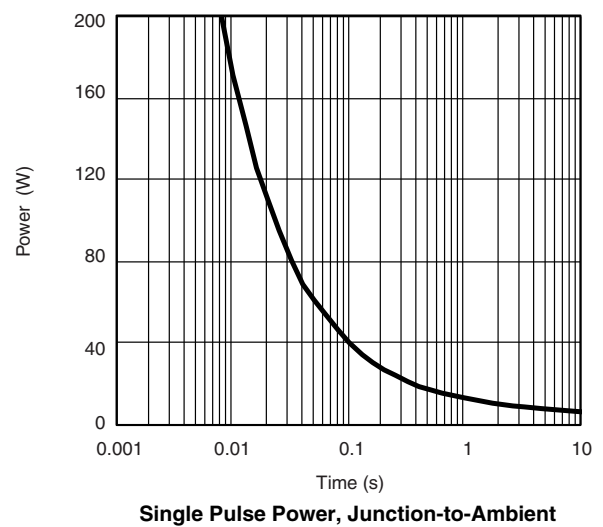
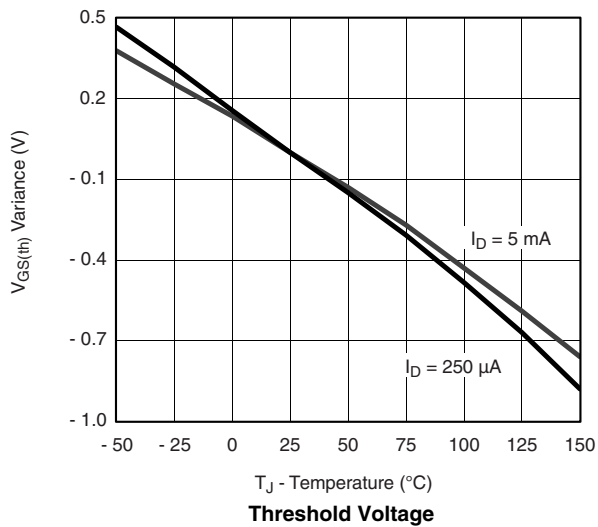
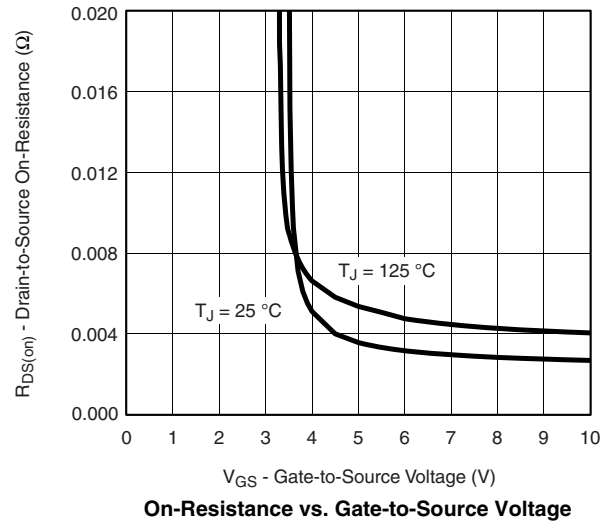
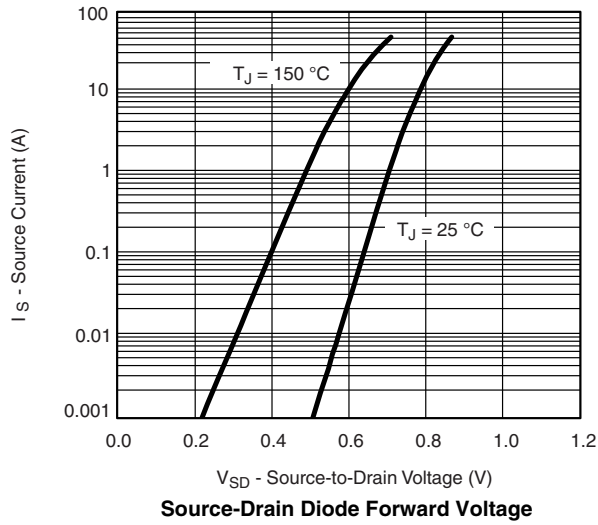
**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

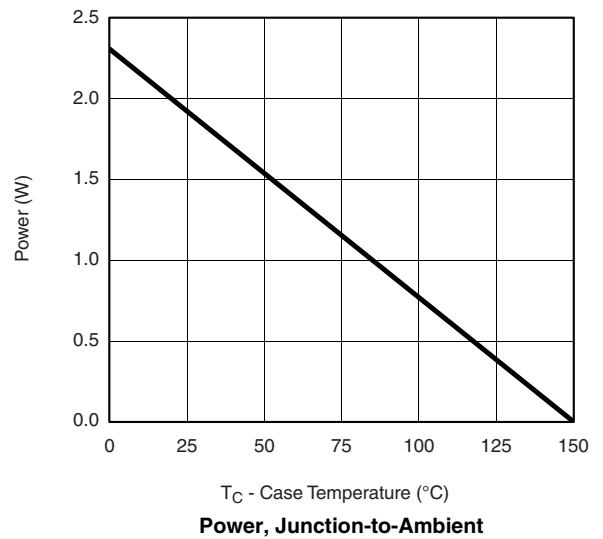
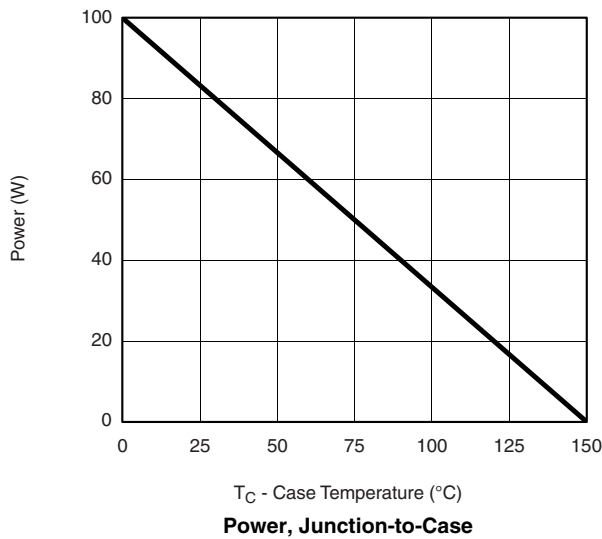
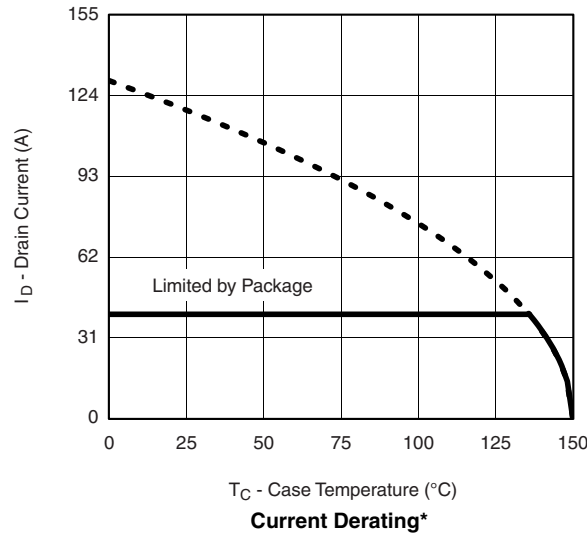


**On-Resistance vs. Junction Temperature**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

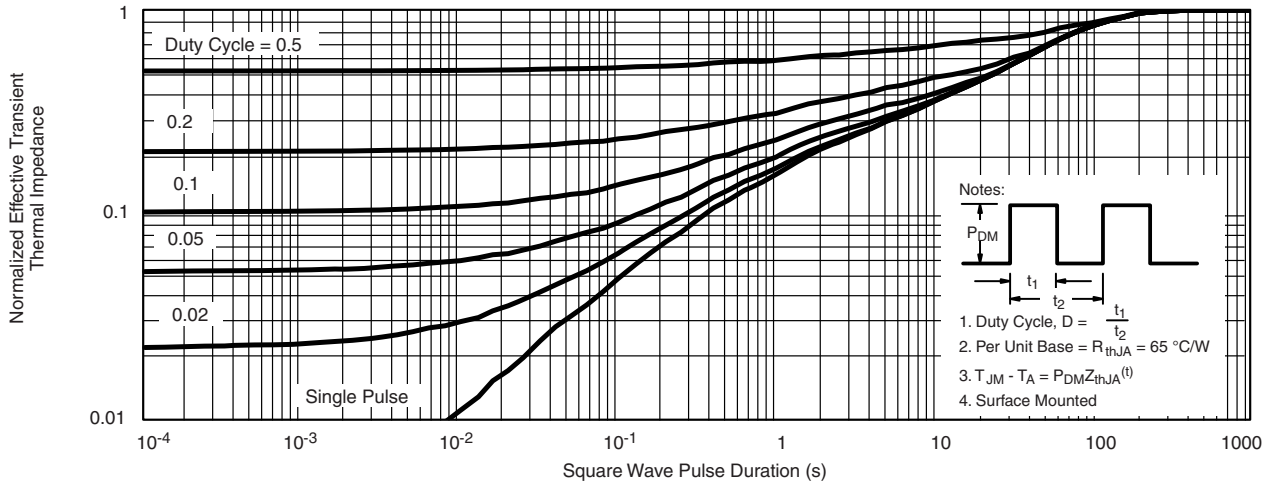


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

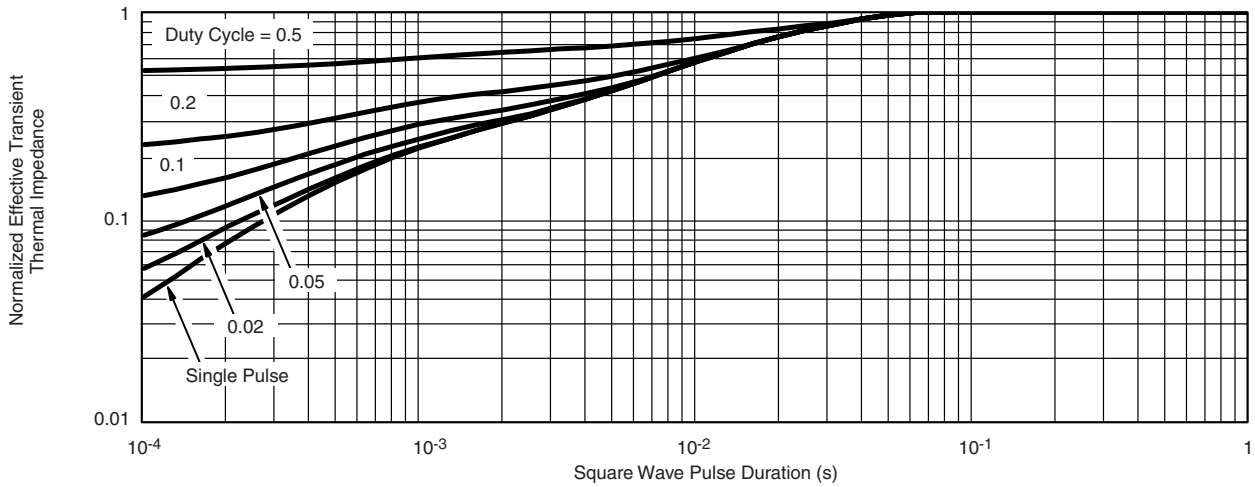


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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