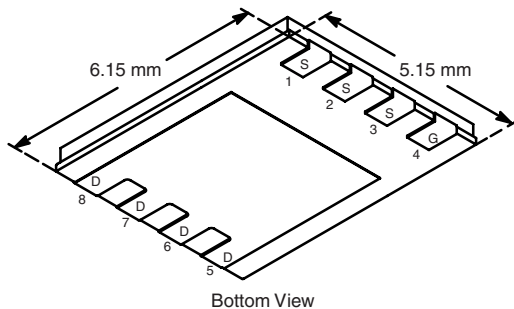


N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.0031 at $V_{GS} = 10$ V	40	37 nC
	0.0036 at $V_{GS} = 4.5$ V	40	

PowerPAK SO-8



Ordering Information: Si7664DP-T1-E3 (Lead (Pb)-free)
Si7664DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

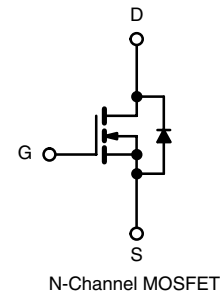
FEATURES

- Halogen-free available
- TrenchFET[®] Power MOSFET
- PWM Optimized
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g , Capacitance and UIS Tested



APPLICATIONS

- Synchronous - Low Side
- Notebook
- Server
- Workstation



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	40
		$T_C = 70$ °C	32
		$T_A = 25$ °C	31 ^{b, c}
		$T_A = 70$ °C	25 ^{b, c}
Pulsed Drain Current	I_{DM}	70	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	4.9 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	40	mJ
Single Pulse Avalanche Energy	E_{AS}	80	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	83
		$T_C = 70$ °C	53
		$T_A = 25$ °C	5.4 ^{b, c}
		$T_A = 70$ °C	3.4 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	18	23	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.5		

Notes:

- Based on $T_C = 25$ °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 65 °C/W.

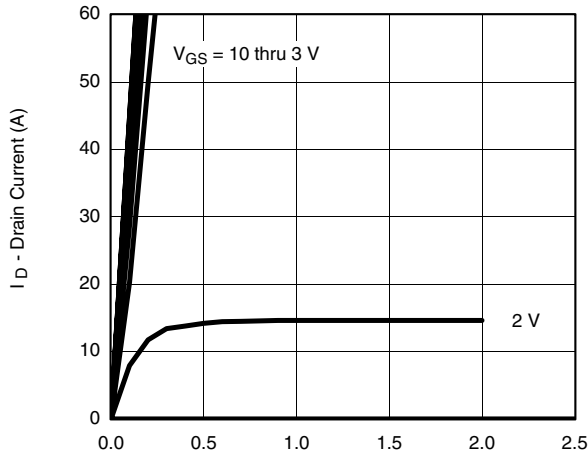
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.0		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.8	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0025	0.0031	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0029	0.0036	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		108		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		5180	7770	pF
Output Capacitance	C_{oss}			880	1320	
Reverse Transfer Capacitance	C_{riss}			305	458	
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		85	125	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		38	55	
Gate-Source Charge	Q_{gs}			10.5		
Gate-Drain Charge	Q_{gd}		5.5			
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.95	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		14	21	ns
Rise Time	t_r			100	150	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			8	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		28	45	
Rise Time	t_r			103	155	
Turn-Off Delay Time	$t_{d(off)}$			41	65	
Fall Time	t_f			9	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			40	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$		0.73	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		35	55	ns
Body Diode Reverse Recovery Charge	Q_{rr}			35	55	nC
Reverse Recovery Fall Time	t_a			18		ns
Reverse Recovery Rise Time	t_b			17		

Notes:

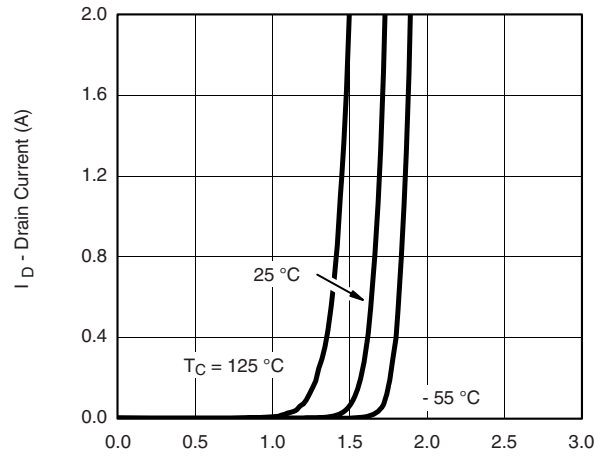
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

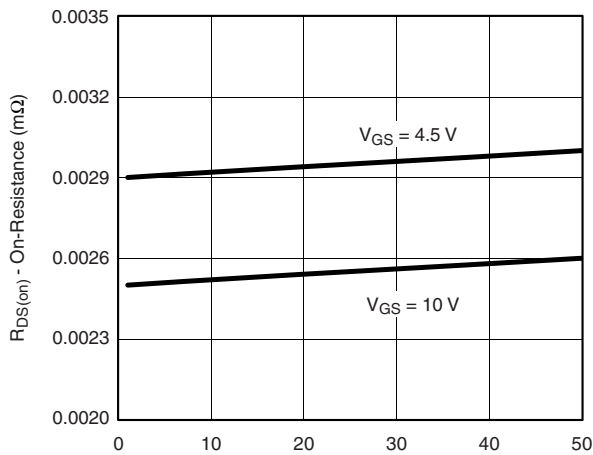
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



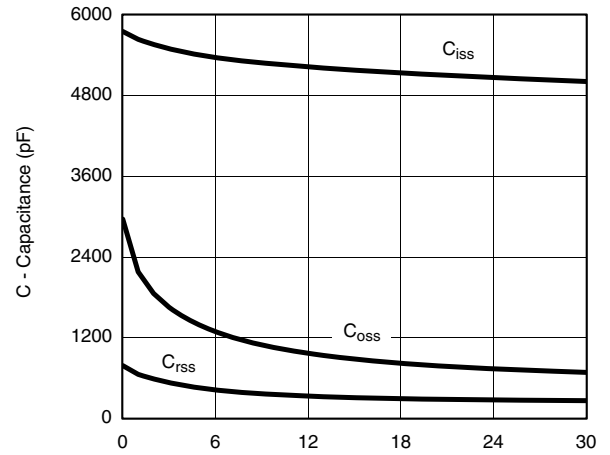
Output Characteristics



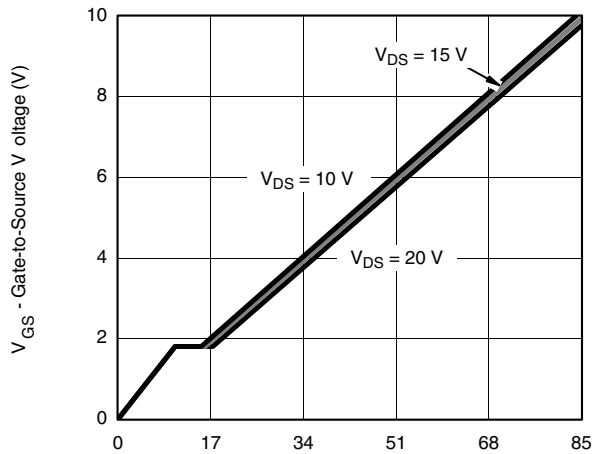
Transfer Characteristics



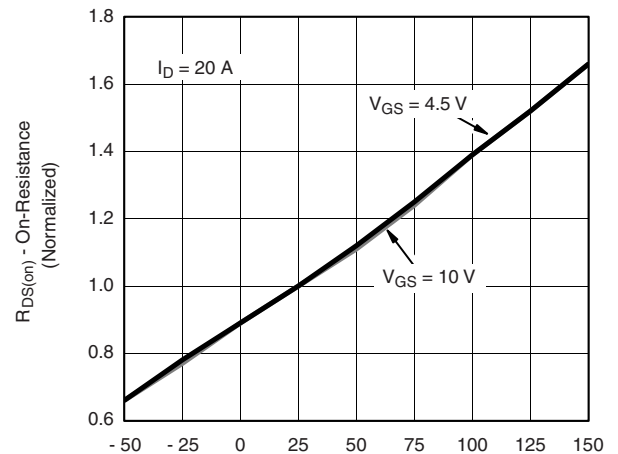
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

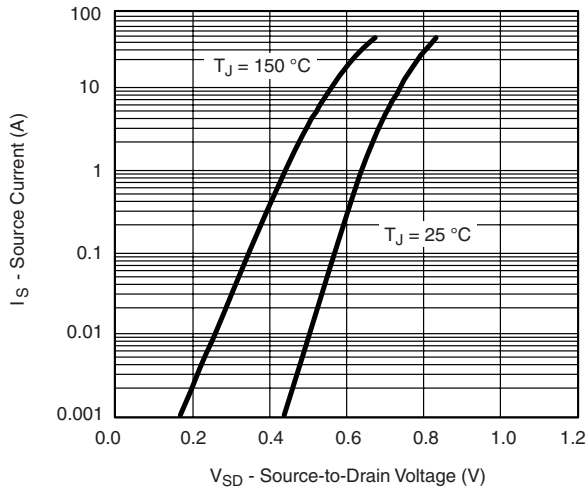


Gate Charge

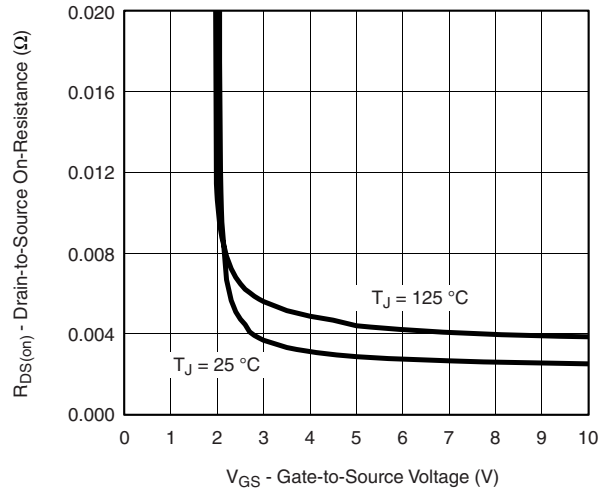


On-Resistance vs. Junction Temperature

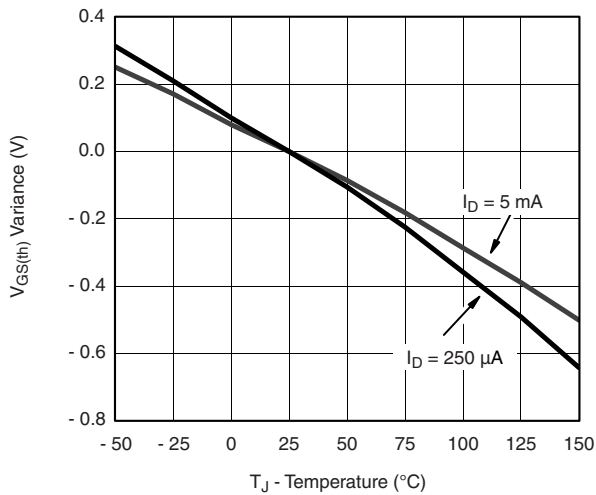
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



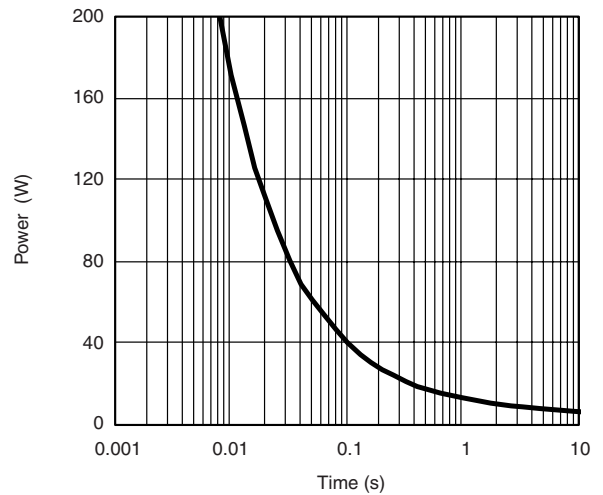
Source-Drain Diode Forward Voltage



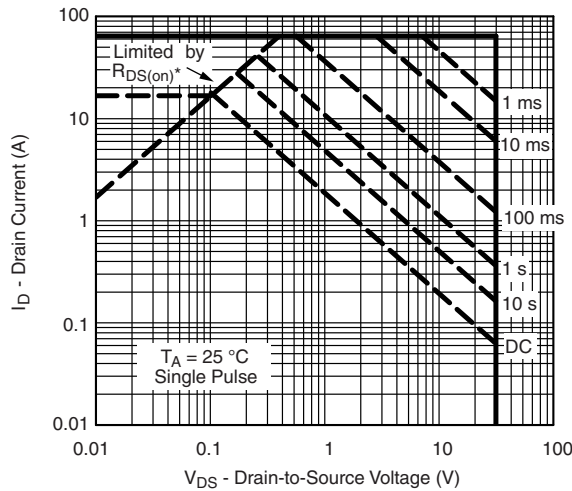
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



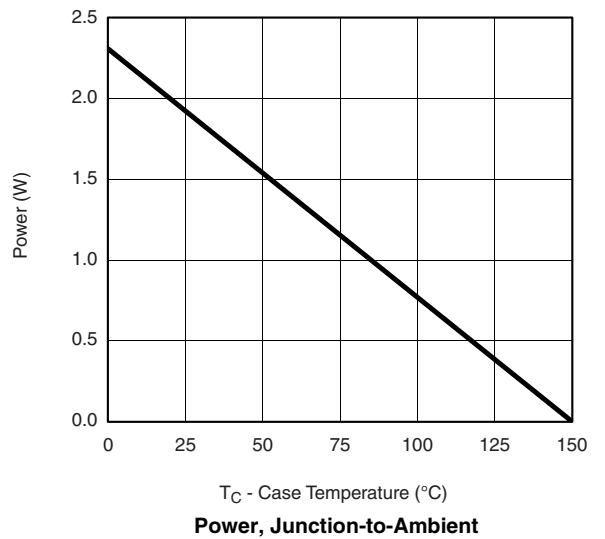
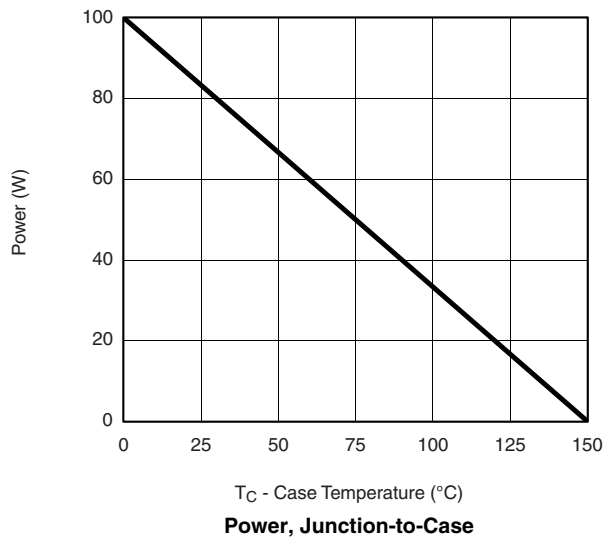
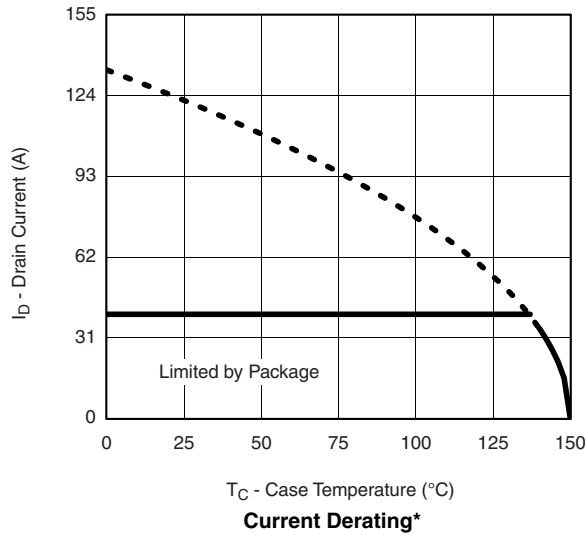
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

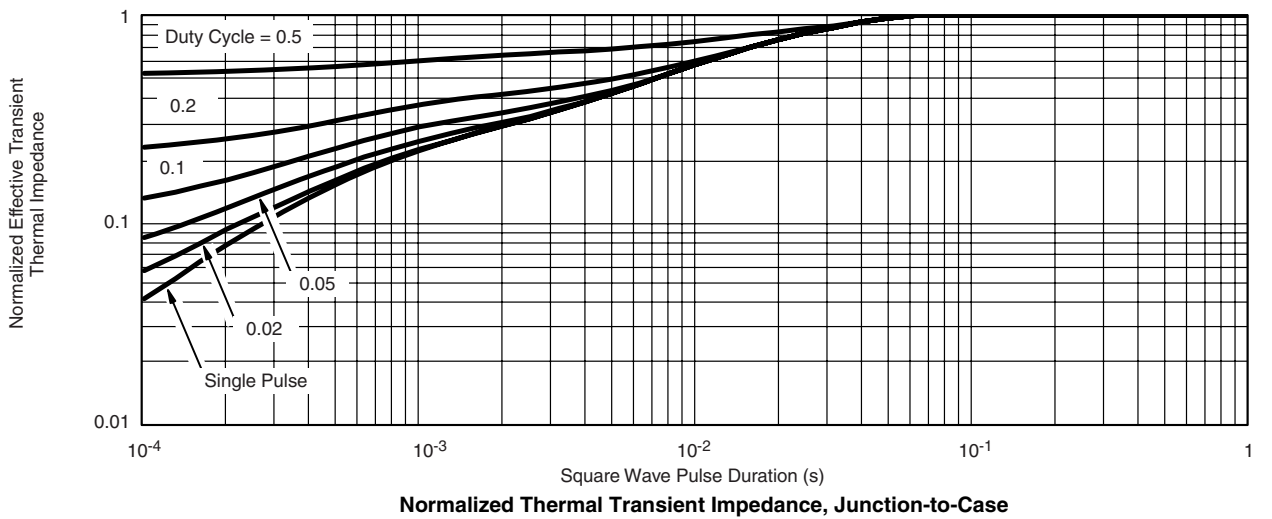
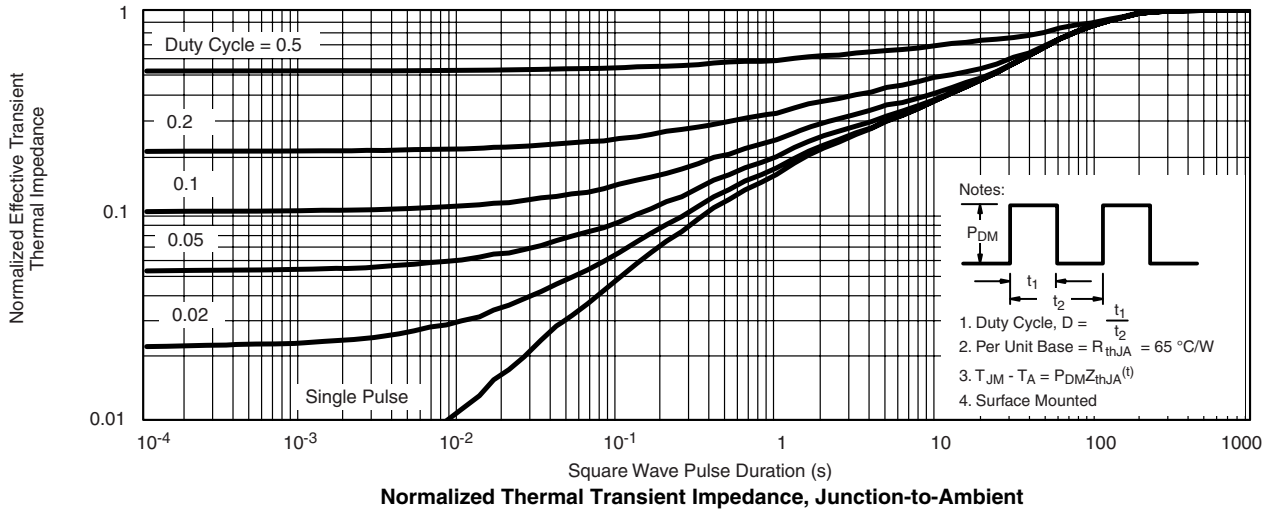
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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