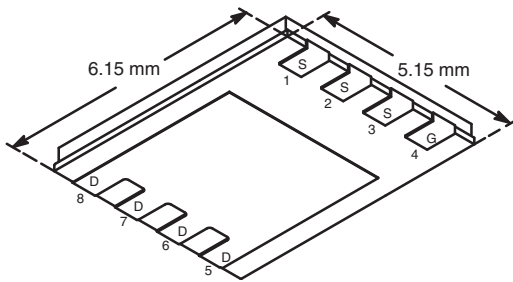


## N-Channel Reduced $Q_g$ , Fast Switching MOSFET

<b>PRODUCT SUMMARY</b>			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
30	0.0075 at $V_{GS} = 10$ V	30	12
	0.0115 at $V_{GS} = 4.5$ V	30	

PowerPAK SO-8



Bottom View

Ordering Information: Si7392ADP-T1-E3 (Lead (Pb)-free)  
Si7392ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

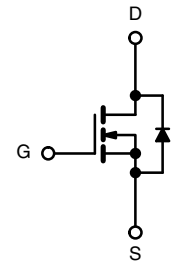
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low  $Q_{gd}$  for Low Switching Losses
- TrenchFET<sup>®</sup> Power MOSFET
- New Low Thermal Resistance PowerPAK<sup>®</sup> Package with Low 1.07 mm Profile
- 100 %  $R_g$  Tested
- Complaint to RoHS Directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE  
Available

### APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook
  - Server



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	$I_{DM}$	50	
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	A
		$T_A = 25$ °C	
Avalanche Current	$I_{AS}$	25	
Single Pulse Avalanche Energy	$E_{AS}$	30	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	20	25	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	3.5	4.5	

Notes:

- Based on  $T_C = 25$  °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- See solder profile ([www.vishay.com/ppg?73461](http://www.vishay.com/ppg?73461)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

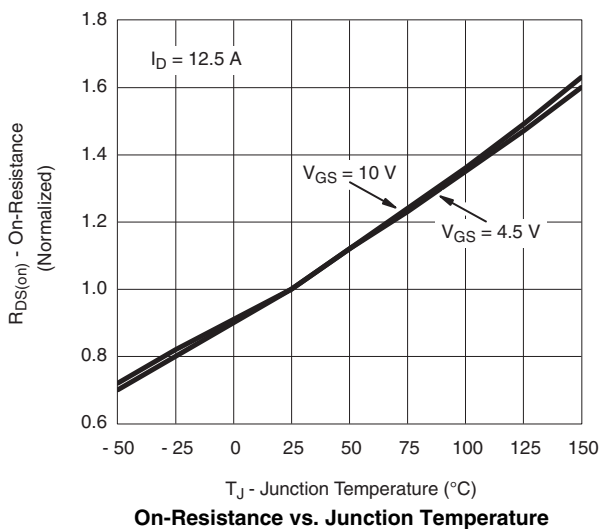
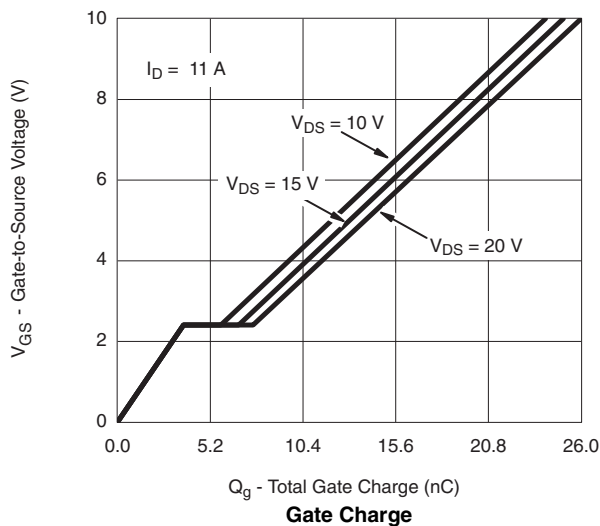
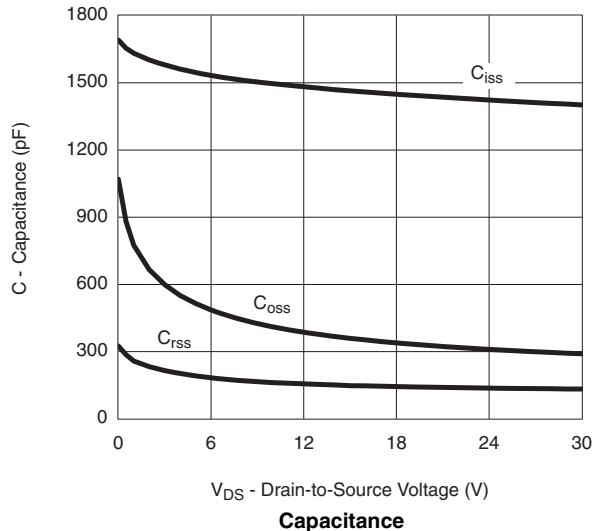
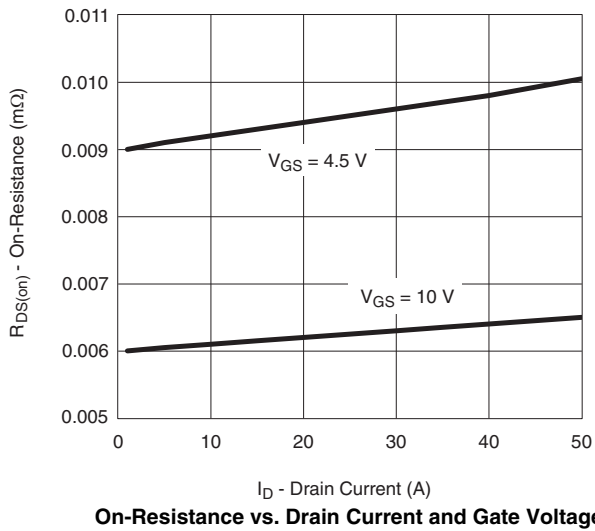
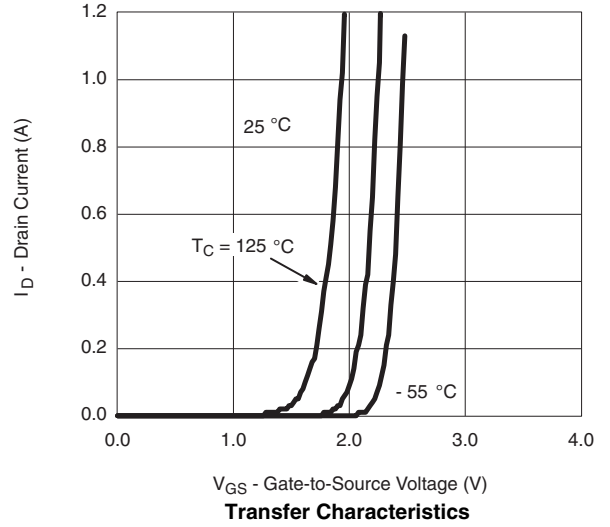
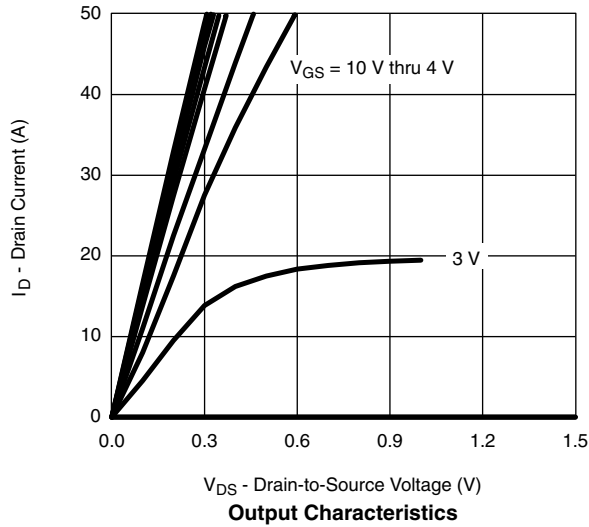
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 1\text{ }\mu\text{A to } 250\text{ }\mu\text{A}$		30		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12.5\text{ A}$		0.006	0.0075	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.009	0.0115	
Forward Transconductance	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 12.5\text{ A}$		46		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1465		pF
Output Capacitance	$C_{oss}$			360		
Reverse Transfer Capacitance	$C_{riss}$			150		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 12.5\text{ A}$		25	38	nC
			$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 12.5\text{ A}$		12	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 12.5\text{ A}$		3.7		nC
Gate-Drain Charge	$Q_{gd}$			3.1		
Gate Resistance	$R_g$		$f = 1\text{ MHz}$		1.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		16	25	ns
Rise Time	$t_r$			50	75	
Turn-Off Delay Time	$t_{d(off)}$			21	32	
Fall Time	$t_f$			8	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		8	15	ns
Rise Time	$t_r$			35	55	
Turn-Off Delay Time	$t_{d(off)}$			23	35	
Fall Time	$t_f$			8	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			30	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				50	
Body Diode Voltage	$V_{SD}$	$I_S = 2.7\text{ A}$		0.73	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		26	40	nC
Body Diode Reverse Recovery Charge	$Q_{rr}$			19	30	
Reverse Recovery Fall Time	$t_a$			13		ns
Reverse Recovery Rise Time	$t_b$			13		

Notes:

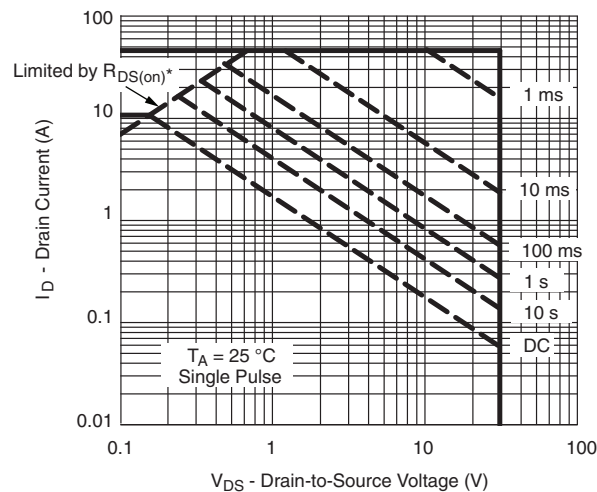
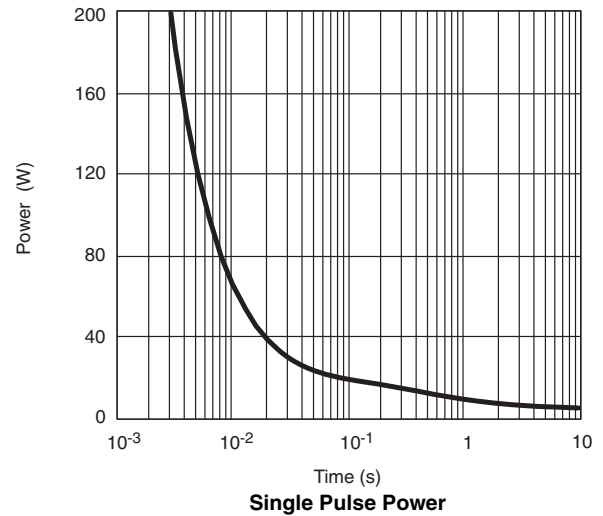
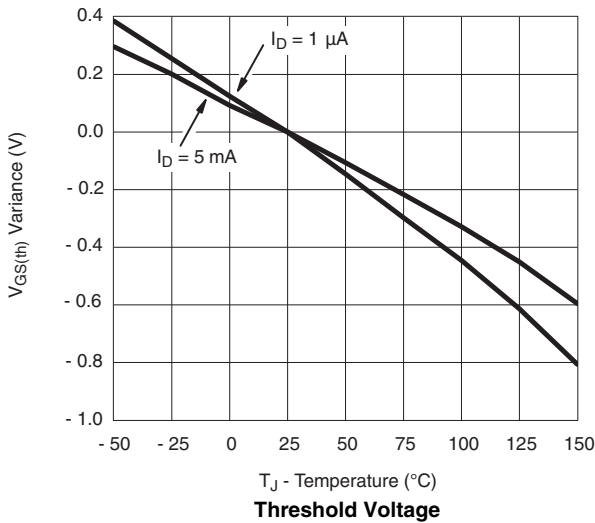
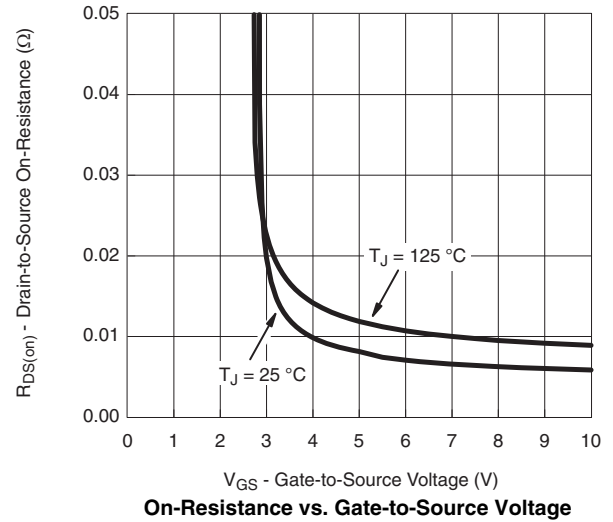
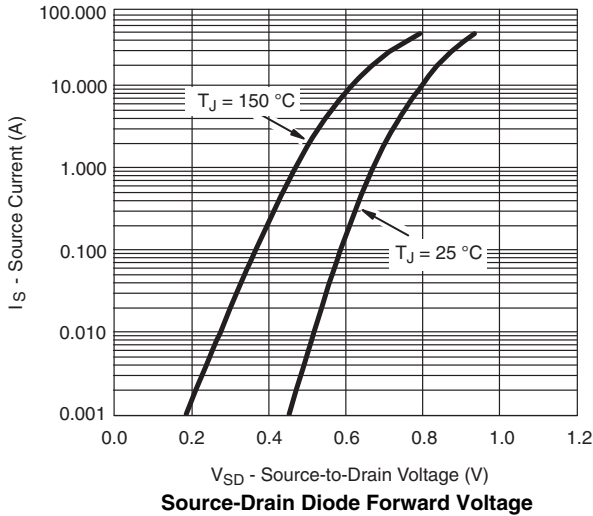
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

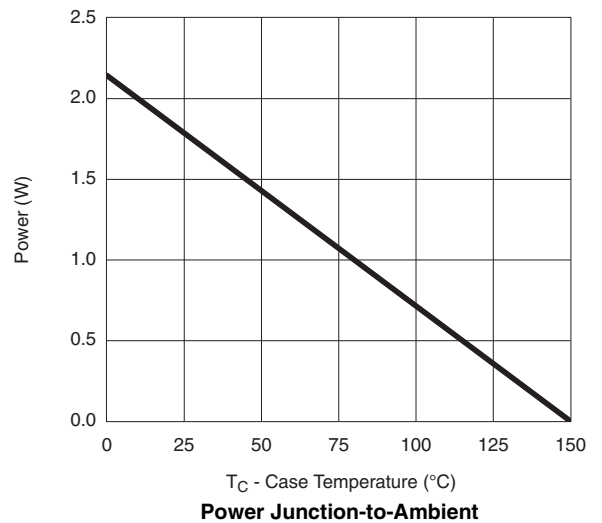
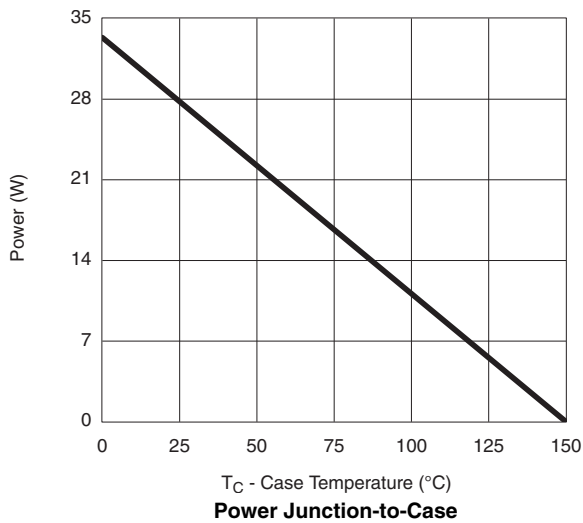
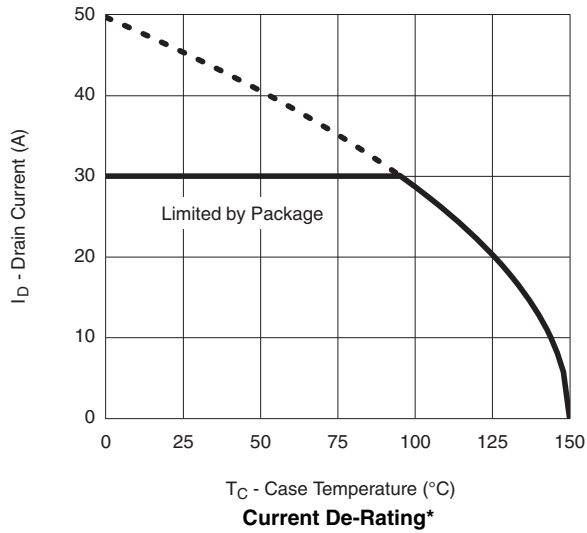


**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



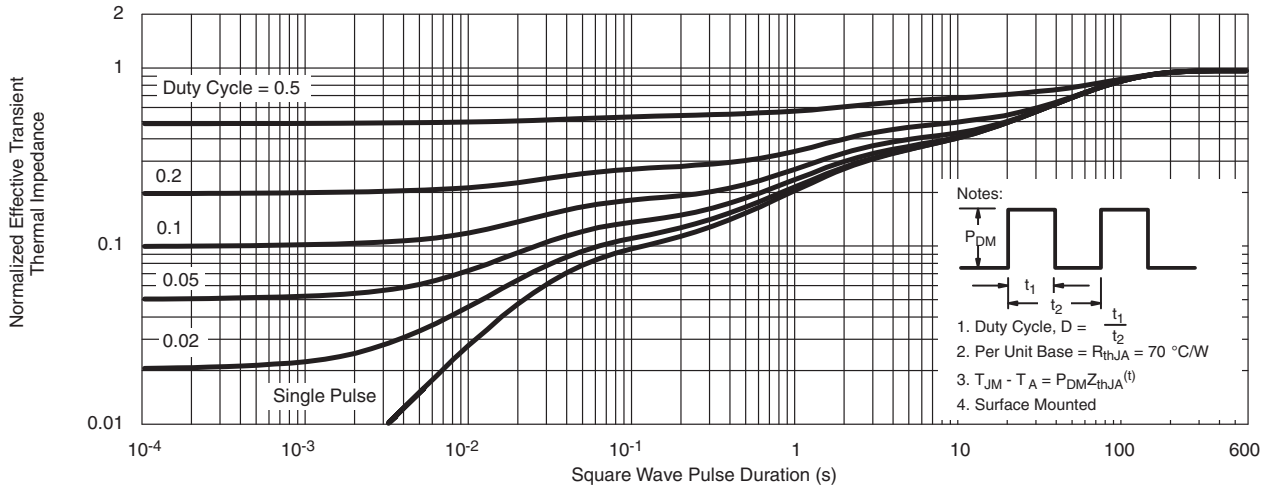
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

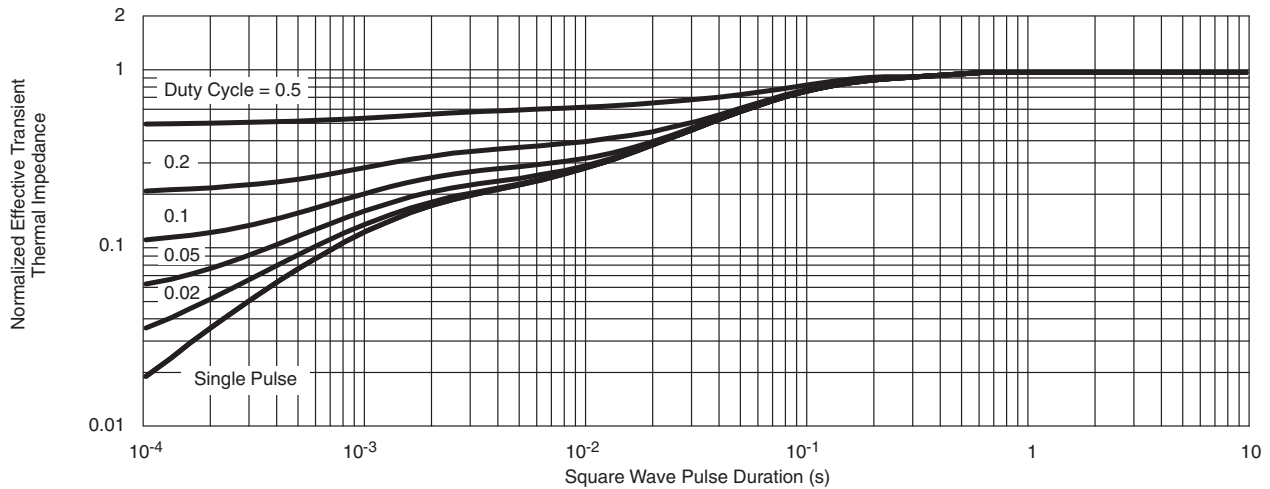


\* The power dissipation PD is based on  $T_{J(max)} = 150\text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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