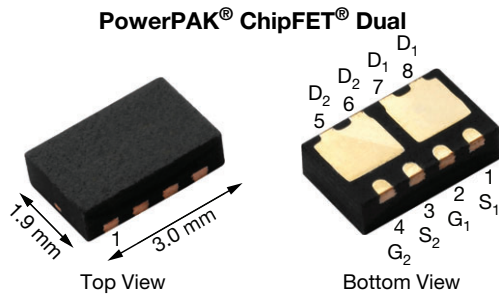


Dual N-Channel 30 V (D-S) MOSFET



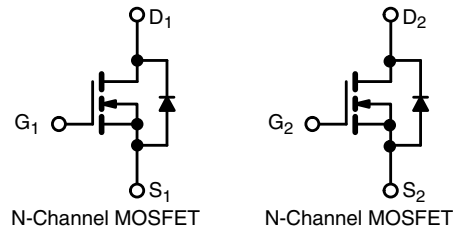
FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® ChipFET® package
 - Small footprint area
 - Low on-resistance
 - Thin 0.8 mm profile
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Network
- System power DC/DC



Marking code: CF

PRODUCT SUMMARY	
V _{DS} (V)	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.030
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.040
Q _g typ. (nC)	3.5
I _D (A) ^a	6
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAK ChipFET
Lead (Pb)-free and halogen-free	Si5936DU-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	30	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	6 ^a
		T _C = 70 °C	6 ^a
		T _A = 25 °C	6 ^{a, b, c}
		T _A = 70 °C	5.3 ^{b, c}
Pulsed drain current (t = 300 μs)	I _{DM}	25	A
Continuous source-drain diode current	I _S	T _C = 25 °C	
		T _A = 25 °C	1.9 ^{b, c}
Maximum power dissipation	P _D	T _C = 25 °C	10.4
		T _C = 70 °C	6.7
		T _A = 25 °C	2.3 ^{b, c}
		T _A = 70 °C	1.5 ^{b, c}
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	t ≤ 5 s	R _{thJA}	43	55	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	9.5	12	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- t = 5 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 105 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	34	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-4.4	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2	-	2.2	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A	-	0.025	0.030	Ω
		V _{GS} = 4.5 V, I _D = 4 A	-	0.032	0.040	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5 A	-	11	-	S
Dynamic ^b						
Input capacitance	C _{ISS}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	320	-	pF
Output capacitance	C _{OSS}		-	70	-	
Reverse transfer capacitance	C _{RSS}		-	38	-	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 7 A	-	7	11	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 7 A	-	3.5	5.3	
Gate-source charge	Q _{gs}		-	1	-	
Gate-drain charge	Q _{gd}		-	1.3	-	
Gate resistance	R _g	f = 1 MHz	0.8	4	8	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 2.8 Ω I _D ≅ 5.3 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	65	130	
Turn-off delay time	t _{d(off)}		-	15	30	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 2.8 Ω I _D ≅ 5.3 A, V _{GEN} = 10 V, R _g = 1 Ω	-	5	10	
Rise time	t _r		-	12	25	
Turn-off delay time	t _{d(off)}		-	12	25	
Fall time	t _f		-	6	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	6	A
Pulse diode forward current	I _{SM}		-	-	25	
Body diode voltage	V _{SD}	I _S = 5.3 A, V _{GS} = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 5.3 A, di/dt = 100 A/μs, T _J = 25 °C	-	11	20	ns
Body diode reverse recovery charge	Q _{rr}		-	5	10	nC
Reverse recovery fall time	t _a		-	6	-	ns
Reverse recovery rise time	t _b		-	5	-	

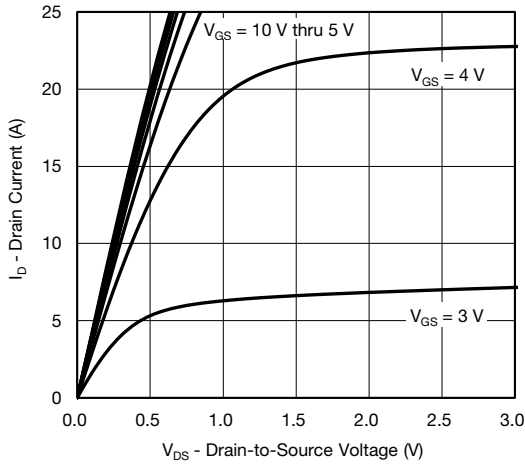
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

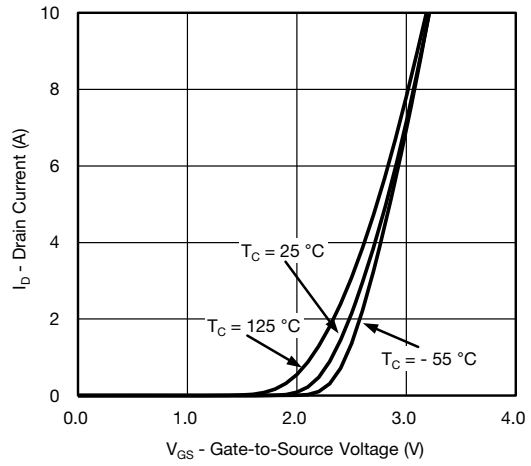
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



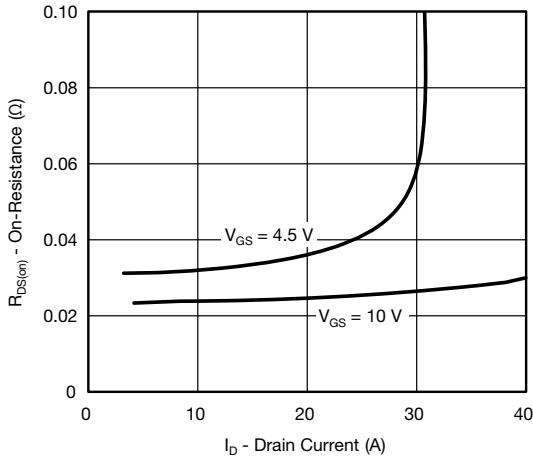
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



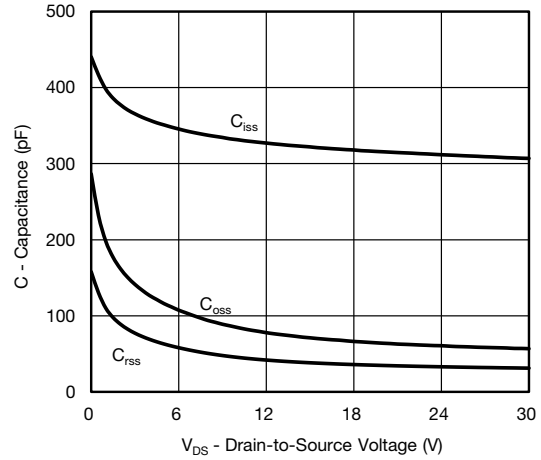
Output Characteristics



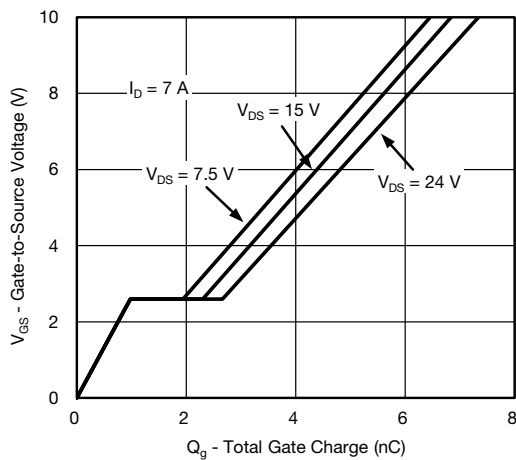
Transfer Characteristics



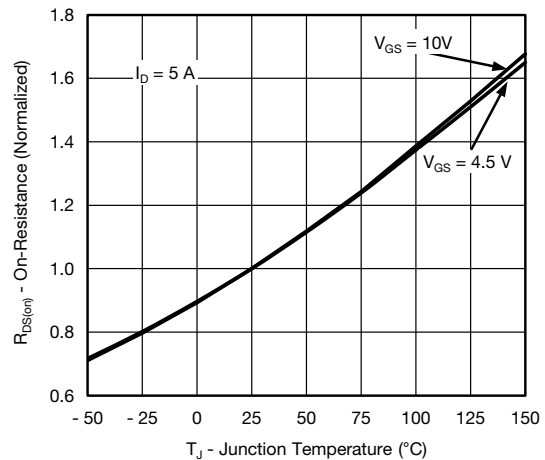
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



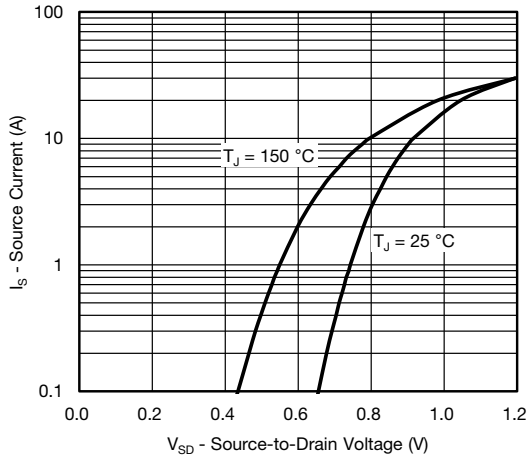
Gate Charge



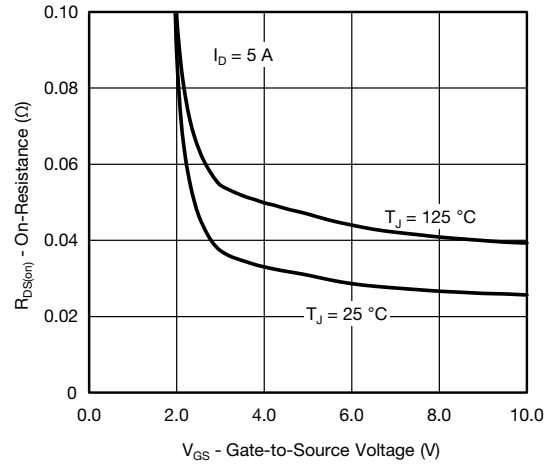
On-Resistance vs. Junction Temperature



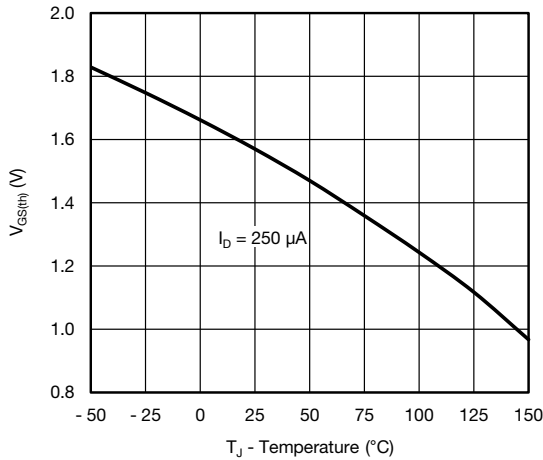
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



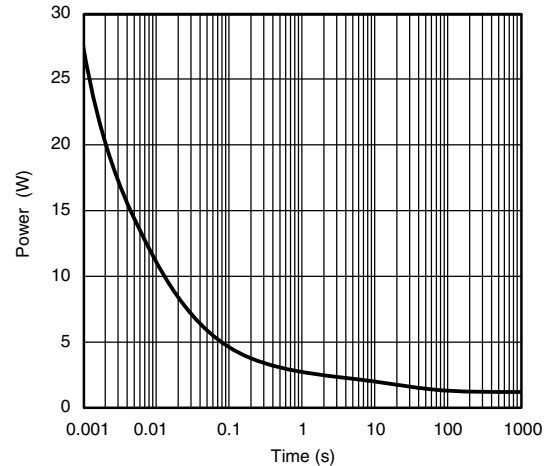
Source-Drain Diode Forward Voltage



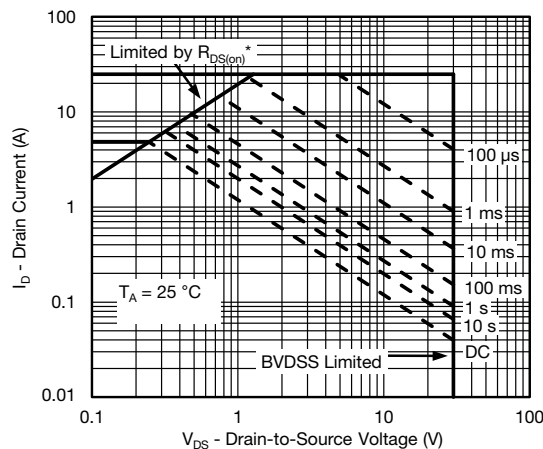
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



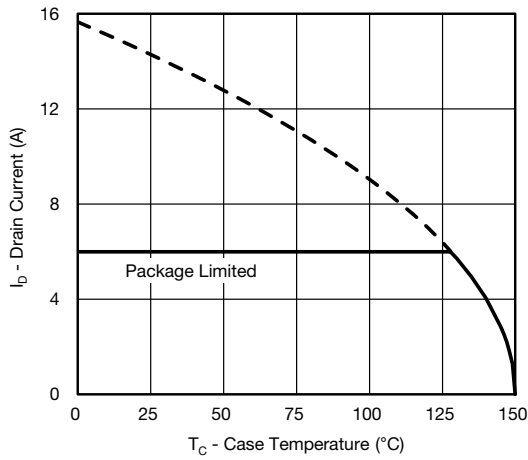
Single Pulse Power (Junction-to-Ambient)



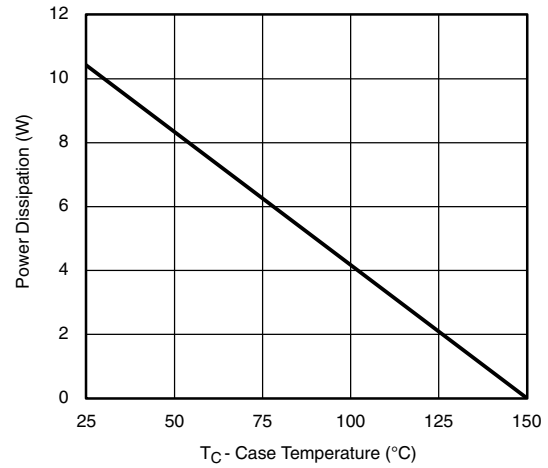
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating^a



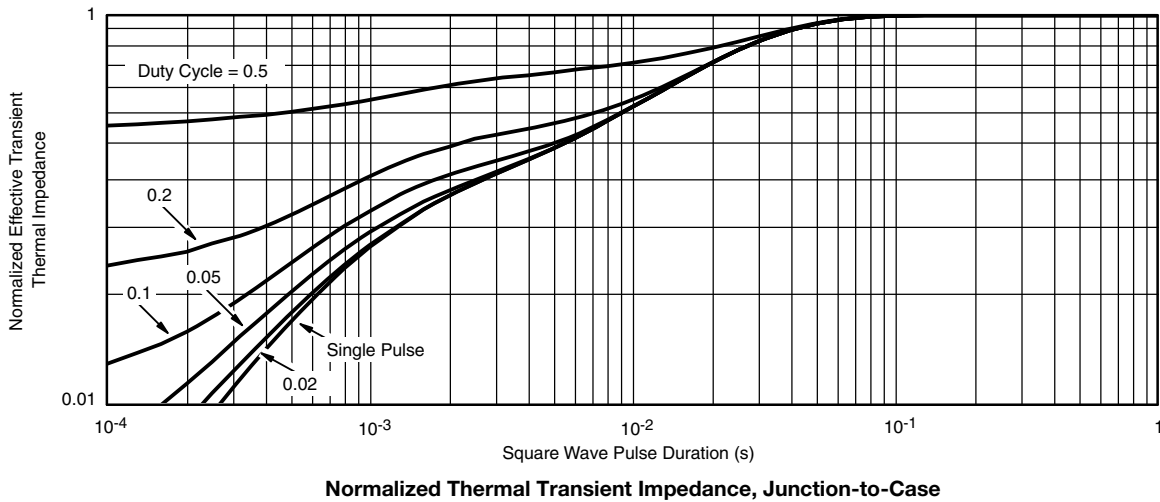
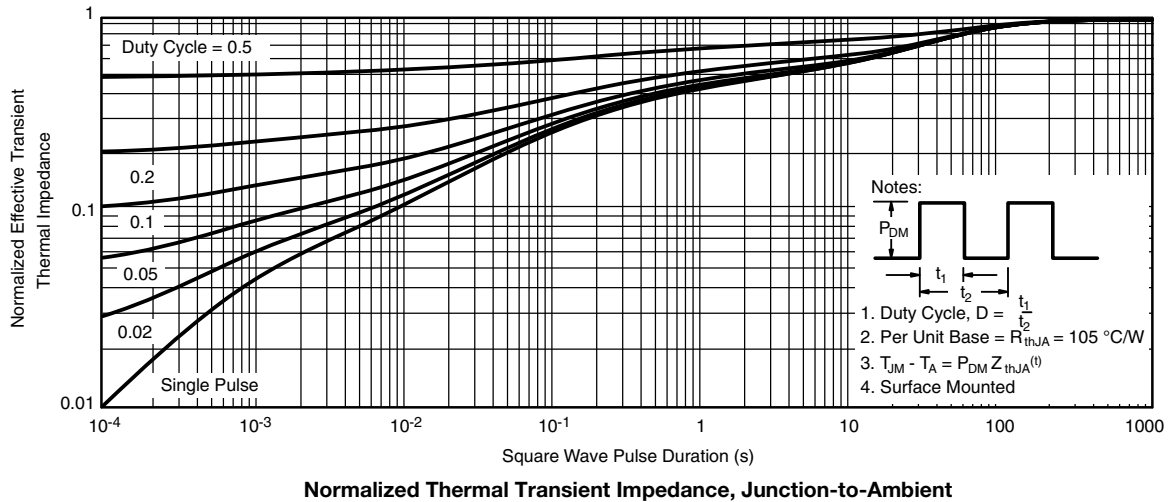
Power Derating

Note

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

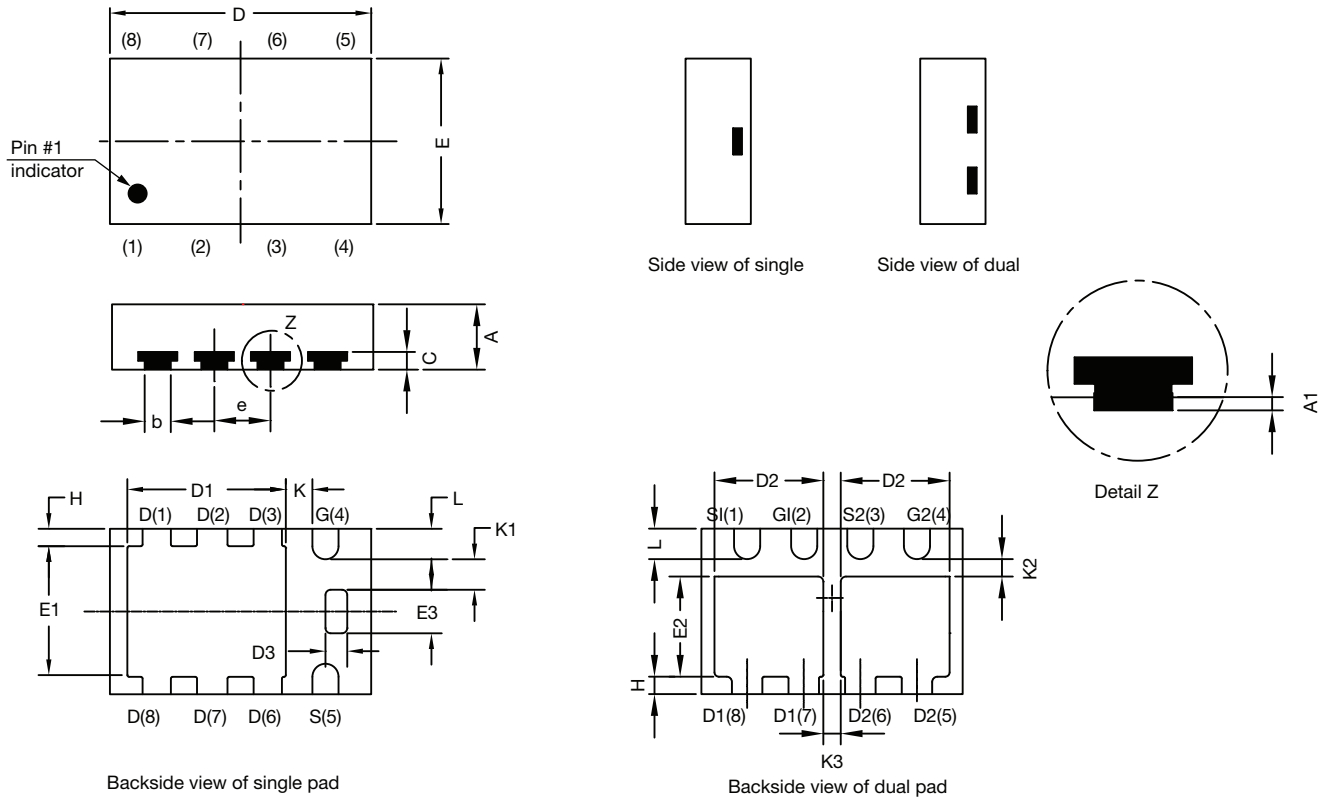


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62804.

PowerPAK[®] ChipFET[®] Case Outline

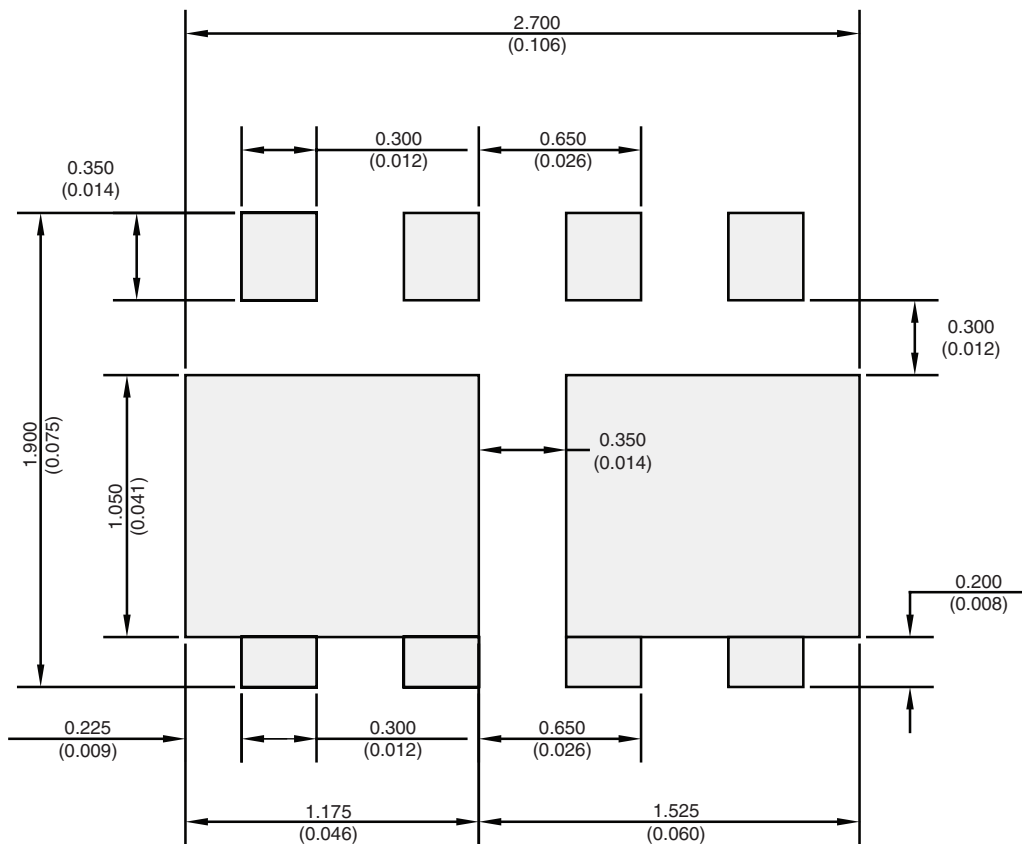


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14						
DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner



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