

P-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
- 200	1.61 at V _{GS} = - 10 V	- 0.95	8 nC
	1.65 at V _{GS} = - 6 V	- 0.93	

FEATURES

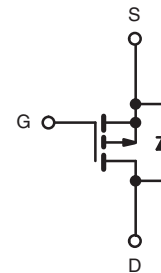
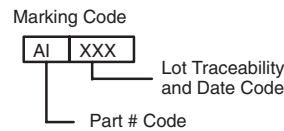
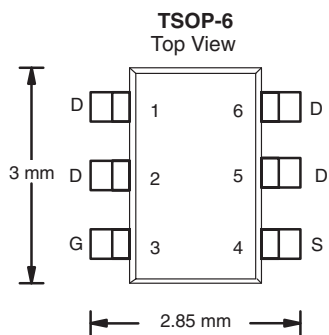
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Active Clamp Circuits in DC/DC Power Supplies



Ordering Information: Si3475DV-T1-E3 (Lead (Pb)-free)
Si3475DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 200	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 0.95 ^a	A
		T _C = 70 °C	- 0.77	
		T _A = 25 °C	- 0.75 ^{b,c}	
		T _A = 70 °C	- 0.59 ^{b,c}	
Pulsed Drain Current	I _{DM}	- 3	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		
		T _A = 25 °C	1.6 ^{b,c}	
Avalanche Current	I _{AS}	3	mJ	
Single-Pulse Avalanche Energy	E _{AS}	0.45		
Maximum Power Dissipation	P _D	T _C = 25 °C	3.2	W
		T _C = 70 °C	2.1	
		T _A = 25 °C	2 ^{b,c}	
		T _A = 70 °C	1.25 ^{b,c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	51	62.5	°C/W	
Maximum Junction-to-Foot	R _{thJF}	32	39		

Notes:

- T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- Maximum under Steady State conditions is 110 °C/W.

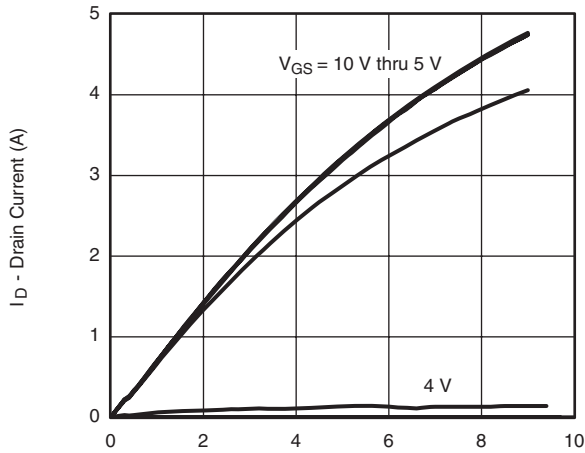
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-200			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\ \mu\text{A}$		-240		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		6.2			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2		-4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	-2			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -0.9\text{ A}$		1.34	1.61	Ω
		$V_{GS} = -6\text{ V}, I_D = -0.7\text{ A}$		1.37	1.65	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -0.9\text{ A}$		3.5		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		500		pF
Output Capacitance	C_{oss}		26			
Reverse Transfer Capacitance	C_{rss}		18			
Total Gate Charge	Q_g	$V_{DS} = -100\text{ V}, V_{GS} = -10\text{ V}, I_D = -1\text{ A}$		11.7	18	nC
				7.8	12	
Gate-Source Charge	Q_{gs}	$V_{DS} = -100\text{ V}, V_{GS} = -6\text{ V}, I_D = -1\text{ A}$		2		nC
Gate-Drain Charge	Q_{gd}			3.7		
Gate Resistance	R_g		$f = 1\text{ MHz}$		9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, R_L = 100\ \Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$		9	14	ns
Rise Time	t_r			11	18	
Turn-Off Delay Time	$t_{d(off)}$			28	42	
Fall Time	t_f			12	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, R_L = 100\ \Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -6\text{ V}, R_g = 1\ \Omega$		14	21	ns
Rise Time	t_r			29	44	
Turn-Off Delay Time	$t_{d(off)}$			23	35	
Fall Time	t_f			14	21	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			-0.95	A
Pulse Diode Forward Current	I_{SM}				-3	
Body Diode Voltage	V_{SD}	$I_S = -1\text{ A}, V_{GS} = 0\text{ V}$		-0.81	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		84	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}			235	350	nC
Reverse Recovery Fall Time	t_a			46		ns
Reverse Recovery Rise Time	t_b			38		

Notes:

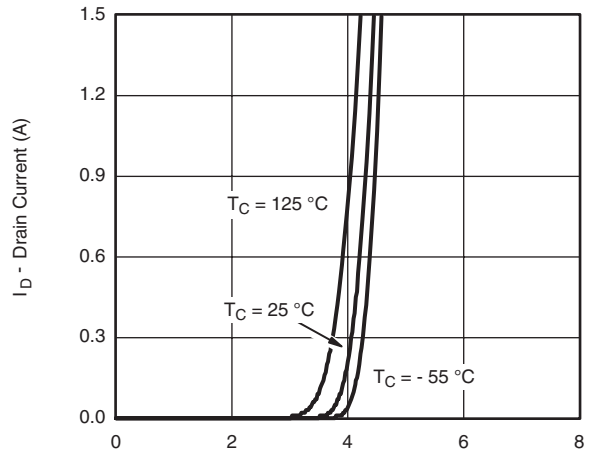
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

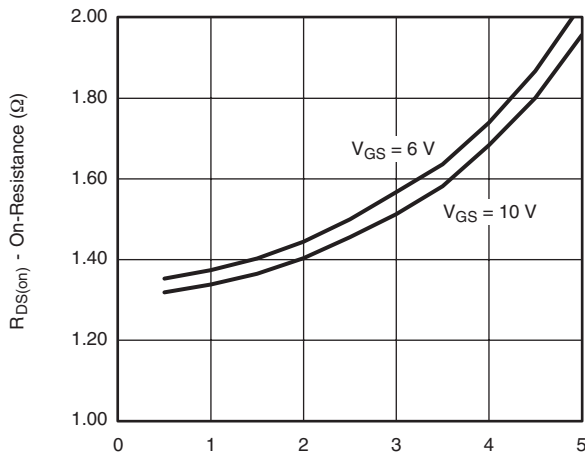
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



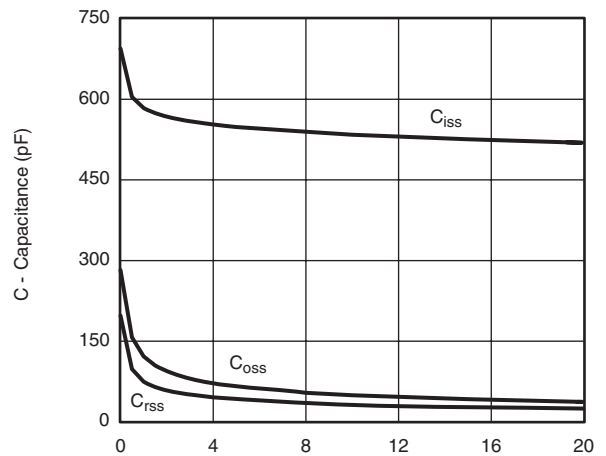
$V_{GS} = 10\text{ V thru } 5\text{ V}$
 V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



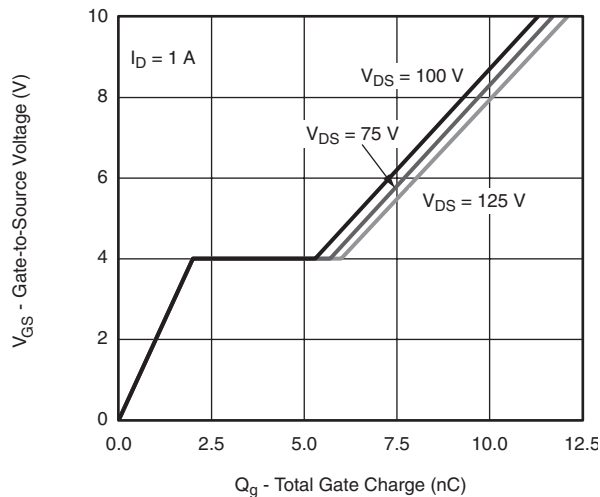
$T_C = 125^\circ\text{C}$
 $T_C = 25^\circ\text{C}$
 $T_C = -55^\circ\text{C}$
 V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



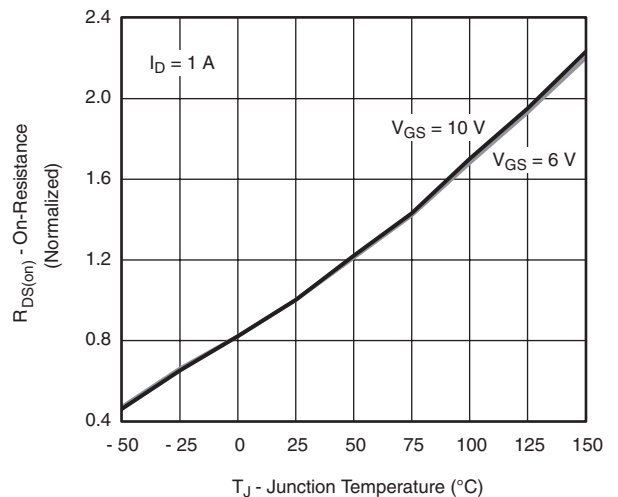
$V_{GS} = 6\text{ V}$
 $V_{GS} = 10\text{ V}$
 $R_{DS(on)}$ - On-Resistance (Ω)
 I_D - Drain Current (A)
On-Resistance vs. Drain Current



C_{iss}
 C_{oss}
 C_{rss}
 V_{DS} - Drain-to-Source Voltage (V)
Capacitance

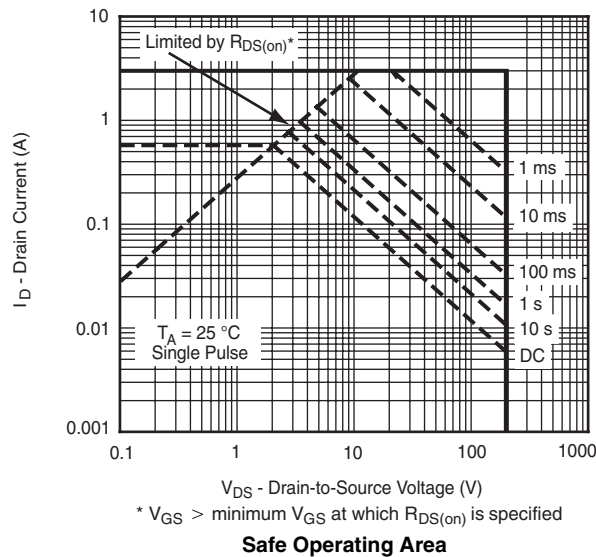
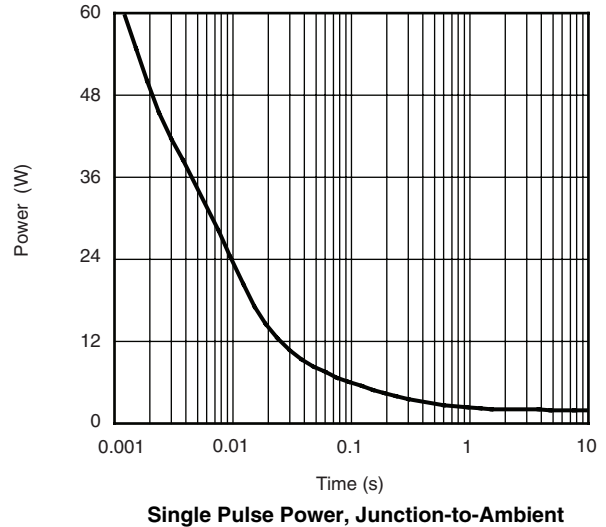
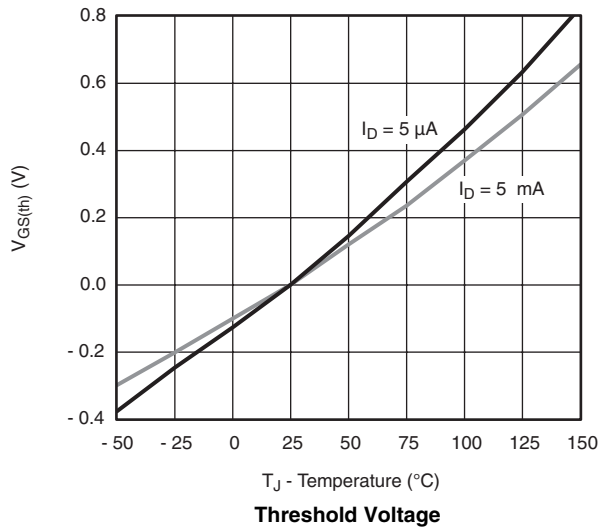
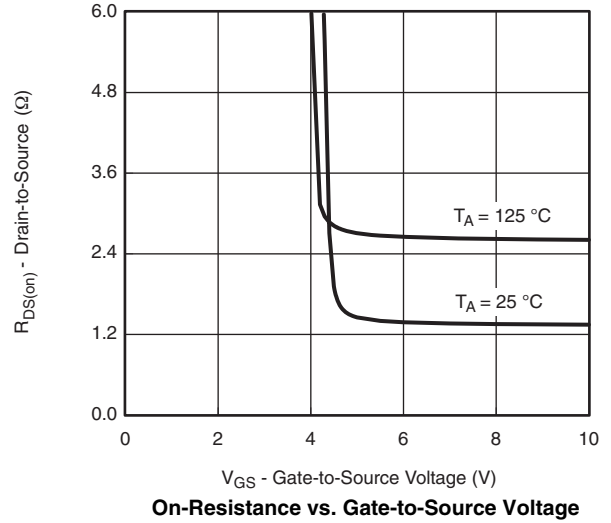
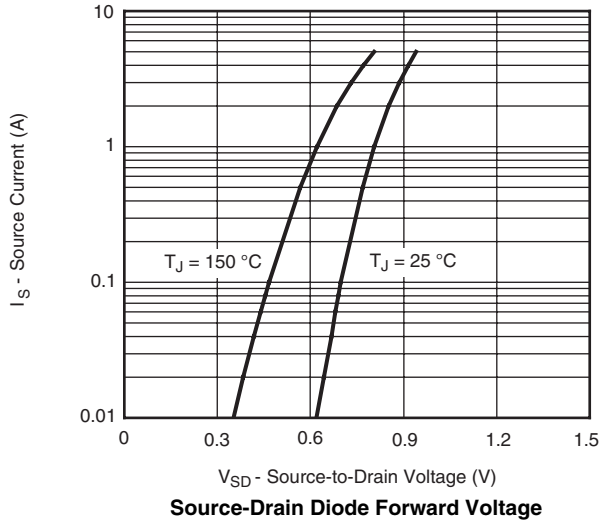


$I_D = 1\text{ A}$
 $V_{DS} = 100\text{ V}$
 $V_{DS} = 75\text{ V}$
 $V_{DS} = 125\text{ V}$
 Q_g - Total Gate Charge (nC)
Gate Charge

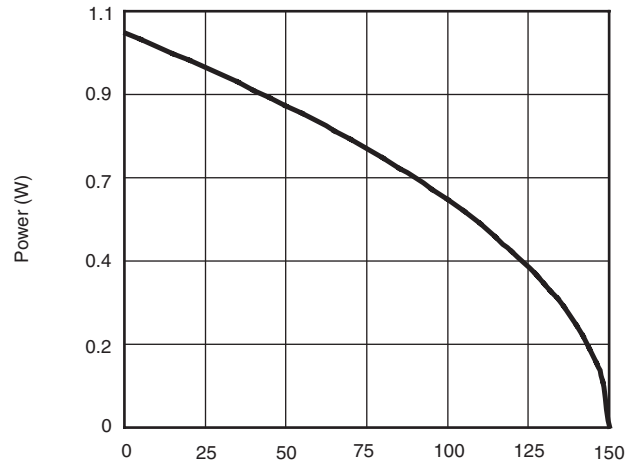


$I_D = 1\text{ A}$
 $V_{GS} = 10\text{ V}$
 $V_{GS} = 6\text{ V}$
 $R_{DS(on)}$ - On-Resistance (Normalized)
 T_J - Junction Temperature ($^\circ\text{C}$)
On-Resistance vs. Junction Temperature

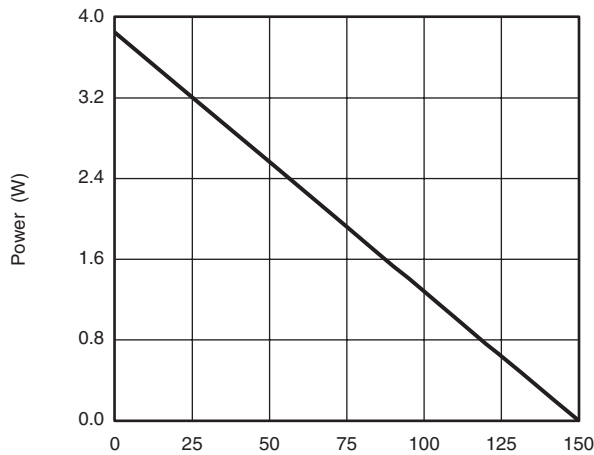
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



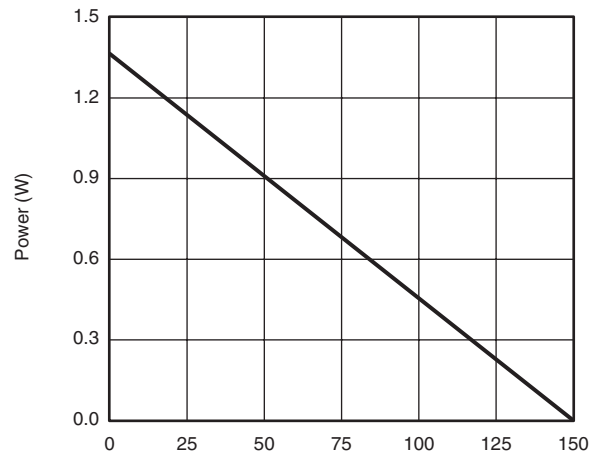
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)
Current Derating*



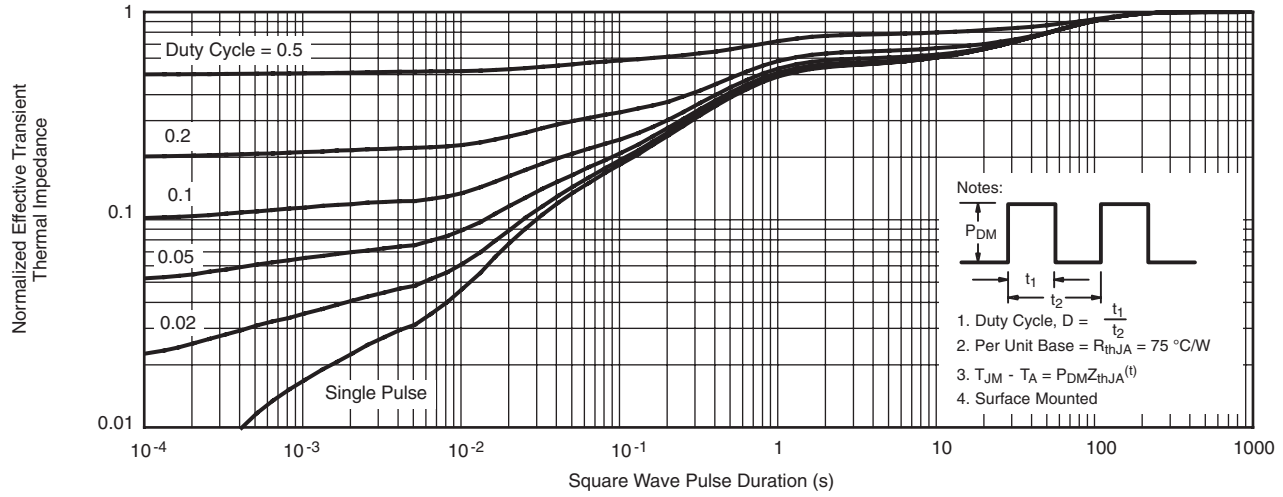
T_C - Case Temperature (°C)
Power, Junction-to-Foot



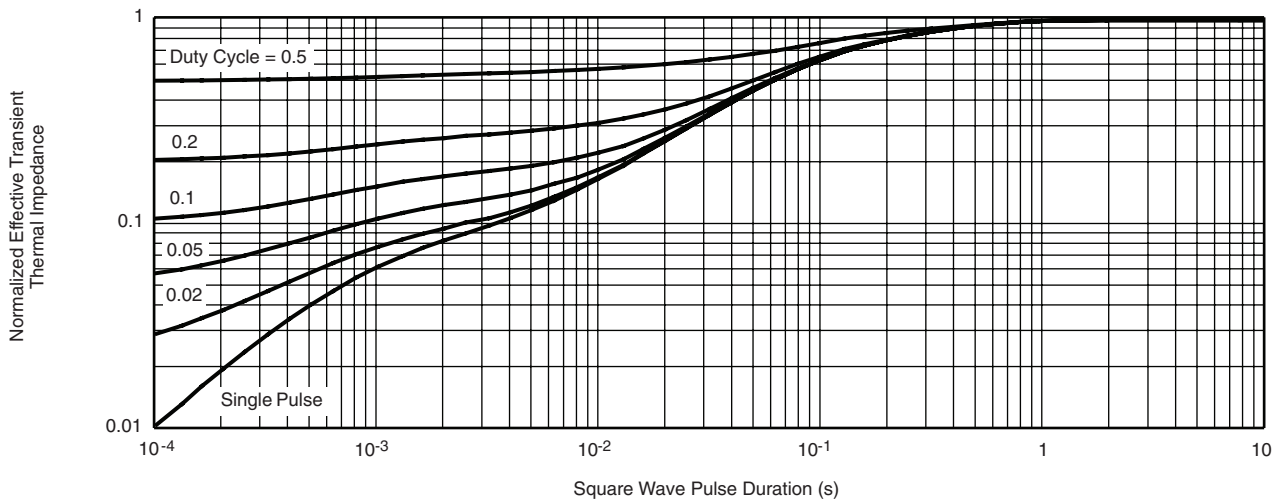
T_A - Ambient Temperature (°C)
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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