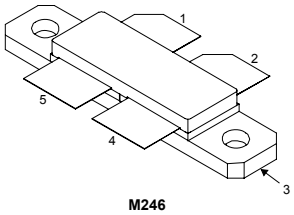
SD56060

Datasheet

60 W, 28 V, HF to 1 GHz RF power LDMOS transistor



M246

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
SD56060	860 MHz	28 V	60 W	16 dB	60

- Excellent thermal stability
- Common source configuration push-pull
- BeO-free package

Applications

- Ground/air communication
- ISM

Description

The SD56060 is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1 GHz. It is designed for high gain and broadband performance operating in common source mode at 28 V.

Product status link
SD56060

Product summary	
Order code	SD56060
Marking	SD56060
Package	M246
Packing	Box
Base/bulk quantity	20/60

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current	8	A
P_{TOT}	Total power dissipation at T_C = 70 °C	148	W
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.875	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	65			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
I_{GSS}	Gate-source leakage current	V_{GS} = 20 V, V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 28 V, I_D = 100 mA	2.8		5.0	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 3 A		1.3		V
G_{FS}	Transconductance	V_{DS} = 10 V, I_D = 3 A		1.8		S
C_{iss}	Common source input capacitance	V_{GS} = 0 V, V_{DD} = 28 V, f = 1 MHz		58		pF
C_{rss}	Common source feedback capacitance			34		pF
C_{oss}	Common source output capacitance			2.7		pF

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	V_{DD} = 28 V, I_{DQ} = 100 mA, f = 860 MHz	60		-	W
G_{PS}	Power gain	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{OUT} = 60 W, f = 860 MHz	14	16	-	dB
η_D	Drain efficiency		50	60	-	%
IMD	Intermodulation distorsion	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{OUT} = 60 W, PEP(1)		-28	-	dB_C
VSWR	Load mismatch	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{OUT} = 60 W, f = 860 MHz, all phases	5:1		-	

1. *PEP is: f1 = 860 MHz and f2 = 860.1 MHz.*

3 Typical performances

Figure 1. Capacitance vs drain voltage (per section)

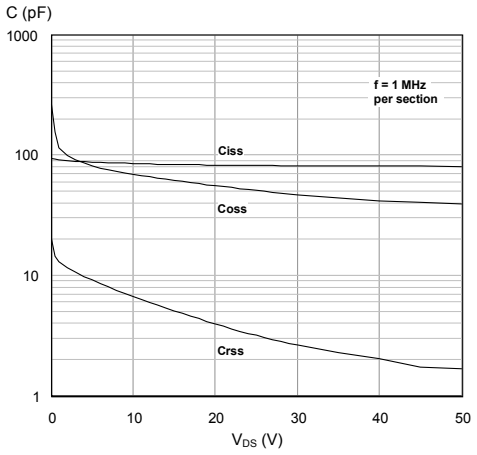


Figure 2. Gate-source voltage vs case temperature

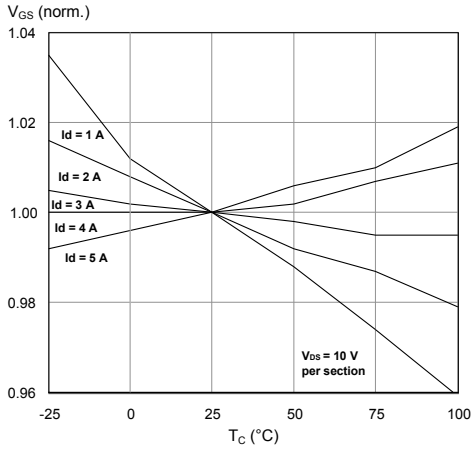


Figure 3. Drain current vs gate voltage

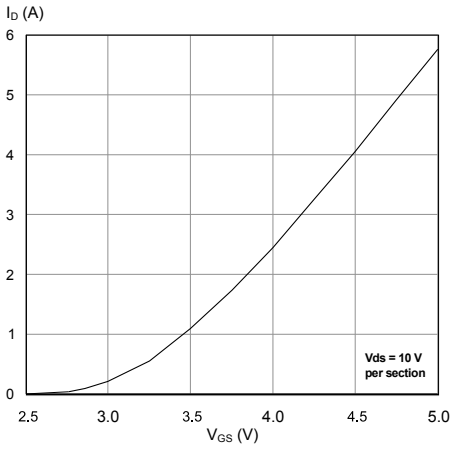


Figure 4. Output power vs input power

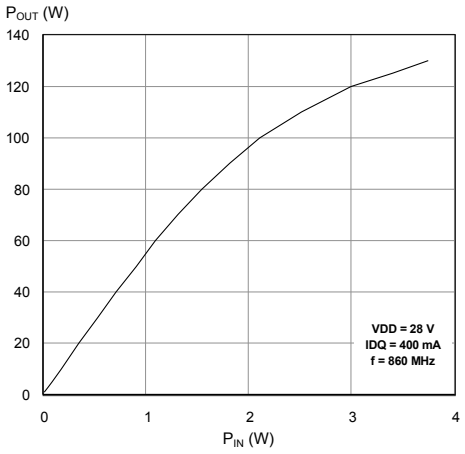


Figure 5. Power gain vs input power

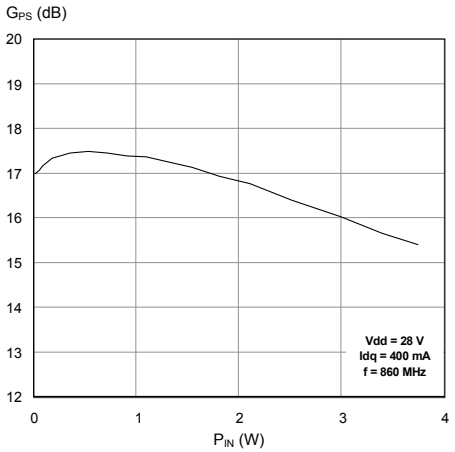


Figure 6. Efficiency vs output power

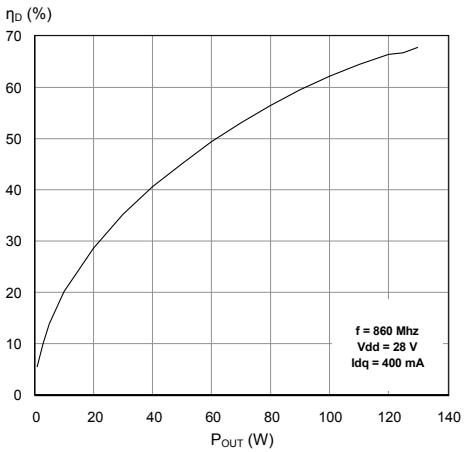


Figure 7. Power gain vs output power

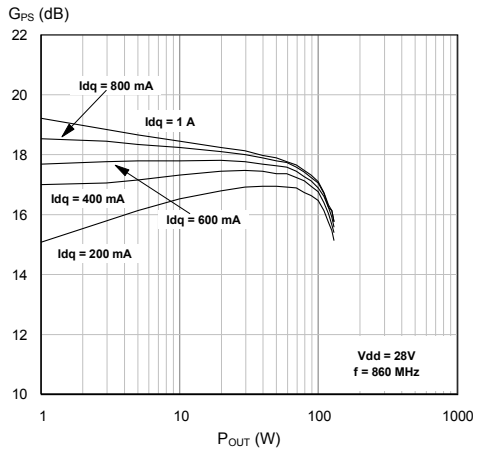


Figure 8. Intermodulation distortion vs output power

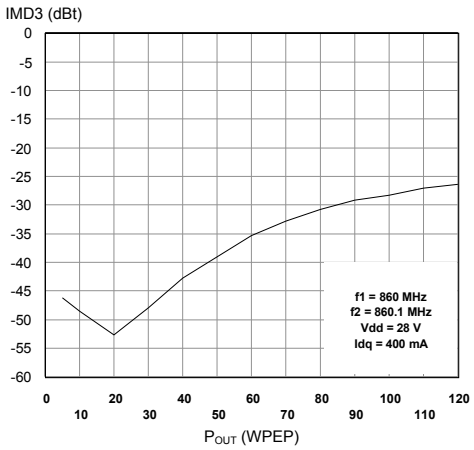


Figure 9. Output power vs drain voltage

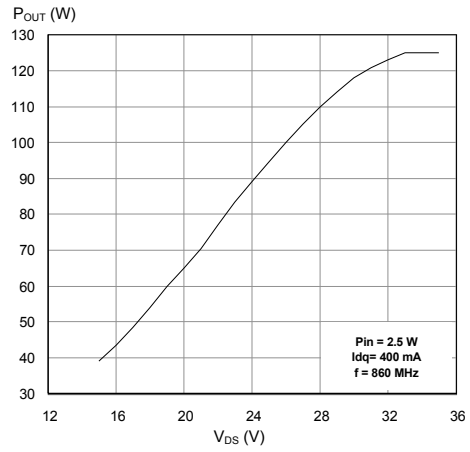


Figure 10. Output power vs bias current

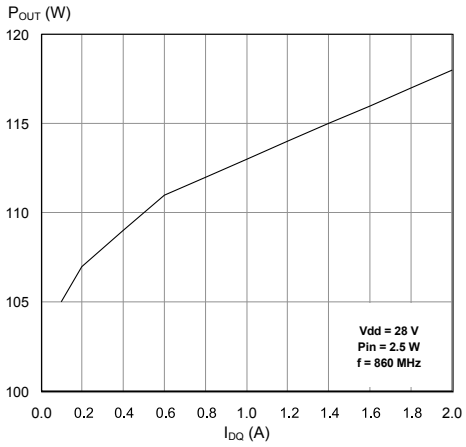
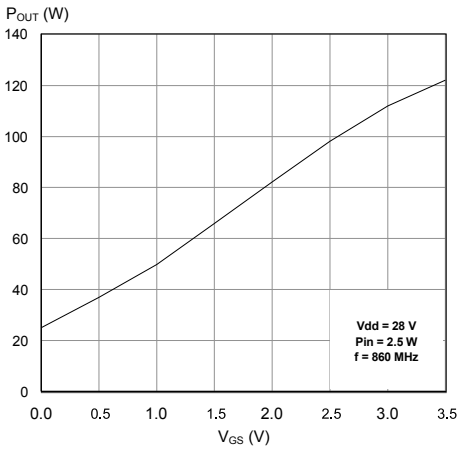
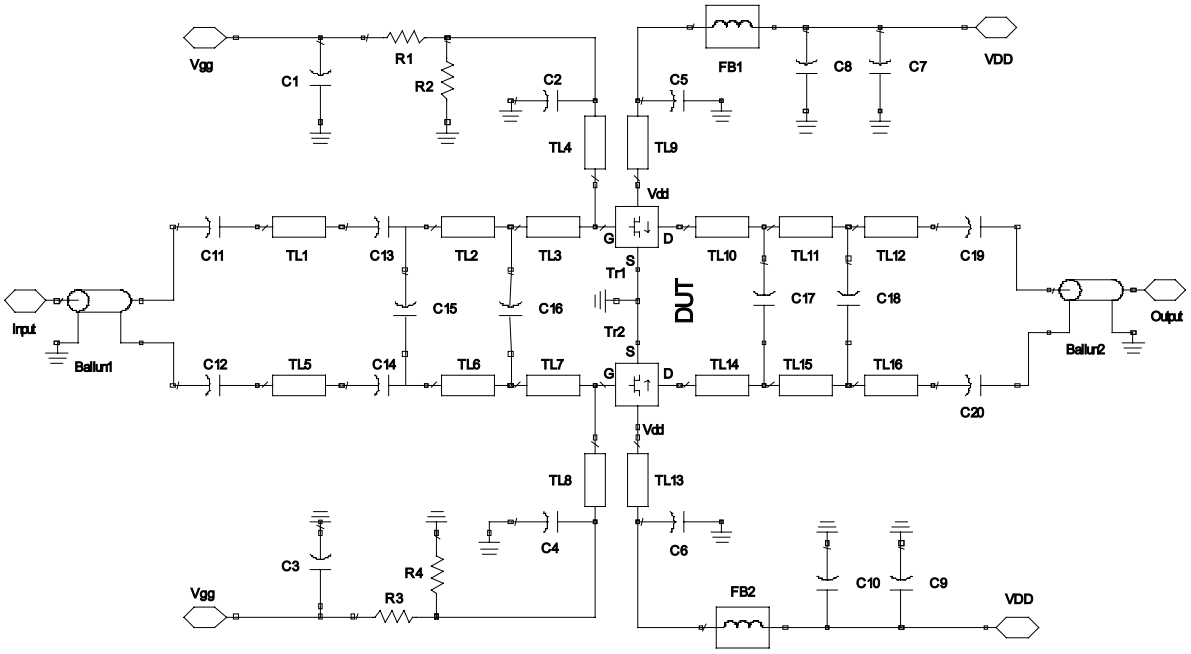


Figure 11. Output power vs gate-source voltage



4 Test circuits

Figure 12. **Test circuit schematic (f = 860 MHz)**



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Note: 1. *Dimensions at component symbols are reference for component placement.*

2. *Gap between ground and transmission line = 0.056 in [1.42 mm] +0.002 in [0.05 mm] -0.000 in [0.00 mm] typ.*

Table 5. Components list

Component	Q.ty	Part number	Vendor	Description
R1, R3	2	CR1206-8W-130JB	VENKEL	13 Ω, 1/8 W surface mount chip resistor
R2, R4	2	CR1206-8W-122JB	VENKEL	1.2 kΩ, 1/8 W surface mount chip resistor
R5, R6	2	CR1206-8W-250JB	VENKEL	25 Ω, 1/8 W surface mount chip resistor
B1, B2	2	2743021447	FAIR-RITE CORP	Surface mount EMI shield bead
C1, C3, C7, C9	4			100 µF, 63 V electrolytic capacitor
C2, C4, C5, C6	4	ATC100B910XXXX	ATC	91 pF chip capacitor
C8, C10	2	C1812X7R501-104KNE		0.1 F 500 V surface mount ceramic chip capacitor
C11, C12	2	ATC100B620XXXX	ATC	62 pF chip capacitor
C13, C14	2	ATC100B151XXXX	ATC	150 pF chip capacitor
C15	1	ATC100B110XXXX	ATC	5.1 pF chip capacitor
C16	1	ATC100B7R5XXXX	ATC	7.5 pF chip capacitor
C17	1	ATC100B1R1XXXX	ATC	1.1 pF chip capacitor
C18	1	27291PC	JOHANSON	0.8-8 pF giga trim variable capacitor
C19, C20	2	ATC100B101XXXX	ATC	100 pF chip capacitor
TL1, TL5				L= 0.250 in [6.35 mm], W=0.214 in [5.44 mm]
TL2, TL6				L= 0.182 in [4.62 mm], W=0.284 in [7.21 mm]
TL3, TL7				L= 0.318 in [8.08 mm], W=0.284 in [7.21 mm]
TL4, TL8, TL9, TL13				L= 2.37 in [60.19 mm], W=0.082 in [2.08 mm]
TL10, TL14				L= 0.314 in [7.97 mm], W=0.230 in [5.84 mm]
TL11, TL15				L= 0.460 in [11.68 mm], W=0.230 in [5.84 mm]
TL12, TL16				L= 0.280 in [7.11 mm], W=0.230 in [5.84 mm]
Board 3x5	1		Rogers Corp	εr = 2.55, t (copper layer thickness) = 0.0026 in [0.066 mm], h (PCB thickness) = 0.030 in [0.762 mm]

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 M246 package information

Figure 13. M246 package outline

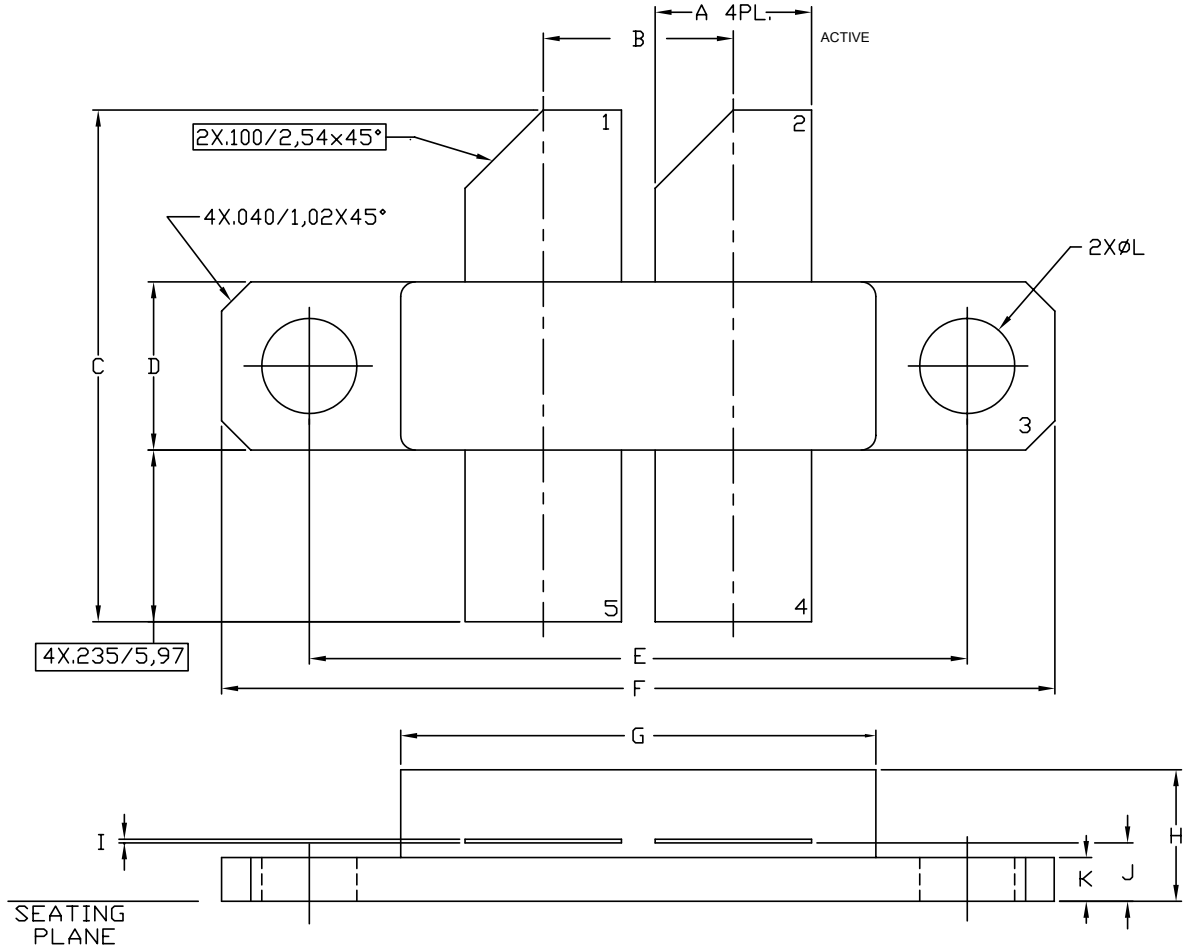

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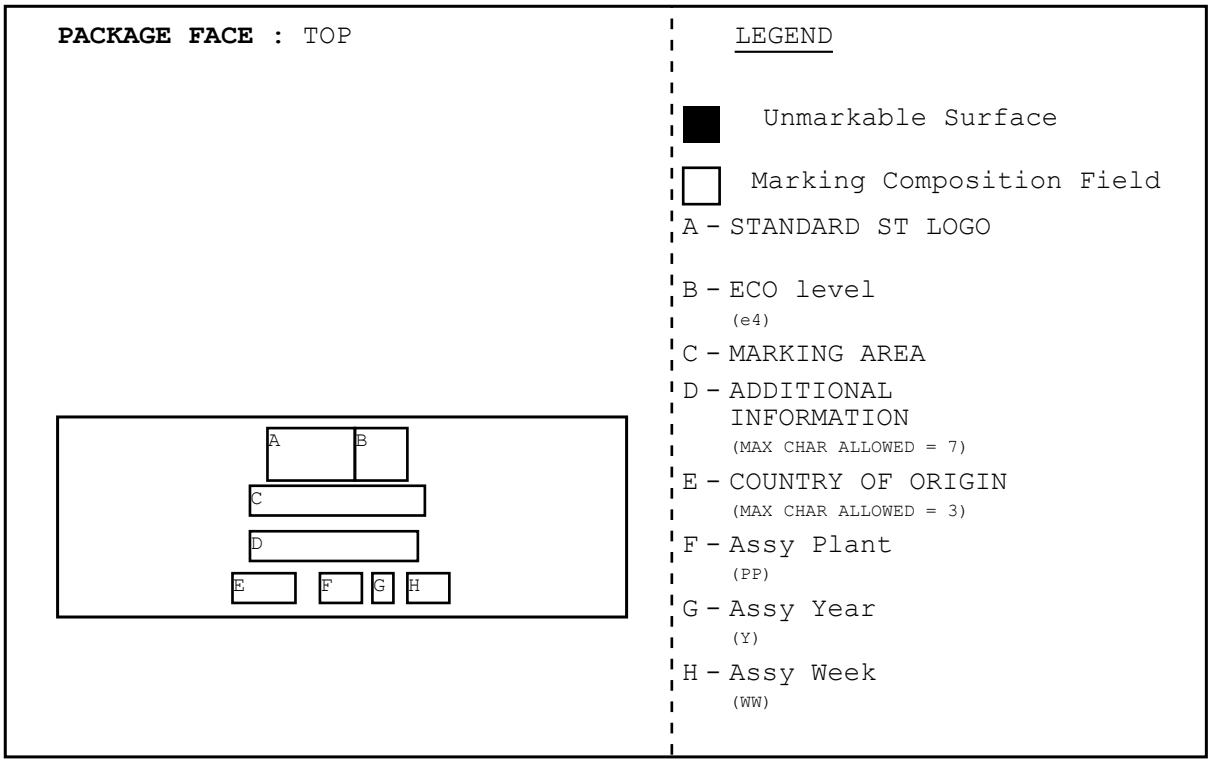
Table 6. **M246 mechanical data**

Symbol	Milimeters		
	Min.	Typ.	Max.
A	5.33		5.59
B	6.48		6.73
C	17.27		18.29
D	5.72		5.97
E		22.86	
F	28.83		29.08
G	16.26		16.76
H	4.19		5.08
I	0.08		0.15
J	1.83		2.24
K	1.40		1.65
L	3.18		3.43

5.2 Marking information

Figure 14. **Marking composition**



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Revision history

Table 7. **Document revision history**

Date	Version	Changes
15-Jun-2015	1	First release.
22-Dec-2021	2	Updated title, Features, Description, Device summary and added Applications on cover page. Updated Table 3. Static (per side). Removed *Impedances* chapter. Updated Section 5 Package information and added Section 5.2 Marking information. Minor text changes.

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