Signal Chain Power
ADP5070 Dual Output Boost/Inverter

DESCRIPTION

Demonstration circuit SCP-ADP5070-EVALZ is a dual output DC-DC converter designed to create a dual polarity regulated voltage for powering several signal chains. The positive regulator provides 15V/1A of output while the negative regulator delivers –15V/300mA.

Like all boards in the Signal Chain Power series, this board is designed to be easily plugged into other SCP boards to form a complete signal chain power system, enabling fast evaluation of low power signal chains. To evaluate this board, some universal SCP hardware is required, namely:

SCP-INPUT-EVALZ
SCP-OUTPUT-EVALZ
SCP-1X5BKOUT-EVALZ
SCP-THRUBRD-EVALZ
SCP-FILTER-EVALZ
SCP-1X2BKOUT-EVALZ
SCP-5X1-EVALZ

To properly evaluate SCP series demo boards, you will need the SCP Configurator companion software. SCP Configurator can help you choose the right board and topology for your design.

Note that this Demo Manual does not cover details important to the operation and configuration regarding the ADP5070. Please refer to the ADP5070 datasheet for a complete description of the part.

Design files for this circuit board are available.

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Table 1. Performance Summary

SYMBOL	PARAMETER	NOTES	MIN	TYP	MAX	UNITS
$V_{IN(MAX)}$	Max Input Voltage				15	V
$V_{OUT(MAX)}$	Max Output Voltage	Positive V_{OUT}			39	V
		Negative V_{OUT}			–39	
$I_{OUT(MAX)}$	Max Output Current	Positive V_{OUT}			1	A
		Negative V_{OUT}			0.6	

BOARD IMAGE

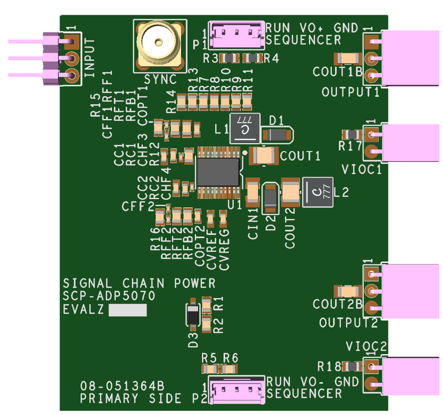


Figure 1. SCP-ADP5070-EVALZ Board

QUICK START PROCEDURE

Demonstration circuit SCP-ADP5070-EVALZ is easy to set up to evaluate the performance of any SCP hardware configuration.

1. The SCP-ADP5070-EVALZ ships with default output voltages of 15V and –15V, respectively. To change the output voltage, see "Configuration Settings" section, and modify the board accordingly. Be sure to check for open connections or solder shorts after making any modifications.
2. Connect the SCP-INPUT-EVALZ and SCP-OUTPUT-EVALZ boards to the SCP-ADP5070-EVALZ (refer to Figure 2) and connect the input board to a voltage source, V_{SOURCE}. Connect the output board to a voltmeter or dynamic load. Slowly raise the input voltage until the SCP-ADP5070-EVALZ powers up into regulation and sweep V_{SOURCE} through the desired range of operation.

   NOTE: Make sure that the input voltage is always within spec. If using a dynamic load to measure output voltage, make sure the load is initially set to zero.
3. Check for proper output voltages. The output should be regulated at the programmed value (±5%).
4. Once the proper output voltage is established, power off V_{SOURCE} and similarly test other boards in the SCP system until all elements have been individually verified prior to assembling into the final circuit configuration.

   NOTE: When measuring the input or output voltage ripple, use the optional SMA connector locations available on the input, output, 1 × 5, 1 × 2, and 5 × 1 breakout boards. Avoid using the test point connections with long scope leads.

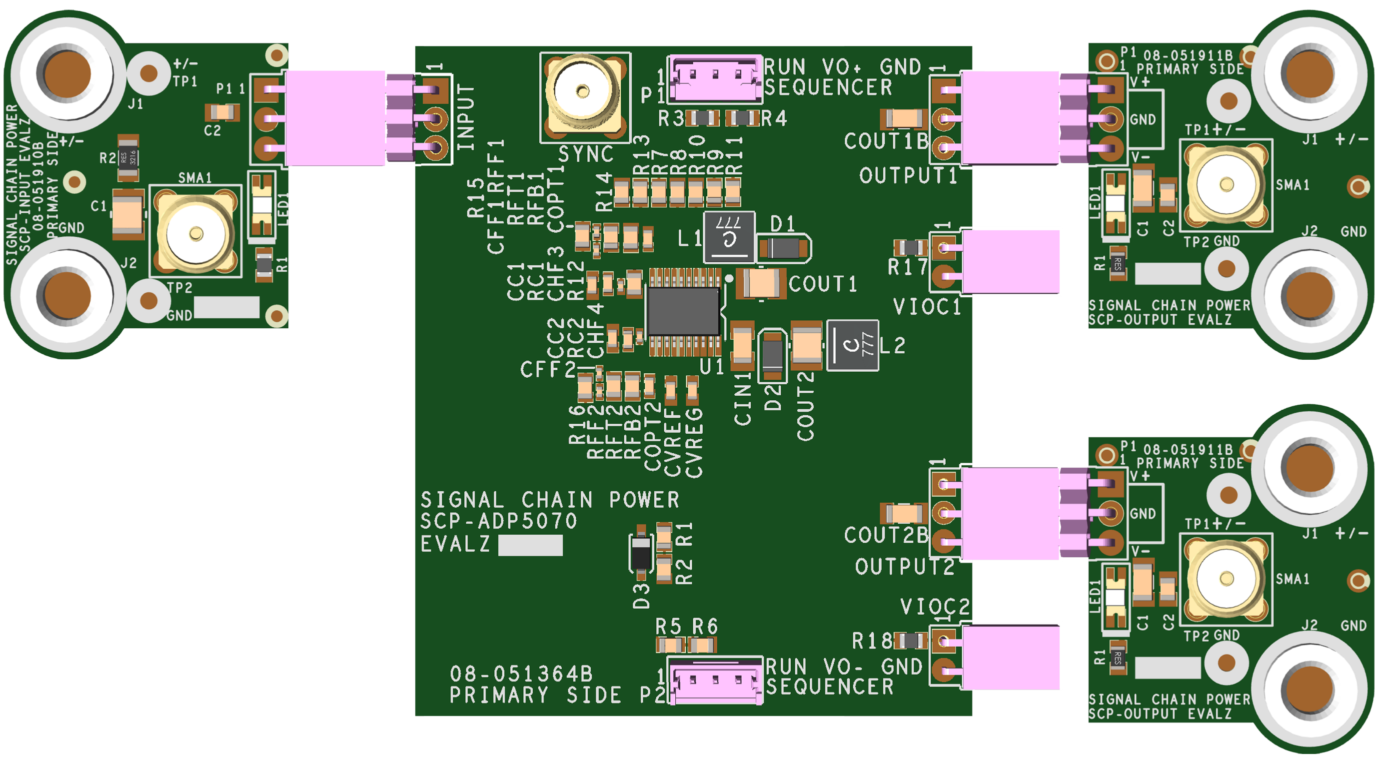


Figure 2. Proper Measurement Equipment Setup (Use SMA connectors for Measuring Input or Output Ripple)

CONFIGURATION SETTINGS

Demonstration circuit SCP-ADP5070-EVALZ is a dual output DC-DC converter designed to create a dual polarity regulated voltage for powering several signal chains. The positive regulator provides 15V/1A of output while the negative regulator delivers –15V/300mA.

Each output of the SCP-ADP5070-EVALZ is resistor-programmable from |5V| to |39V|. The board can be also configured to drive VIOC-capable linear regulators.

OUTPUT VOLTAGE PROGRAMMING

$$+V_{OUT} = 0.8V\left(1+\frac{R_{FT1}}{R_{FB1}}\right)$$

$$-V_{OUT} = 0.8V - \frac{R_{FT2}}{R_{FB2}}(1.6V - 0.8V)$$

Table 2. Resistor Selection Guide for Common Output Voltages

$\|V_{OUT}\|$ (V)	R_{FT1} (Ω)	R_{FB1} (Ω)	R_{FT2} (Ω)	R_{FB2} (Ω)
5.0	105k	20.0k	115k	15.8k
5.5	107k	18.2k	226k	28.7k
6.0	71.5k	11.0k	113k	13.3k
6.5	97.6k	13.7k	93.1k	10.2k
7.0	78.7k	10.2k	392k	40.2k
7.5	115k	13.7k	169k	16.2k
8.0	102k	11.3k	110k	10.0k
8.5	162k	16.9k	137k	11.8k
9.0	205k	20.0k	162k	13.3k
9.5	150k	13.7k	137k	10.7k
10.0	115k	10.0k	137k	10.2k
11.0	255k	20.0k	174k	11.8k
12.0	140k	10.0k	115k	7.15k
13.0	210k	13.7k	280k	16.2k
14.0	165k	10.0k	255k	13.7k
15.0	442k	24.9k	232k	11.8k
16.0	215k	11.3k	210k	10.0k
17.0	232k	11.5k	255k	11.5k
18.0	215k	10.0k	267k	11.3k
19.0	232k	10.2k	280k	11.3k
20.0	255k	10.7k	294k	11.3k
25.0	357k	11.8k	442k	13.7k
30.0	365k	10.0k	412k	10.7k
35.0	590k	13.7k	511k	11.5k
39.0	487k	10.2k	200k	40.2k

ENABLE PIN CONFIGURATION

The EN1 and EN2 pins are tied to the optional SCP Run/Sequence headers P1 and P2. To create a harness for this function, use Molex part 0510650300 with crimp pin 50212-8000.

The pins allow for a high, low or precision adjustment for undervoltage lockout (UVLO) if desired. To set both channels high with pinstrapping (default), use 0Ω for R3 and R5. To use an active run signal, use a 100kΩ resistor for either pull-up or pull-down resistors R3, R4, R5 and R6 and use the drive signal from connectors P1 and P2. Table 6 contains additional startup sequence options.

If precision UVLO operation is desired, program the enable pins such that:

$$V_{UVLO\_1} = 2.80V\left(1+\frac{R3}{R4}\right)$$

$$V_{UVLO\_2} = 2.80V\left(1+\frac{R5}{R6}\right)$$

With 100kΩ internal R_{HYST}, size R4 and R6 such that:

$$V_{UVLO\_1} = 2.55V\left(1+\frac{R3}{R4}\right)$$

$$V_{UVLO\_2} = 2.55V\left(1+\frac{R5}{R6}\right)$$

VOLTAGE INPUT-TO-OUTPUT CONTROL (VIOC) IMPLEMENTATION

To implement the VIOC function for both regulators, set R17 and R18 to 0Ω, respectively. Refer to the "Configuration Settings" section in the Demo Manual for the low-dropout (LDO) linear regulator board and use the following configuration for this board.

Table 3. VIOC Cross-Reference Designators

VIOC SETTING REFERENCES	R_{BOT}	R_{TOP}	R_{MAX}
$+V_{OUT}$ Reference Designators	R_{FB1}	R_{FT1}	R15
$–V_{OUT}$ Reference Designators	R_{FB2}	R_{FT2}	R16

Positive VIOC Equations

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC} = 0.8V\left(\frac{R_{BOT} + R_{TOP}}{R_{BOT}}\right)$$

$$V_{(MAX)LDOIN} = 0.8V\left(\frac{R_{BOT} + R_{TOP} + R_{MAX}}{R_{BOT}}\right) + I_{SINK}R_{MAX}$$

I_{SINK} is the current through R_{MAX}, typically 15µA, so R_{BOT} should be sized such that the divider current runs a minimum of 100µA to minimize the I_{SINK} error term.

Negative VIOC Equations

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC} = 0.8V - \left(\frac{R_{BOT} + R_{TOP}}{R_{BOT}}\right)(1.6V - 0.8V)$$

$$V_{(MAX)LDOIN} =$$

$$0.8V - \left(\frac{R_{BOT} + R_{TOP} + R_{MAX}}{R_{BOT}}\right)(1.6V - 0.8V) + I_{SINK}R_{MAX}$$

Because the V_{LDOIN} term is simply the sum of the final output voltage after the LDO and the difference the ADP5070 is adding on top, it can be helpful to take the desired final output voltage, add (or subtract for negative voltages) 1.0V, and then look up that voltage-resistor combination from Table 2.

R_{MAX} can then be obtained by figuring out the difference between the maximum and nominal output voltage of the ADP5070, divided by the current through the internal R_{BOT} resistor, which is $0.8V/R_{BOT}$.

FREQUENCY, SYNC AND SLEW RATE CONFIGURATION

Table 4. Slew Rate Configuration Settings

RATE	EFFICIENCY	R13	R14
Fast	Higher	Open	Open
Nominal	Nominal	0Ω	Open
Slow	Lower	Open	0Ω

Table 5. Frequency/Sync Configuration

RATE	R9	R10	R11
2.4MHz	0Ω	Open	Open
1.2MHz	Open	0Ω	Open
Clock Sync	Open	Open	0Ω

Table 6. Startup Sequence Configuration

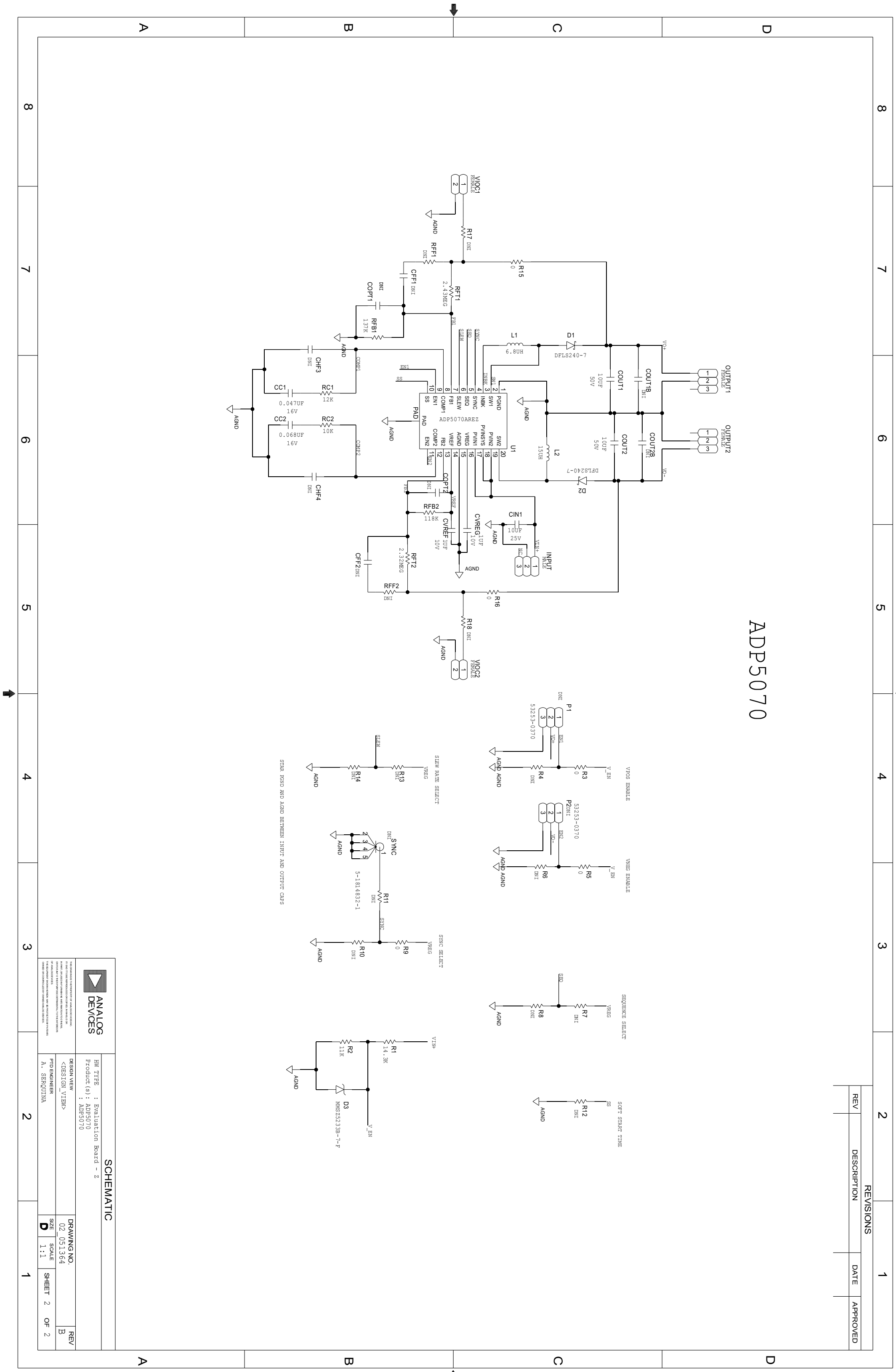
MODE	R7	R8	EN1	EN2
Manual	Open	Open	High	High
Tracking	0Ω	Open	High	_↑
Seq 1–2	Open	0Ω	_↑	Low
Seq 2–1	Open	0Ω	Low	_↑

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	PCB	PCB	ANALOG DEVICES 08_051364b
2	1	CC1	CAP CER 47nF 16V X7R 0603	YAGEO CC0603KRX7R7BB473
3	1	CC2	CAP CER 68nF 16V X7R 0603	AVX 0603YC683KAZ2A
4	4	C_{FF1}, C_{FF2}, C_{HF3}, C_{HF4}	RES TBD 0402 (Note 1)	N/A
5	1	C_{IN1}	CAP 10uF 25V CER X7R 1206	TAIYO YUDEN TMK316B7106KL-TD
6	2	C_{OPT1}, C_{OPT2}	CAP TBD CER 0603 (Note 1)	TBD
7	2	C_{OUT1}, C_{OUT2}	CAP CER 10UF 50V X5R 1206	SAMSUNG CL31A106MBHNNNE
8	2	C_{OUT1B}, C_{OUT2B}	CAP TBD CER 1206 (Note 1)	TBD
9	2	C_{VREF}, C_{VREG}	CAP 1uF 10V CER X7R 0603	SAMSUNG CL10B105KP8NNNC
10	2	D1, D2	DIODE SCHOTTKY BARRIER RECTIFIER	DIODES INC DFLS240-7
11	1	D3	DIODE ZENER, 6.0V, 500mW	DIODES INC MMSZ5233B-7-F
12	1	INPUT	CONN MALE 3POS 2.54MM PITCH R/A	SULLINS PBC03SBAN
13	1	L1	6.8uH 3.9A 74.1mOHM INDUCTOR	COILCRAFT XAL4030-682MEC
14	1	L2	15uH 2.8A 120mOHM INDUCTOR	COILCRAFT XAL4040-153MEB
15	2	OUTPUT1, OUTPUT2	CONN FEMALE 3POS 2.54MM PITCH R/A	SULLINS PPPC031LGBN-RC
16	2	P1, P2	CONN-PCB 3POS HEADER WIRE TO BRD ASSY STRAIGHT 2MM PITCH (Note 1)	MOLEX 53253-0370
17	1	R1	RES 14.3k 1% THICK FILM 0805	PANASONIC ERJ-6ENF1432V
18	11	R4, R6, R7, R8, R10, R11, R12, R13, R14, R17, R18	RES THICK FILM 0805 (Note 1)	N/A
19	5	R3, R5, R9, R15, R16	RES 0.0 5% STANDARD THICK FILM CHIP	VISHAY CRCW08050000Z0EA
20	1	R2	RES 11.0k 1% THICK FILM 0805	PANASONIC ERJ-6ENF1102V
21	1	R_{C1}	RES 12.0k 1% THICK FILM 0603	PANASONIC ERJ-3EKF1202V
22	1	R_{C2}	RES 10.0k 1% THICK FILM 0603	PANASONIC ERJ-3EKF1002V
23	1	R_{FB1}	RES 137k 1% THICK FILM 0805	PANASONIC ERJ-6ENF1373V
24	1	R_{FB2}	RES 118k 1% THICK FILM 0805	PANASONIC ERJ-6ENF1183V
25	2	R_{FF1}, R_{FF2}	RES TBD THICK FILM 0402 (Note 1)	TBD
26	1	R_{FT1}	RES 2.43M 1% THICK FILM 0805	YAGEO RC0805FR-072M43L
27	1	R_{FT2}	RES 2.32M 1% THICK FILM 0805	YAGEO RC0805FR-072M32L
28	1	SYNC	CONN-PCB STRAIGHT SMA PCB DIE CAST (Note 1)	TE CONNECTIVITY 5-1814832-1
29	1	U1	IC-ADI 1A/0.6A, DC TO DC SWITCHING REGULATOR WITH INDEPENDENT POSITIVE AND NEGATIVE OUTPUTS	ANALOG DEVICES ADP5070AREZ
30	2	VIOC1, VIOC2	CONN FEMALE 2POS 2.54MM PITCH R/A	SULLINS PPPC021LGBN-RC

Note 1. These items are not stuffed (DNI).

SCHEMATIC DIAGRAM



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