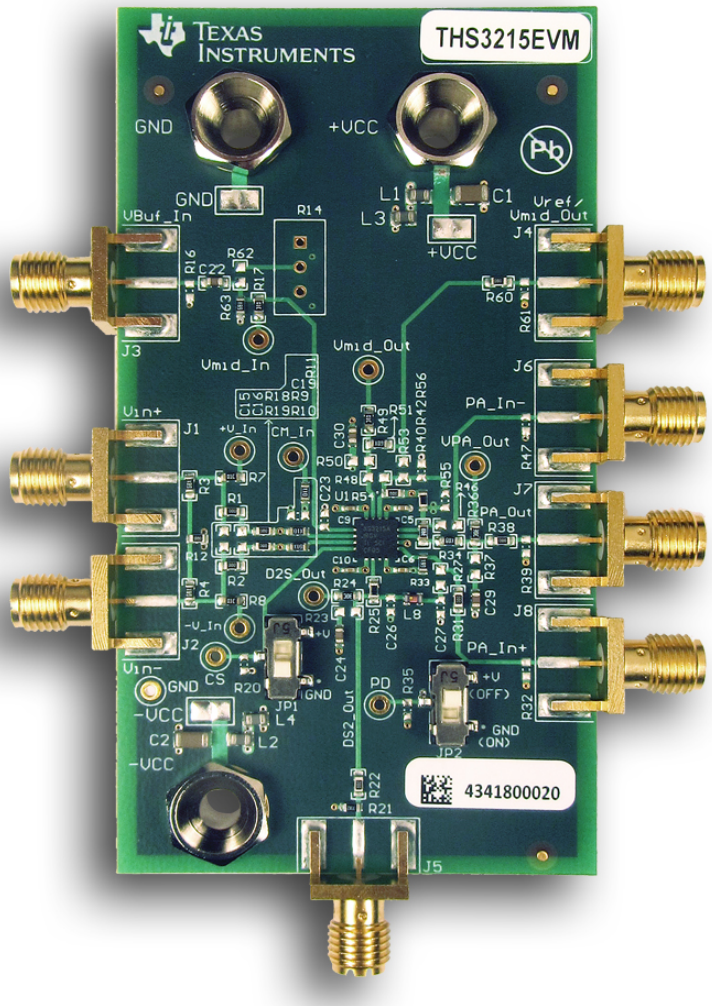
# THS3215EVM and THS3217EVM




This user guide describes the characteristics, operation, and use of the THS3215EVM and THS317EVM (THS321xEVM). This evaluation module (EVM) is a demonstration fixture for the THS3215 andTHS3217 family of wideband, differential DAC to single-ended line drivers. The EVM provides 50-Ω input and output termination for easy evaluation with common 50-Ω test equipment. A complete circuit description, schematic diagram, printed circuit board (PCB) layout, and bill of materials are included.

Throughout this document, the terms demonstration kit, evaluation board, evaluation module, and EVM are synonymous with the THS321xEVM.

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# 1 Introduction

This section provides a general description of the THS3215 and THS3217 devices and the EVM.

## 1.1 THS3215 and THS3217 Description

The THS3215 and THS3217 (THS321x) combine the key signal-chain components required to interface with a complementary-current output, digital-to-analog converter (DAC). These two-stage devices deliver the low-distortion, dc-coupled, single-ended signal required by a wide range of applications. The input stage buffers the DAC resistive termination, and converts the signal from differential to single-ended with a fixed gain of 2 V/V. The differential to single-ended output is available externally for direct use, and can also be connected through an RLC filter or attenuator to the input of an internal output power stage (OPS). The wideband, current-feedback, OPS provides all pins externally for flexible gain setting.

An internal 2 × 1 multiplexer (mux) to the OPS noninverting input provides an easy means to select between the internal differential-to-single ended stage (D2S) output or an external input. More information on the THS3215 and THS3217 can be found in their respective product data sheets, SBOS780 and SBOS766.

## 1.2 EVM Description

The THS321xEVM enables performance evaluation of each individual subblock within these devices. The PCB provides various flexible options to also test either the THS3215 or THS3217 as a complete system. The EVM provides placeholders to insert filters at different points within the system to allow for more realistic end-application evaluation.

The following list describes key EVM components:

- Power input: ±6 VDC (typical) at $+V_{CC}$ (P3, TP1) and $–V_{CC}$ (P1, TP2)
- Common reference: GND (P2, TP3 and TP13)
- Interface to the midscale buffer input pin, VMID_IN, through J3 (TP8).
- Interface to the midscale buffer output pin, VMID_OUT, through J4 (TP9).
- Interface to the D2S noninverting signal input pin, IN+, through J1 (TP4).
- Interface to the D2S inverting signal input pin, IN–, through J2 (TP5).
- Interface to the D2S output pin, VO1, through J5 (TP14)
- Interface to the D2S reference input, VREF, through J4. SMA connector J4 is shared with the midscale buffer output. Depending on the components populated on the board, the appropriate signal is available at the SMA connector.
- PATHSEL control though switch CS_SW (TP12). Section 2.2 describes the operation of the switch logic.
- Interface to the OPS external, noninverting input pin, VIN+, through J8.
- DISABLE control though switch PD_SW (TP11). Section 2.2 describes the operation of the switch logic.
- Interface to the OPS output pin, VOUT, through J7 (TP10).
- Interface to the OPS inverting input pin, VIN–, through J6.

## 2 Design Considerations

This section discusses general design considerations and options when setting up and configuring the various blocks in THS321xEVM.

### 2.1 Power Supplies

Power is applied to the board through connectors P1, P2, and P3, as shown in Figure 1. Both bipolar and single-sided supplies can be used. The typical supplies are ±6 V.

**CAUTION**

Supplies beyond ±8.1 V can damage the device.

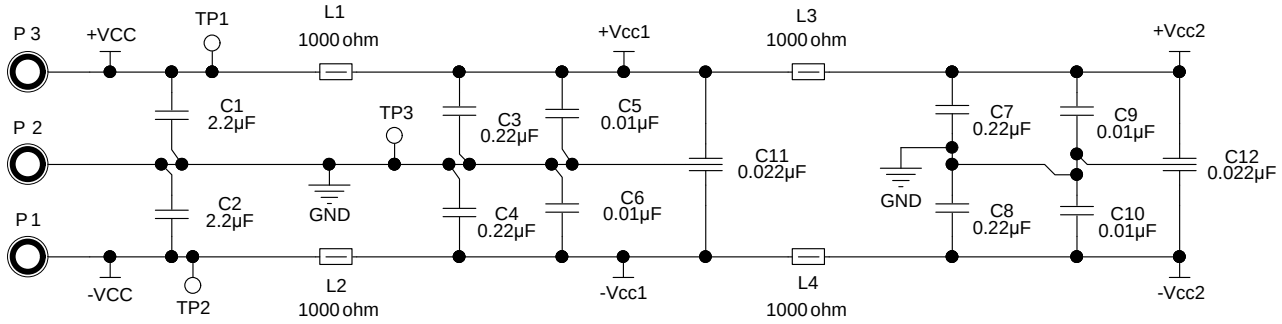


**Figure 1. THS321x Power-Supply Schematic**

### 2.2 Digital Logic Control

There are two bidirectional switches on the THS321xEVM that control the status of the PATHSEL and DISABLE control pins. Figure 2 shows the control logic with respect to the switch position. For brevity, the PATHSEL control is shown as CS and the DISABLE control is shown as PD on the PCB. The full switch settings are listed in Table 1.

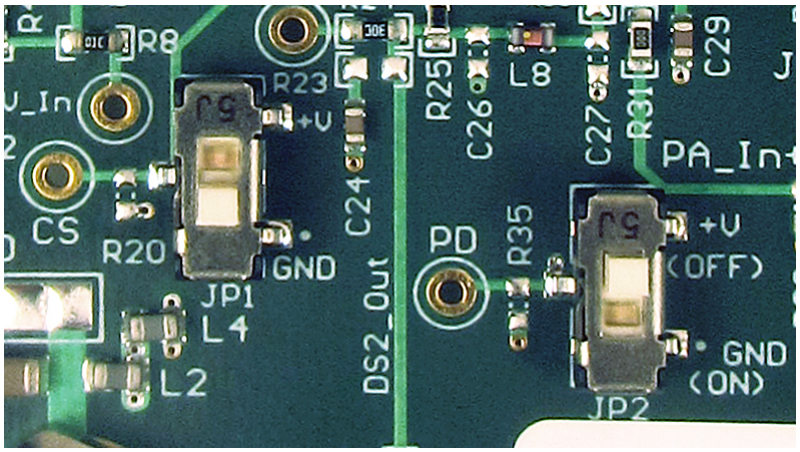


**Figure 2. Logic Control Switches**

**Table 1. Bidirectional Switch Settings**

| Switch | Set to +VCC | Set to GND |
|---|---|---|
| CS_SW (PATHSEL control) | OPS external, noninverting path | Internal path from D2S to OPS |
| PD_SW (DISABLE control) | OPS off | OPS on |

## 2.3 Midscale or Reference Buffer

The EVM is configured by default to drive a ground-centered signal. In cases where a different output common-mode voltage is required, use the midscale buffer to provide a low impedance path. This buffer is also used in applications where a servo loop is required to set the dc offset of the system to a desired value. Alternatively, the buffer can also be used to set the reference voltage in single-supply applications where the inputs to the D2S are ac-coupled. The midscale buffer input defaults to the midsupply voltage. In cases where a different input voltage is required, adjust the R14 potentiometer (uninstalled by default) to achieve the desired offset voltage. Resistor R62 must be appropriately sized, and resistor R63 uninstalled in order to set the correct voltage at the input of the midscale buffer. The EVM allows for connecting the output of the midscale buffer to various nodes of the THS321x. The different options are:

1. In single-supply and ac-coupled applications, the common-mode input of the D2S is configured in one of two ways. The first way is by installing R56 = 0 Ω. This setting connects the output of the buffer to the Junc_Vocm node on the board. Components R5, R6, R11, and C19 must be appropriately sized and installed. The second way is by applying an external common-mode voltage through test-point TP7.
2. If the output common-mode voltage of the D2S must be set to any voltage other than GND, uninstall resistors R54 and R51, and install R48 instead. This configuration connects the output of the midscale buffer to VREF (pin 14).
3. If the OPS is configured in the noninverting mode with a common-mode dc offset voltage from the D2S, then the D2S provides the necessary dc bias to the noninverting pin of the OPS. However, if the OPS $R_G$ is grounded, the dc common-mode offset voltage from the D2S is amplified by $(1 + R_F / R_G)$, and may result in limited output headroom from the OPS. To prevent this limitation, connect $R_G$ to the midscale buffer output so that the common-mode gain is 0 dB by setting R55 to the desired value of the gain resistor and uninstalling R42. Installing R55 connects the output of the midscale buffer to Junc_Vneg enabling configuration of the OPS in a level-shifted, common-mode, noninverting configuration. Make sure that R54 and R60 are uninstalled, and R51 = R53 = 0 Ω in this configuration.

The areas within the dashed boxes in Figure 3 show the described configurations.

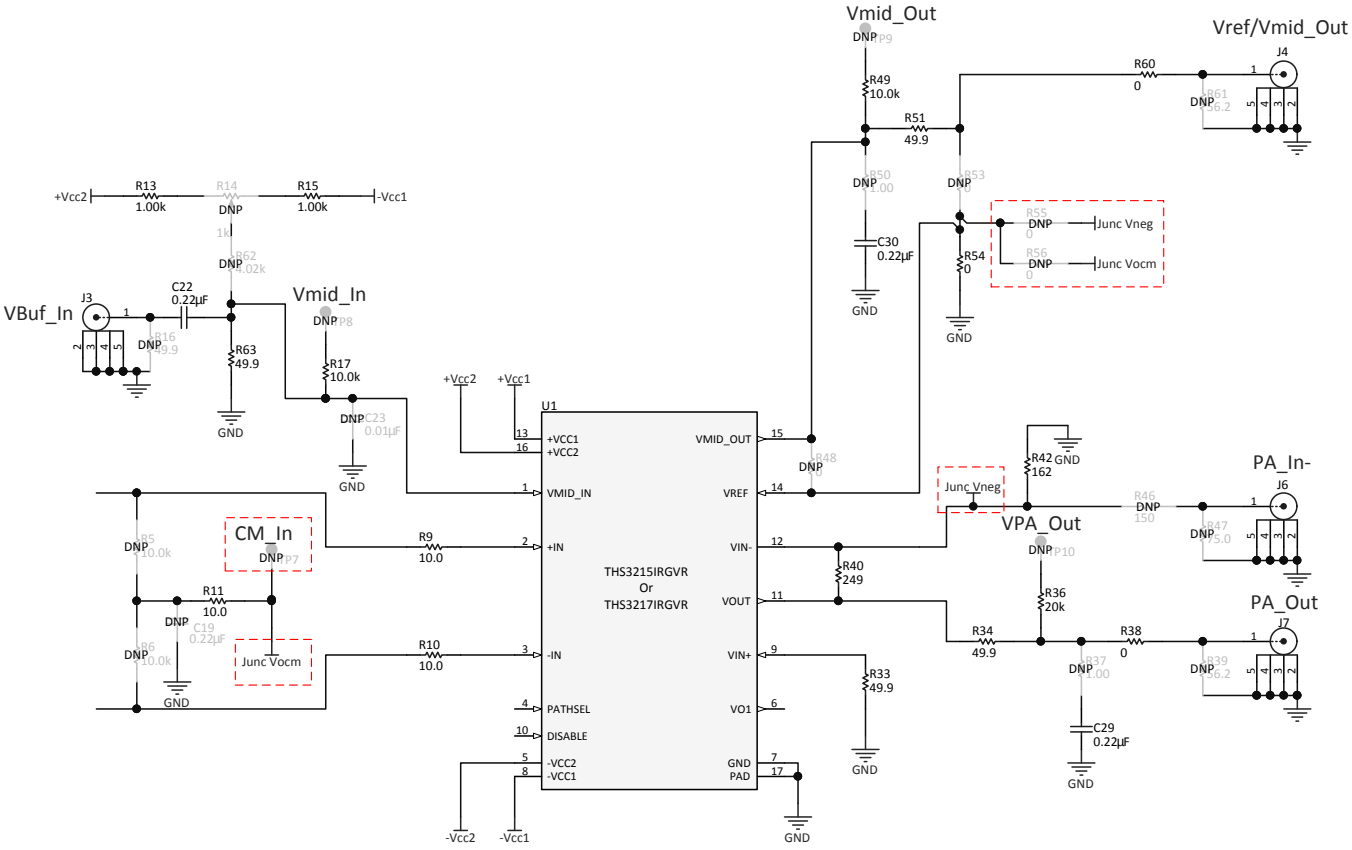


**Figure 3. Midscale Buffer Configuration Options**

## 2.4 Differential to Single-Ended Stage (D2S)

The D2S inputs are driven by an external differential signal through SMA connectors J1 and J2. Standard lab equipment usually provides only a single-ended output. The LMH3401, a very wideband, single-ended to differential amplifier, was used during product evaluation to drive a differential signal into the D2S. The spacing of the SMA connectors on the THS321xEVM is designed to interface directly with the output of the LMH3401EVM through standard SMA barrel connectors. The THS321xEVM provides a standard 100-Ω differentially-terminated resistive network to GND, dc-coupled to the D2S input pins. Figure 4 shows the EVM schematic of the D2S input/output network with the default passive components installed. The output of the D2S can also be measured externally at J5.

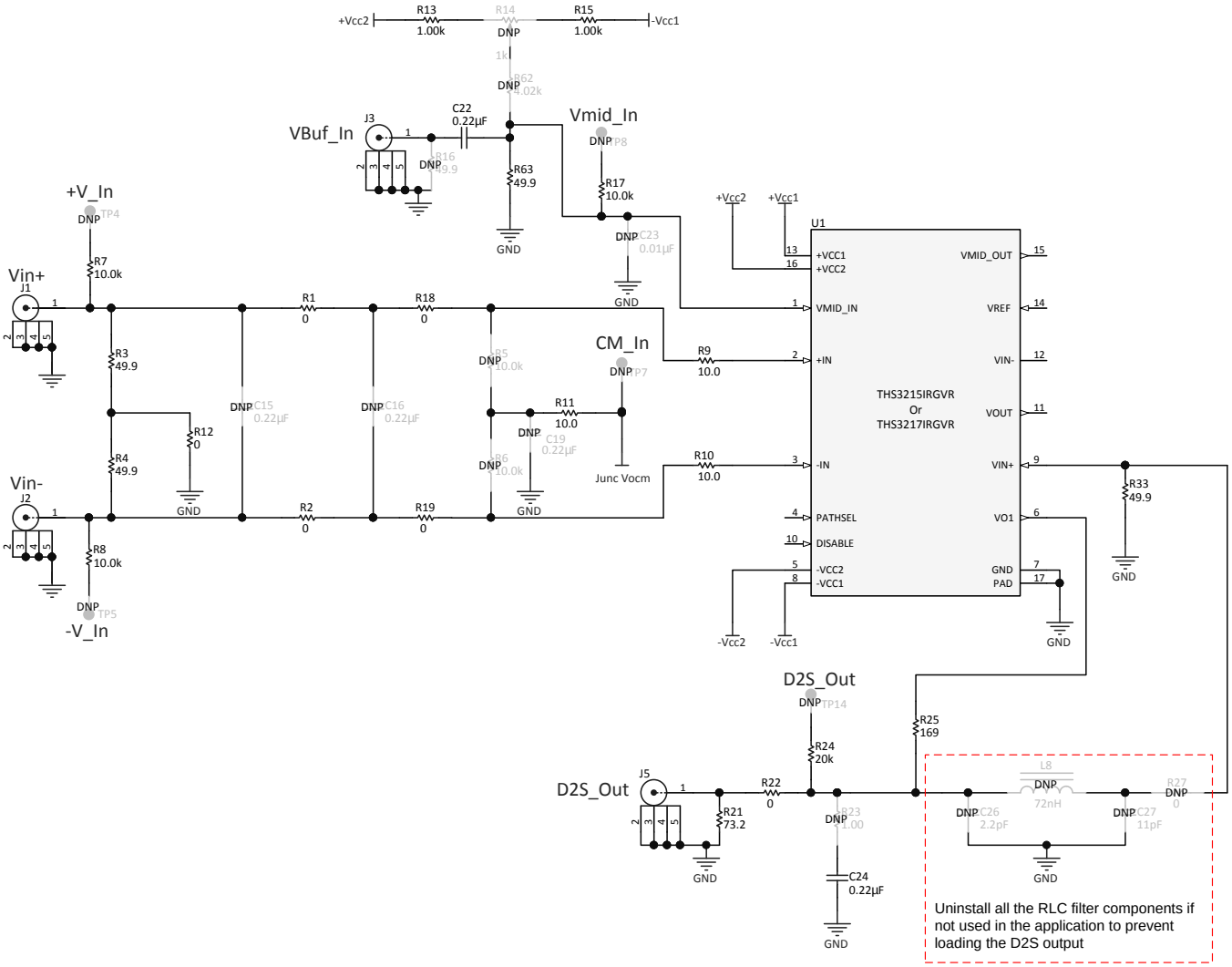


**Figure 4. D2S Input Connection Options**

The EVM allows for flexibility in the D2S input network configuration. The different options are:

1. In order to reduce the high-frequency noise and distortion components from the previous stage driving the D2S, a passive RLC filter can be inserted prior to the D2S inputs. Figure 5 shows an example of a third-order, 200-MHz, Butterworth filter placed between the DAC output and D2S input. The THS321xEVM is able to evaluate system performance with similar RLC-filter architectures installed on the board.

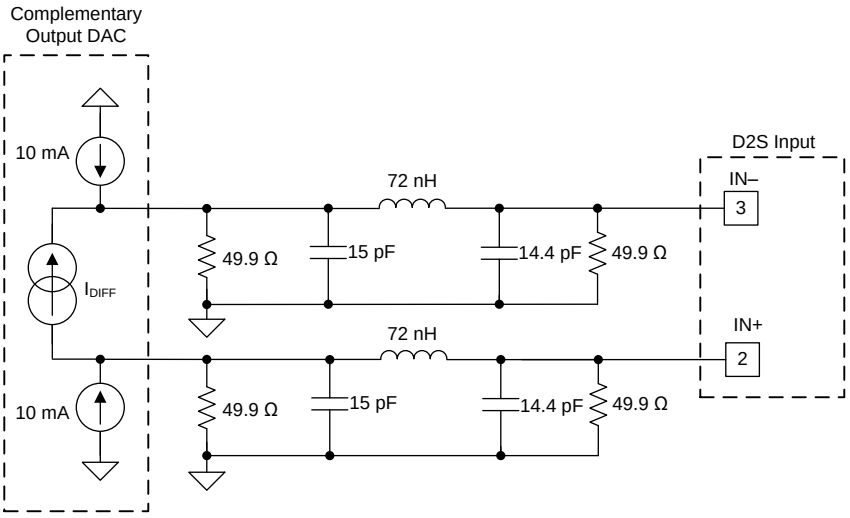


**Figure 5. 200-MHz Butterworth Filter Before D2S Inputs**

2. In single-supply and ac-coupled applications, use R18 and R19 to install the appropriately-sized, ac-blocking capacitors (see Figure 4). Use the midscale buffer output in conjunction with R56, R11, R5, and R6 to set the desired dc common-mode voltage for the D2S input.
3. The output of the D2S is fed into the internal, noninverting input pin of the OPS by driving PATHSEL low through switch CS_SW.
4. Certain applications may require an interstage filter inserted between the D2S and OPS to reduce overall system noise, and prevent high-frequency harmonics from previous stages propagating to the OPS output. In such situations, use C26, L8, and C27 to insert a third-order, RLC filter into the signal path of the THS321x (see Figure 4). The output of the filter then drives the external noninverting input of the OPS, VIN+ (pin 9).

## 2.5 Output Power Stage (OPS)

As described in option 3 and option 4 of Section 2.4, the OPS can be driven internally or externally. The OPS can be also used as a standalone amplifier in an inverting or noninverting configuration. The output of the OPS is available at SMA connector J7. Figure 6 shows the EVM schematic of the OPS input/output network with the default passive components installed. The different options are:

1. When configuring the OPS as a standalone-noninverting amplifier, apply the external input at J8. Set termination resistor R33 = 49.9 Ω.
2. When configuring the OPS as a standalone-inverting amplifier, apply the external input at J6. Set R46 as the $R_G$ resistor, and R47 as the termination resistor. R42 must be uninstalled in this configuration.
3. To conserve power, disable the OPS by setting the DISABLE control low through switch PD_SW.

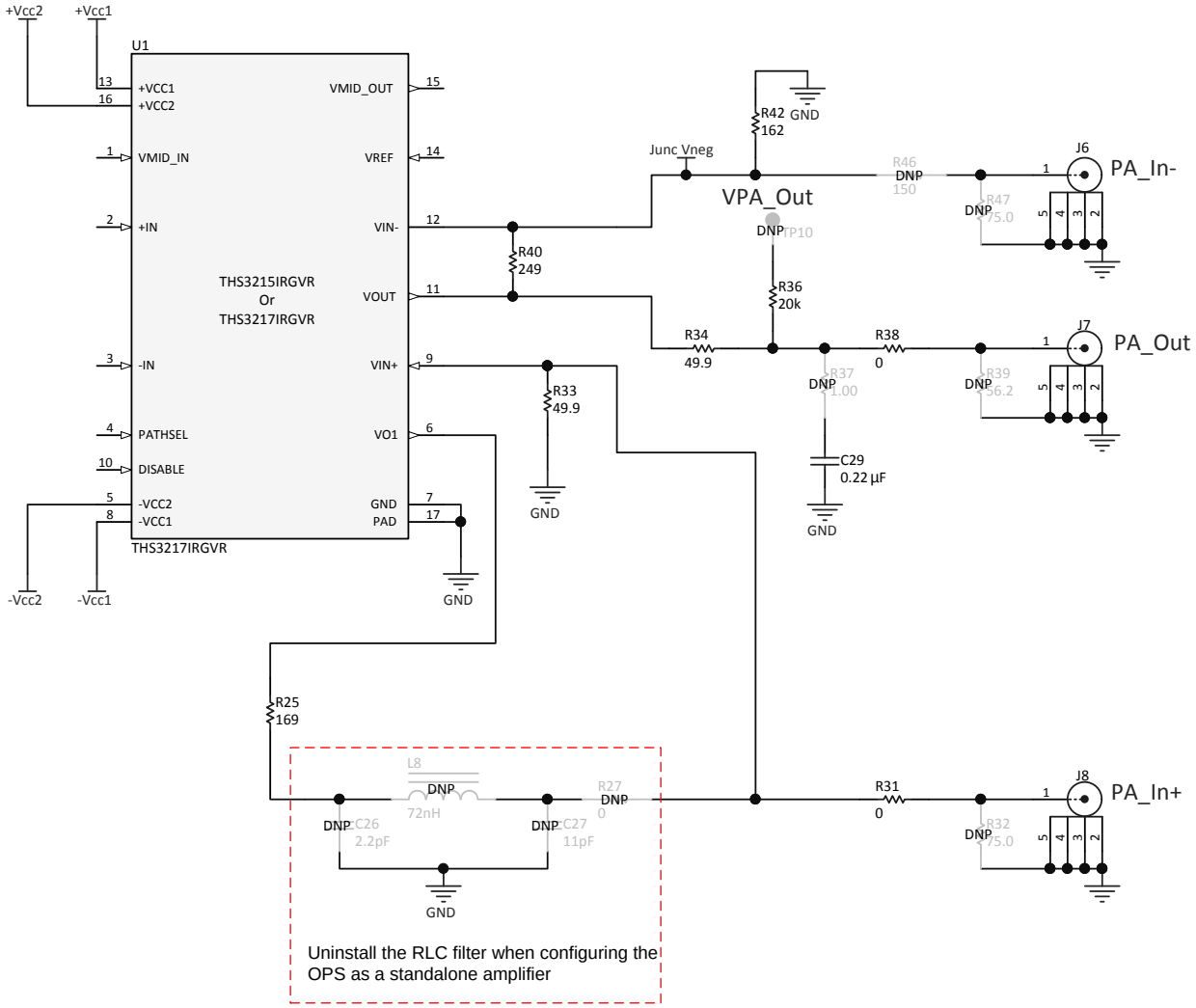


**Figure 6. OPS Input and Output Connection Options**

# 3 Schematic, PCB Layout, and Bill of Materials

This section provides a complete schematic diagram, PCB layout, and bill of materials (BOM) for the THS321xEVM.

## 3.1 Schematic

Figure 7 shows the schematic.

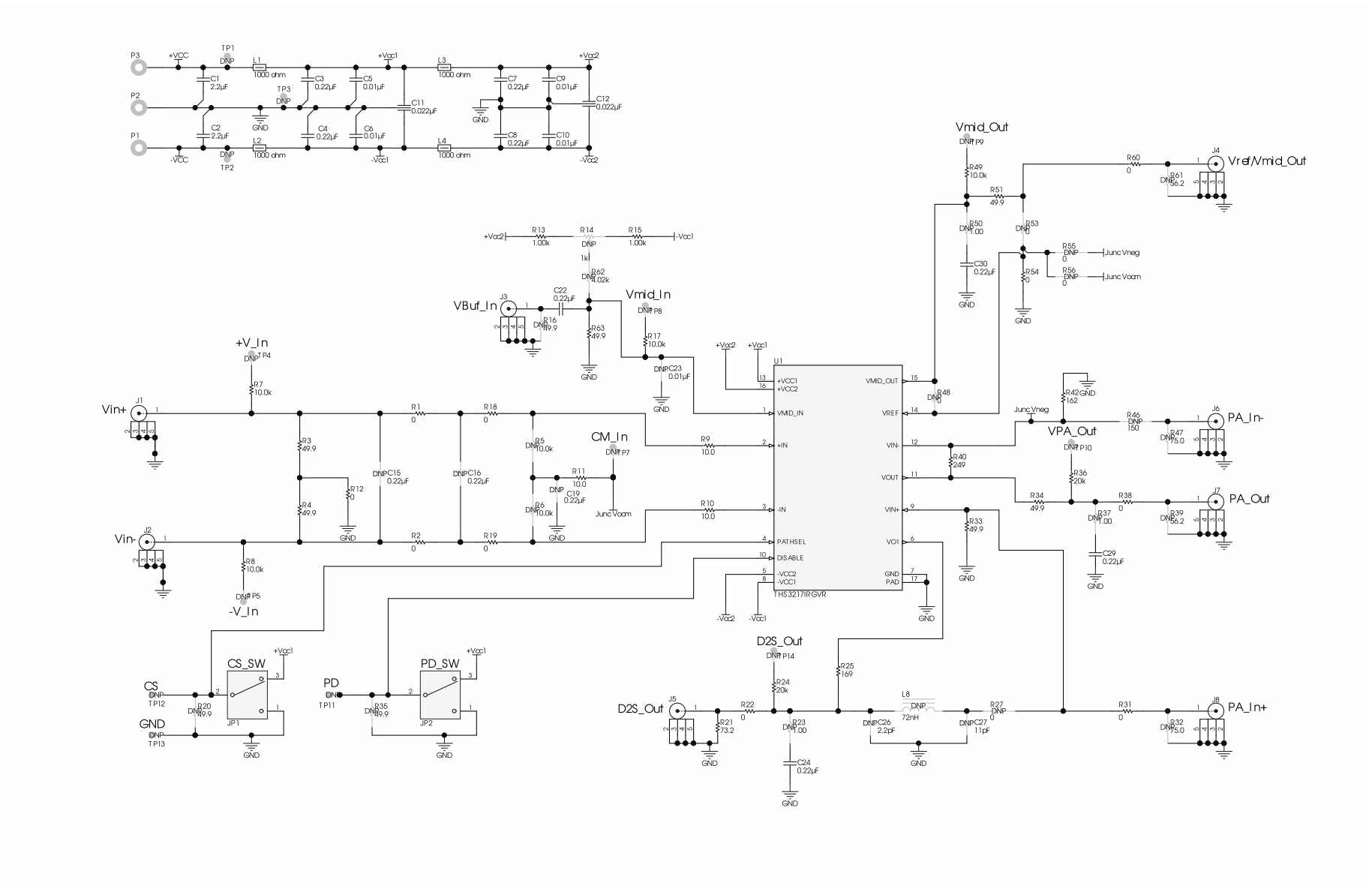


**Figure 7. EVM Schematic**

### 3.2 PCB Layout

The PCB layers are shown in Figure 8 through Figure 13.

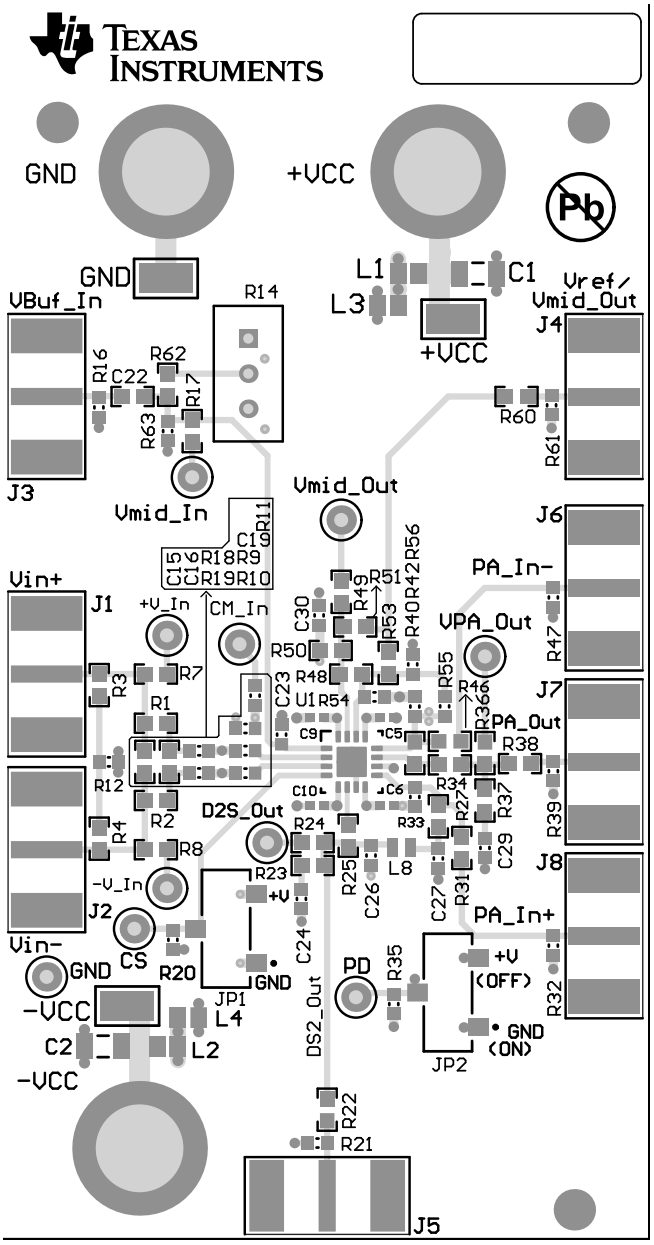


Figure 8. Layer 1: Top Signal Layer

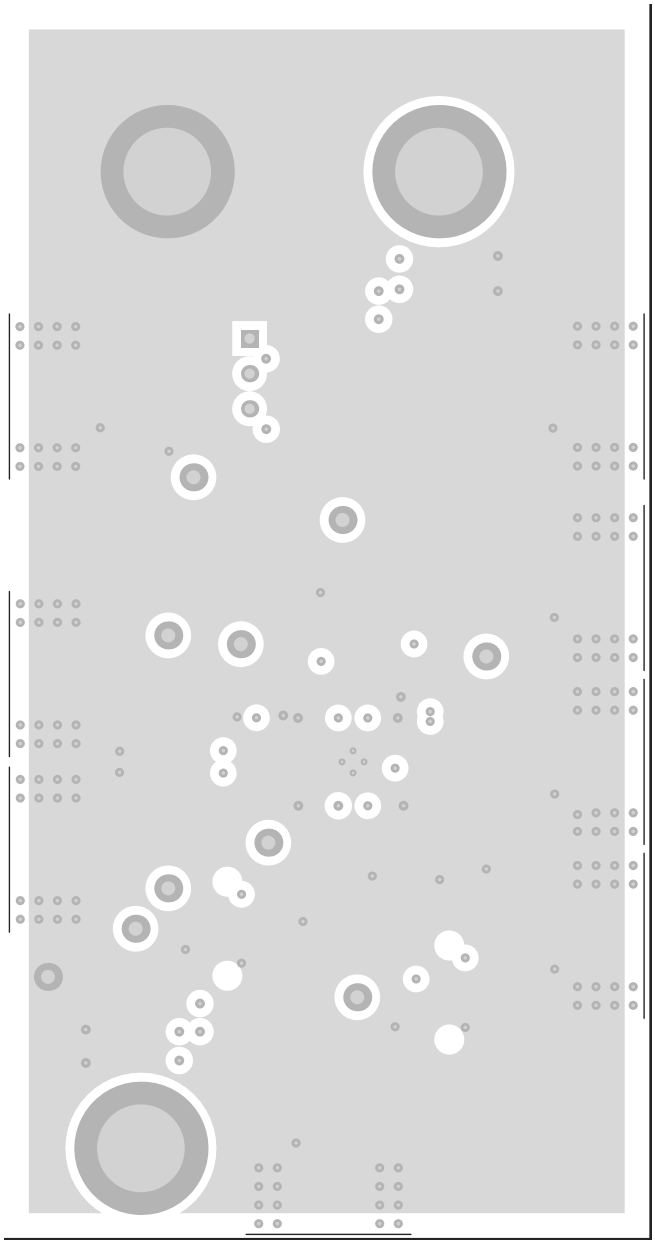

Figure 9. Layer 2: GND Plane

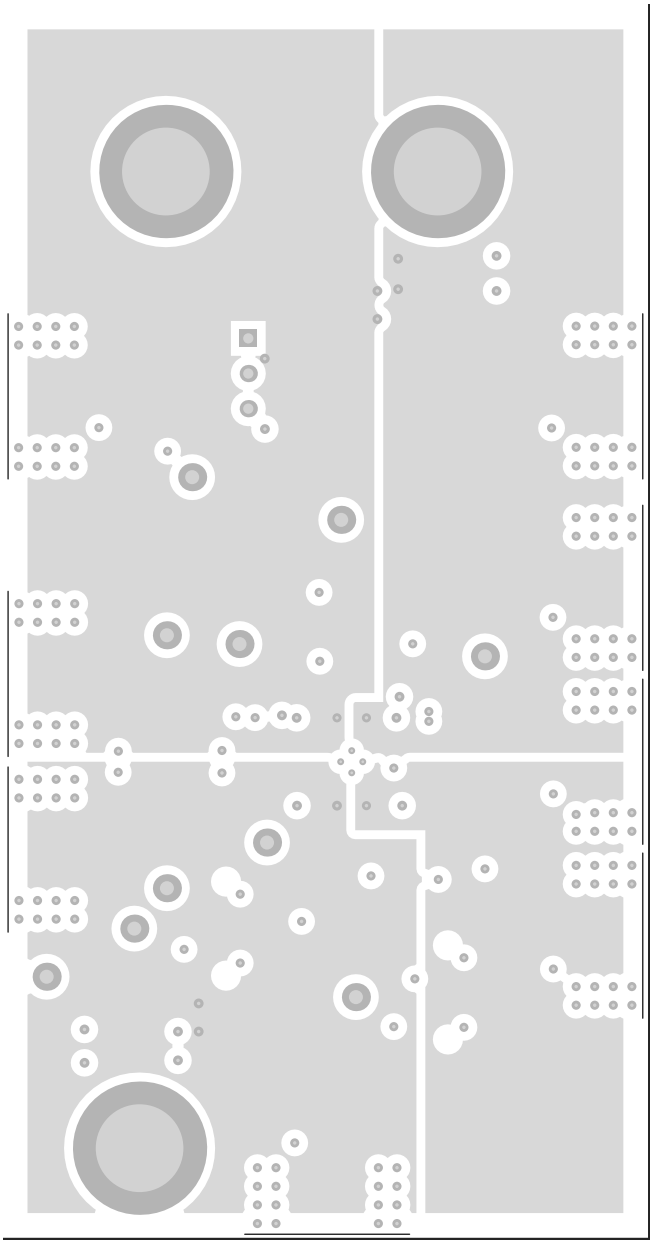

**Figure 10. Layer 3: Power Plane, ±$V_{CC}$**

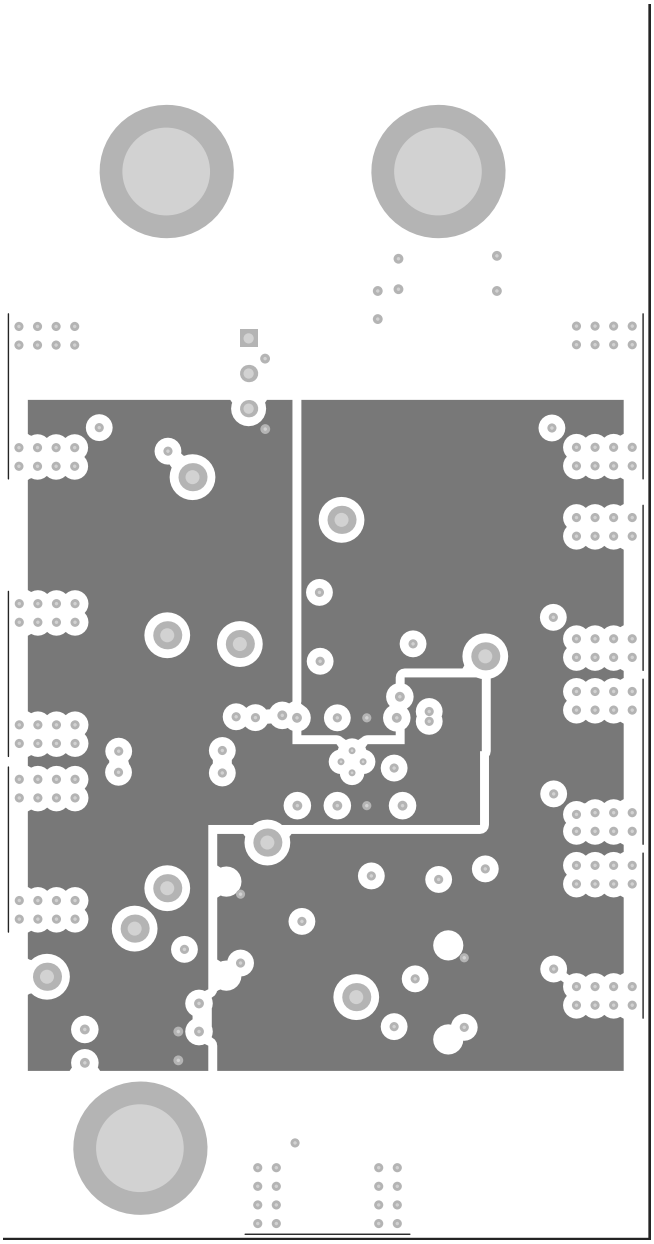

**Figure 11. Layer 4: Power Plane, ±$V_{CC}$**

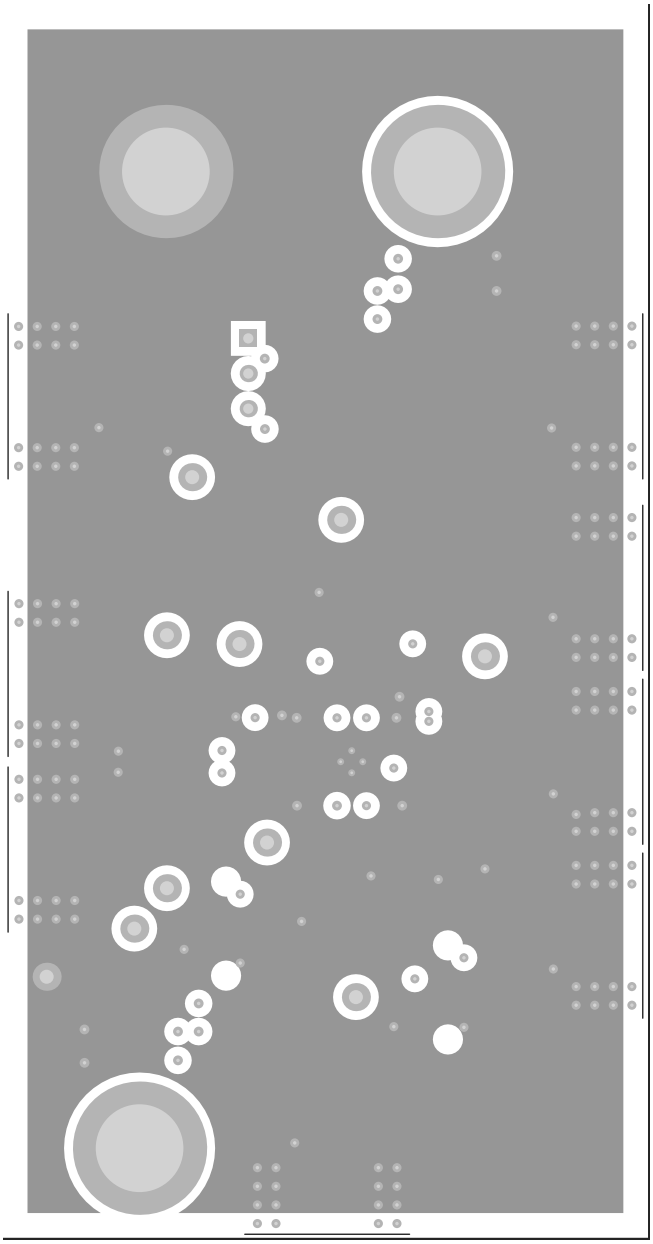

Figure 12. Layer 5: GND Plane

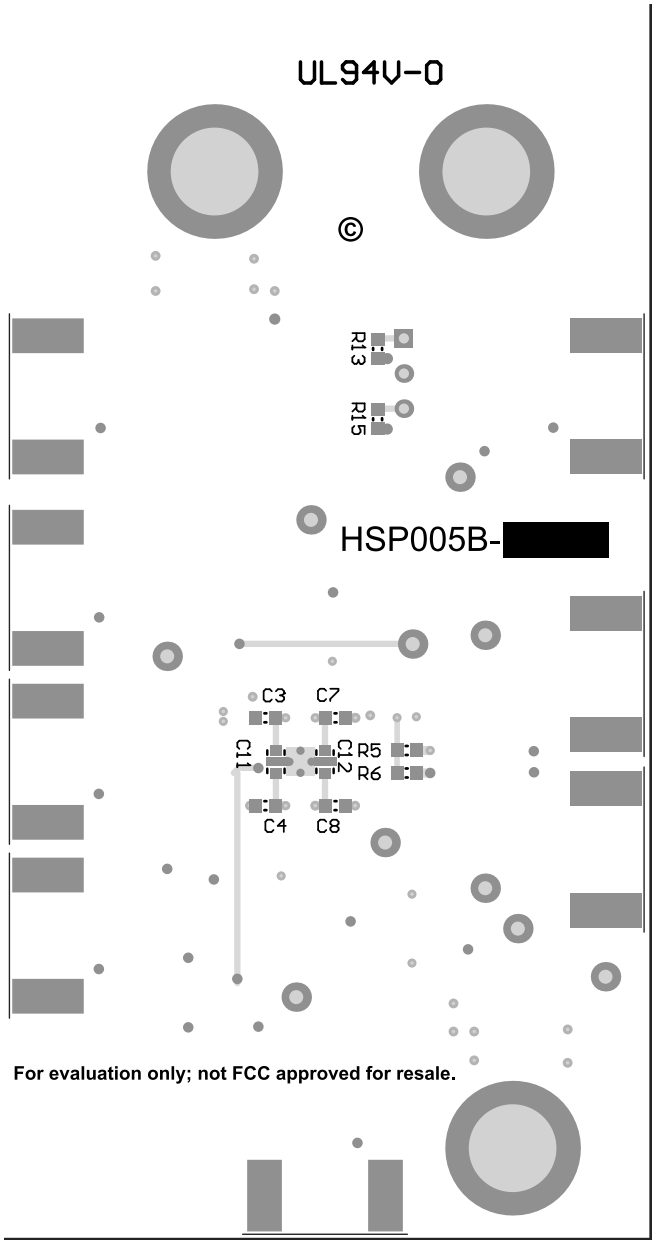


Figure 13. Layer 6: Bottom Signal Layer

## 3.3 Bill of Materials

Table 2 lists the bill of materials for the THS321xEVM. The BOMs for the THS3215EVM and THS3217EVM are identical except for the line item corresponding to the DUT model populated on the EVM.

**Table 2. Bill of Materials, THS321x EVM**

| Item # | Reference Designator | Quantity | Part Number | Value | Description |
|---|---|---|---|---|---|
| 1 | C1, C2 | 2 | GRM31MR71E225KA93L | MuRata | CAP, CERM, 2.2 µF, 25 V, +/- 10%, X7R, 1206 |
| 2 | C3, C4, C7, C8, C22, C24, C29, C30 | 8 | GRM188R71E224KA88D | MuRata | CAP, CERM, 0.22 µF, 25 V, +/- 10%, X7R, 0603 |
| 3 | C5, C6, C9, C10 | 4 | GRM155R71E103KA01D | MuRata | CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0402 |
| 4 | C11, C12 | 2 | 250X14W223MV4T | Johanson Technology | CAP, CERM, 0.022 µF, 25 V, +/- 20%, X7R, 0603 |
| 5 | J1, J2, J3, J4, J5, J6, J7, J8 | 8 | 142-0701-851 | Emerson Network Power | Connector, End launch SMA, 50 ohm, SMT |
| 6 | JP1, JP2 | 2 | CL-SB-12B-01T | Copal Electronics | Switch, Slide, SPDT, 0.2A, GULL, 12V, SMD |
| 7 | L1, L2, L3, L4 | 4 | BLM21AG102SN1D | MuRata | Ferrite Bead, 1000 ohm @ 100 MHz, 0.5 A, 0805 |
| 8 | L8 | 1 | AISC-0603HP-72NJ-T | Abracon Corporation | Inductor, Wirewound, 72 nH, 0.58 A, 0.35 ohm, SMD |
| 9 | P1, P2, P3 | 3 | 6095 | Keystone | Standard Banana Jack, Uninsulated |
| 10 | R1, R2, R12, R18, R19, R22, R31, R38, R54, R60 | 10 | ERJ-3GEY0R00V | Panasonic | RES, 0, 5%, 0.1 W, 0603 |
| 11 | R3, R4, R33, R34, R51, R63 | 6 | ERJ-3EKF49R9V | Panasonic | RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 |
| 12 | R5, R6, R7, R8, R17, R49 | 6 | ERJ-3EKF1002V | Panasonic | RES, 10.0 k, 1%, 0.1 W, 0603 |
| 13 | R9, R10, R11 | 3 | RC0603FR-0710RL | Yageo America | RES, 10.0, 1%, 0.1 W, 0603 |
| 14 | R13, R15 | 2 | ERJ-3EKF1001V | Panasonic | RES, 1.00 k, 1%, 0.1 W, 0603 |
| 15 | R21 | 1 | CRCW060373R2FKEA | Vishay-Dale | RES, 73.2, 1%, 0.1 W, 0603 |
| 16 | R24, R36 | 2 | CRCW060320K0JNEA | Vishay-Dale | RES, 20 k, 5%, 0.1 W, 0603 |
| 17 | R25 | 1 | CRCW0603169RFKEA | Vishay-Dale | RES, 169, 1%, 0.1 W, 0603 |
| 18 | R40 | 1 | CRCW0603249RFKEA | Vishay-Dale | RES, 249, 1%, 0.1 W, 0603 |
| 19 | R42 | 1 | CRCW0603162RFKEA | Vishay-Dale | RES, 162, 1%, 0.1 W, 0603 |
| 20 | U1 | 1 | THS3215IRGVR OR THS3217IRGVR | Texas Instruments | Wideband Differential DAC to Single Ended Line Driver, RGV0016A |
| 21 | C15, C16, C19 | 0 | GRM188R71E224KA88D | MuRata | CAP, CERM, 0.22 µF, 25 V, +/- 10%, X7R, 0603 |
| 22 | C23 | 0 | GRM188R71E103KA01D | MuRata | CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0603 |
| 23 | C26 | 0 | 06035A2R2CAT2A | AVX | CAP, CERM, 2.2 pF, 50 V, +/- 11%, C0G/NP0, 0603 |
| 24 | C27 | 0 | GRM1885C1H110JA01D | MuRata | CAP, CERM, 11 pF, 50 V, +/- 5%, C0G/NP0, 0603 |
| 25 | R14 | 0 | 3296W-1-102LF | Bourns | TRIMMER, 1k ohm, 0.5W, TH |
| 26 | R16, R20, R35 | 0 | ERJ-3EKF49R9V | Panasonic | RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 |
| 27 | R23, R37, R50 | 0 | CRCW06031R00FKEA | Vishay-Dale | RES, 1.00, 1%, 0.1 W, 0603 |
| 28 | R27, R48, R53, R55, R56 | 0 | ERJ-3GEY0R00V | Panasonic | RES, 0, 5%, 0.1 W, 0603 |
| 29 | R32, R47 | 0 | CRCW060375R0FKEA | Vishay-Dale | RES, 75.0, 1%, 0.1 W, 0603 |
| 30 | R39, R61 | 0 | RC0603FR-0756R2L | Yageo America | RES, 56.2, 1%, 0.1 W, 0603 |
| 31 | R46 | 0 | RC0603FR-07150RL | Yageo America | RES, 150, 1%, 0.1 W, 0603 |
| 32 | R62 | 0 | RC0603FR-074K02L | Yageo America | RES, 4.02 k, 1%, 0.1 W, 0603 |
| 33 | TP1, TP2, TP3 | 0 | 5019 | Keystone | Test Point, Miniature, SMT |
| 34 | TP4, TP5, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14 | 0 | 5003 | Keystone | Test Point, Miniature, Orange, TH |

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Original (February 2016) to A Revision** **Page**

- Added THS3215EVM and related information to this user's guide ..... 1
- Changed front page EVM photo ..... 1
- Changed Figure 3 to match new Figure 7 schematic ..... 5
- Changed Figure 4 to match new Figure 7 schematic ..... 6
- Changed Figure 7 ..... 9
- Changed PCB layout, Figure 8 to Figure 13 ..... 10
- Changed BOM ..... 13

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