TI-PLABS-AMP-EVM

This user's guide describes the characteristics, operation, and use of the TI-PLABS-AMP-EVM evaluation board. It discusses how to set up the hardware, and reviews various aspects of the EVM operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the TI-PLABS-AMP-EVM . This user's guide also includes information regarding operating procedures and input/output connections, an electrical schematic, printed circuit board (PCB) layout drawings, and a parts list for the EVM.

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1 Overview

The TI-PLABS-AMP-EVM is an experimentation board of op amp circuits. The EVM provides inverting-, noninverting-, cascaded-, and filter-amplifier configurations. The EVM is intended for use with the Precision Labs video series. The video series covers theory and laboratory experiments for different op amp subjects.

1.1 TI-PLABS-AMP-EVM Kit Contents

Table 1 details the contents of the TI-PLABS-AMP-EVM kit, and Figure 1 shows all of the included hardware. Contact the Texas Instruments Product Information Center at (972) 644-5580 if any component is missing.

Table 1. Contents of TI-PLABS-AMP-EVM Kit

Item	Quantity
TI-PLABS-AMP-EVM Test Board 1, Rev B	1
OPA211 DIP Adaptor	2
OPA188 DIP Adaptor	2
OPA171 DIP Adaptor	1
OPA277 DIP Adaptor	1
OPA140 DIP Adaptor	1
Jumper Shunts	18

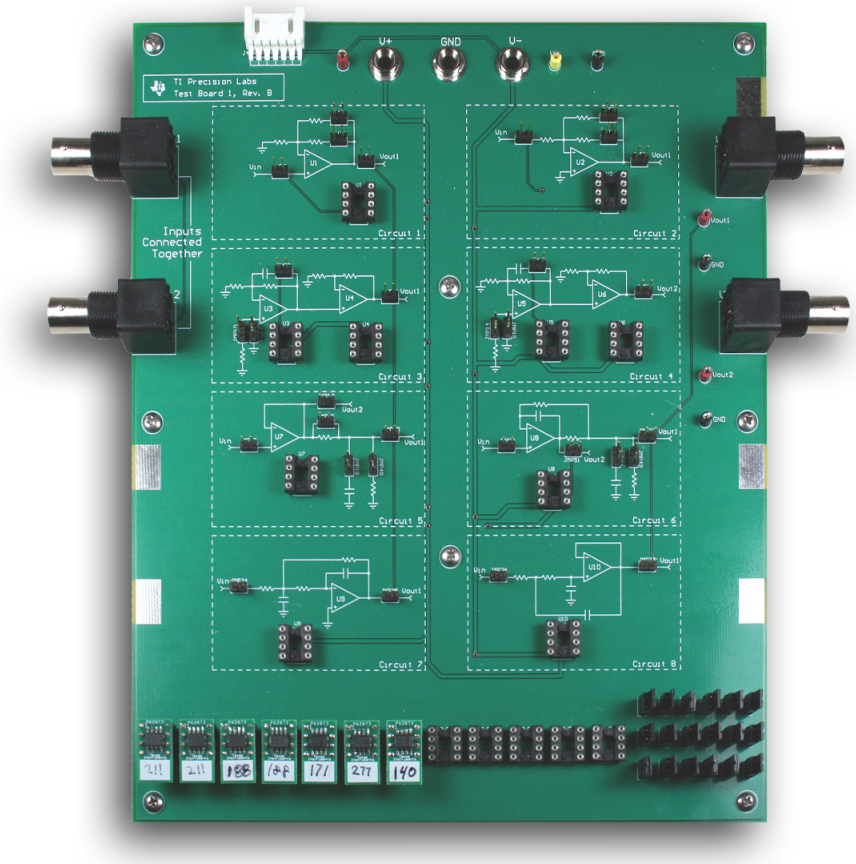

Figure 1. Hardware included with TI-PLABS-AMP-EVM Kit

1.2 Related Documentation from Texas Instruments

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the TI-PLABS-AMP-EVM. This user's guide is available from the TI web site under literature number SBOU150. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site at http://www.ti.com/, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number

Table 2. Related Documentation

Document	Literature Number
OPA211 Product Data Sheet	SBOS377
OPA188 product data sheet	SBOS642
OPA171 product data sheet	SBOS516
OPA277 product data sheet	SBOS079
OPA140 product data sheet	SBOS498

2 External Connections

2.1 Inputs, Outputs, and Power

Figure 2 shows the connections between the TI-PLABS-AMP-EVM and the test equipment. In this example, National Instruments' VirtualBench™ is used, but any standard test equipment can be used. Connect power to the EVM using connector J4 (Molex 6-pin power connector), or with three banana jacks (labeled V+, V–, and GND). The input connections are on the right-hand side of the board, and the output connections are on the left side. Note that the input connections are shorted together. One input connection is intended as a signal generator connection, and the other connection is used to monitor the input. The two output connections allow the comparison of two different circuits.

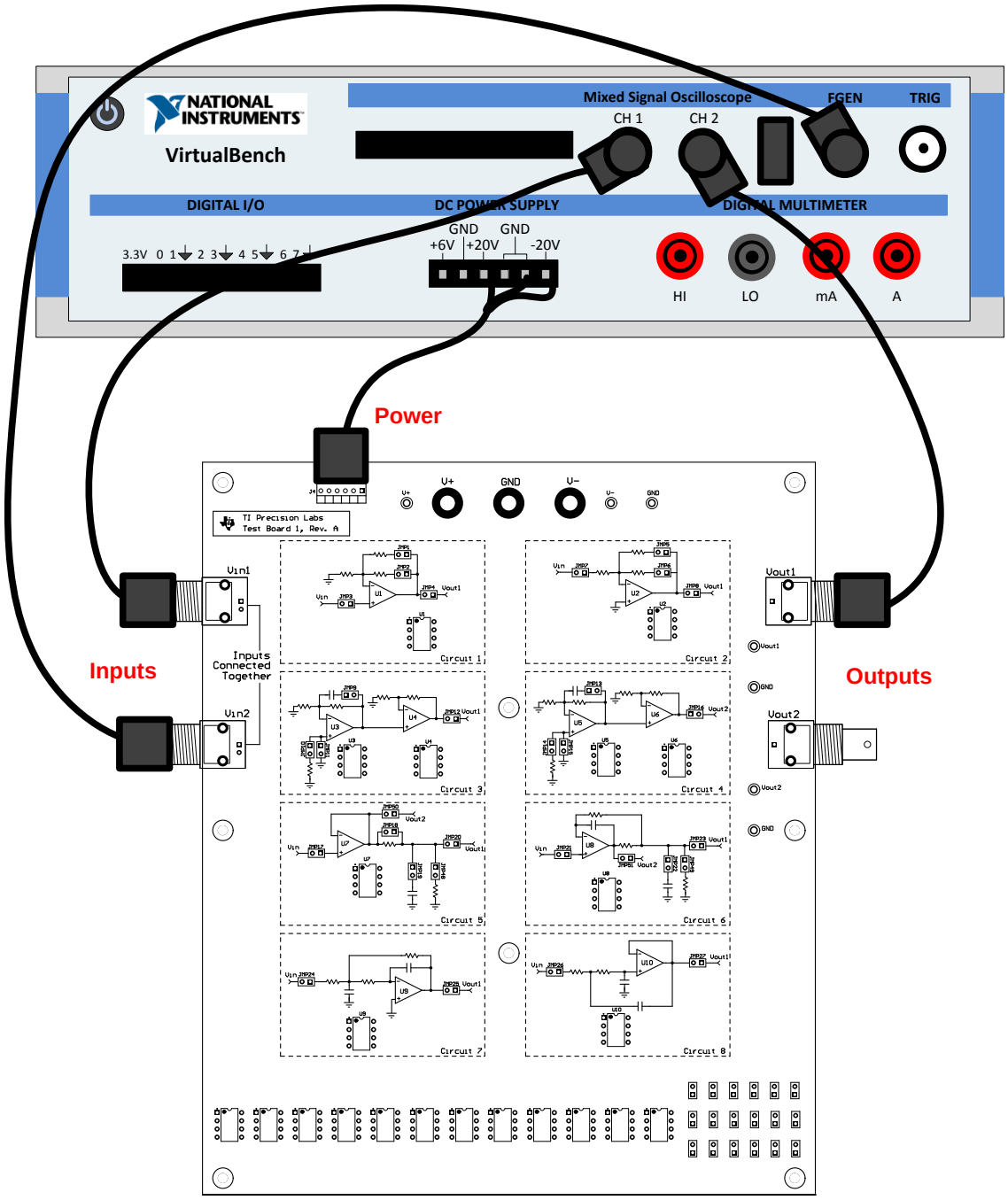

Figure 2. Input Output and Power Connections

2.2 DIP Adaptors and Jumper Storage

Figure 3 shows where the DIP adaptor devices and jumpers are stored on the TI-PLABS-AMP-EVM. Note that the DIP adaptor pins are grounded and no power is applied in this storage area. In general, populate only one experimentation circuit at a time. Make sure that all other circuits jumpers and DIP adaptors are removed and stored in the area identified in Figure 3. The only exception to this rule is that circuits 3 and 4 can both be populated at the same time so that the outputs can be compared.

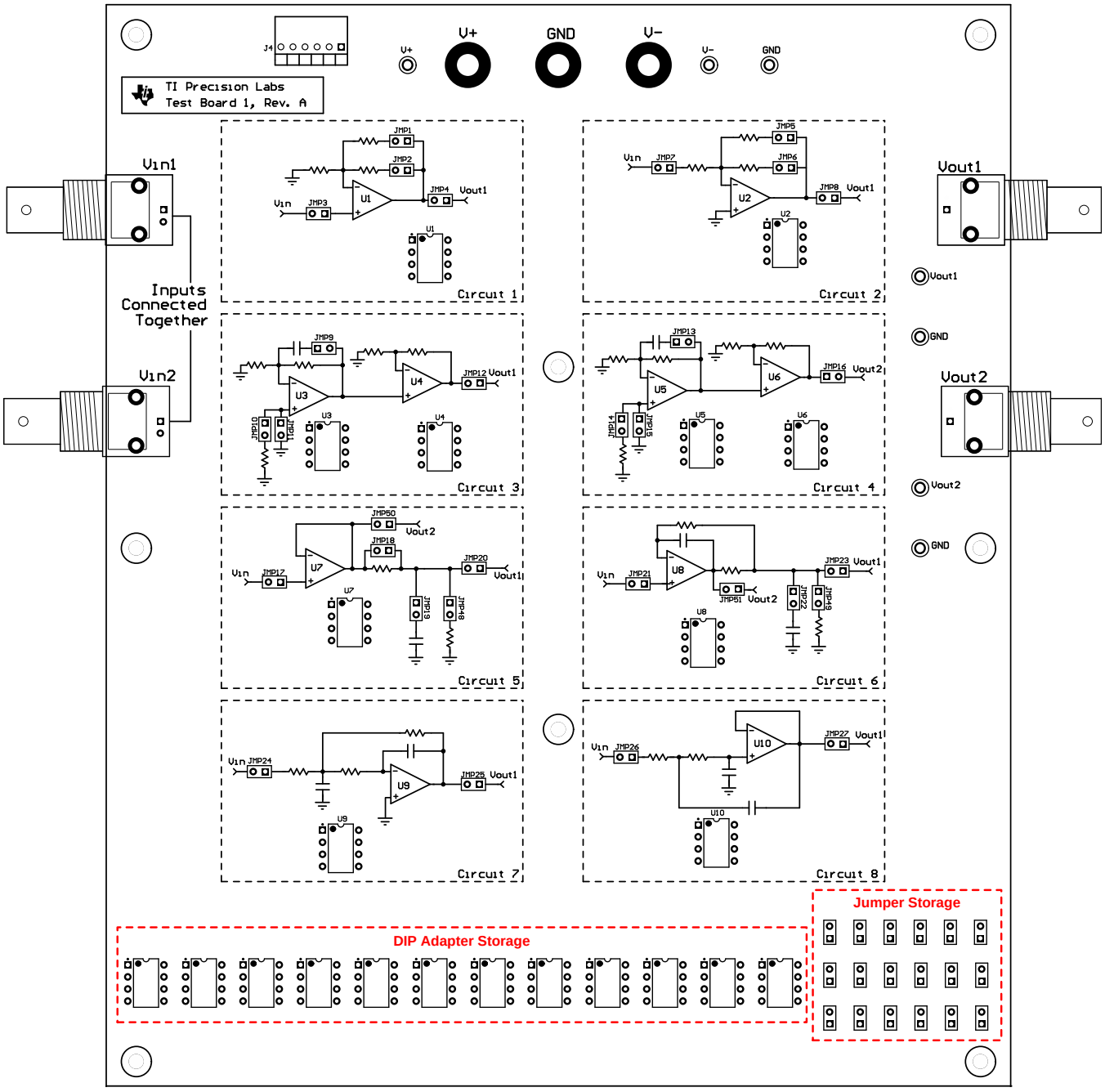

Figure 3. DIP Adaptor and Jumper Storage

3 Hardware Setup

The TI-PLABS-AMP-EVM hardware setup overview involves connecting the shunt and load resistor to the EVM, applying power, setting the jumpers, and measuring the output. This section presents the details of this procedure. The procedure given in each Precision Labs video provides additional information.

3.1 Electrostatic Discharge Warning

Many of the components on the TI-PLABS-AMP-EVM are susceptible to damage by electrostatic discharge (ESD).

CAUTION

Observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

3.2 Dip Adaptor Devices

DIP adaptor cards containing different amplifier types are used for the experiments. Bent pins are a common problem that occurs when the adaptor cards are improperly removed from a socket. The proper way to remove the dip adaptor is to gently rock the card back and forth while pulling upward, as shown in Figure 4.

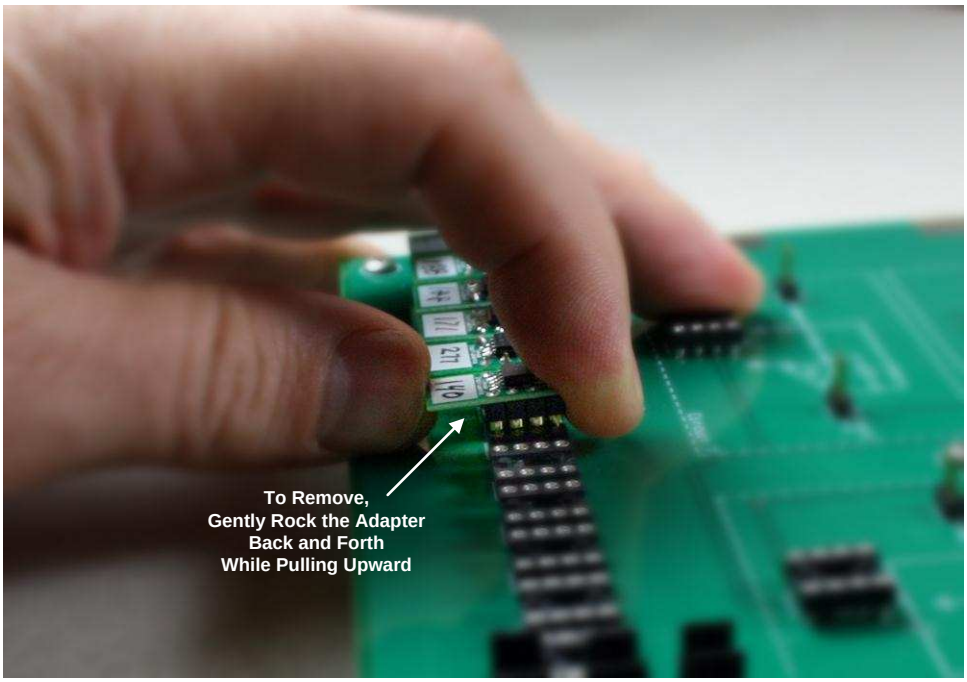

Figure 4. Removing the DIP Adaptor

3.3 Configuring a Circuit

Figure 5 shows an example of how a test circuit is configured. In this example, jumpers are used to connect the input, output, load resistance, and load capacitance. The dip adaptor card for the OPA140 is also installed. The Precision Labs videos give instructions on how the jumpers are configured and which amplifier is used.

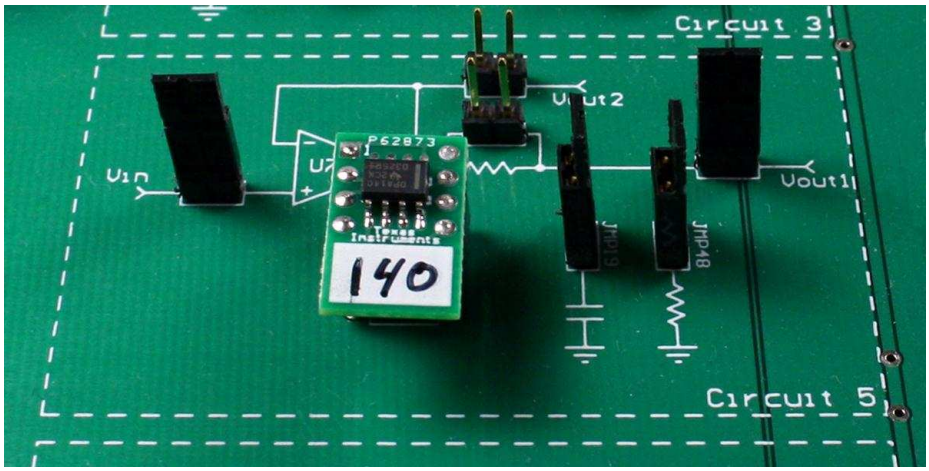

Figure 5. Configuring a Circuit

3.4 Do Not Short the Outputs of Two Circuits

For most experiments, only one test circuit is used at a time. Figure 6 shows a problem that occurs when populating two circuits simultaneously. In this example, both circuit 5 and circuit 6 are populated at the same time causing the outputs to short together.

CAUTION

This configuration produces erratic operation and may damage the circuits under test.

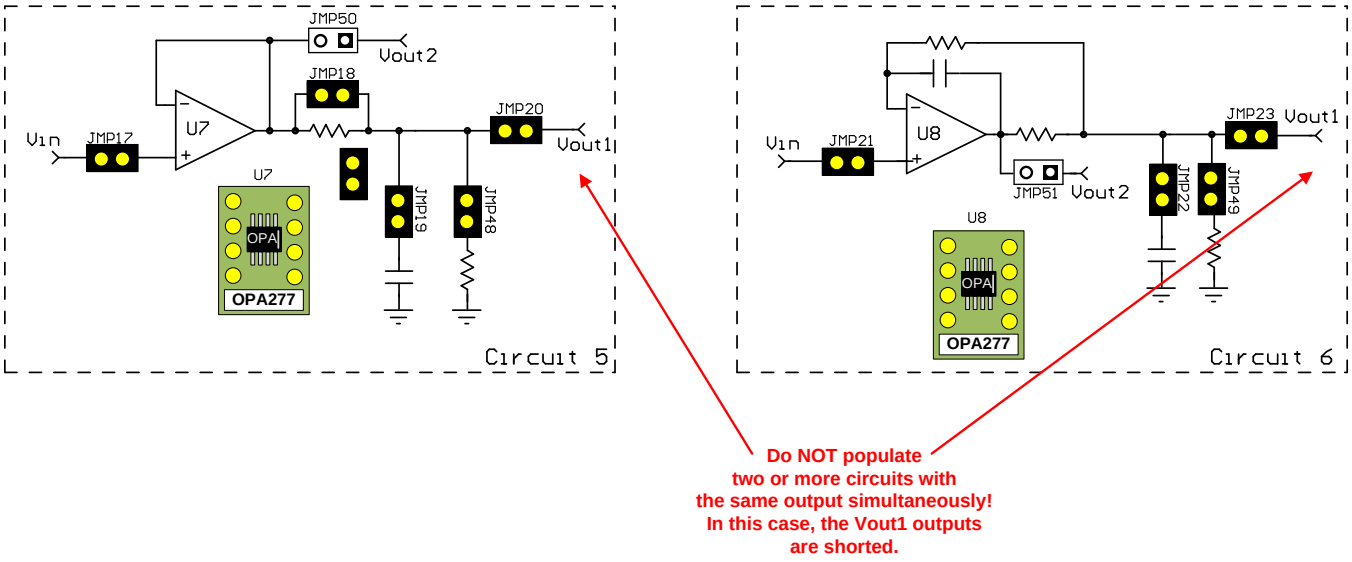

Figure 6. Wrong Connection: Outputs are Shorted

Figure 7 shows the only case where two circuits are populated simultaneously. In this case, both circuit 3 and circuit 4 are populated so that the two outputs are compared to each other. Note that in this case, the outputs are monitored on separate scope channels.

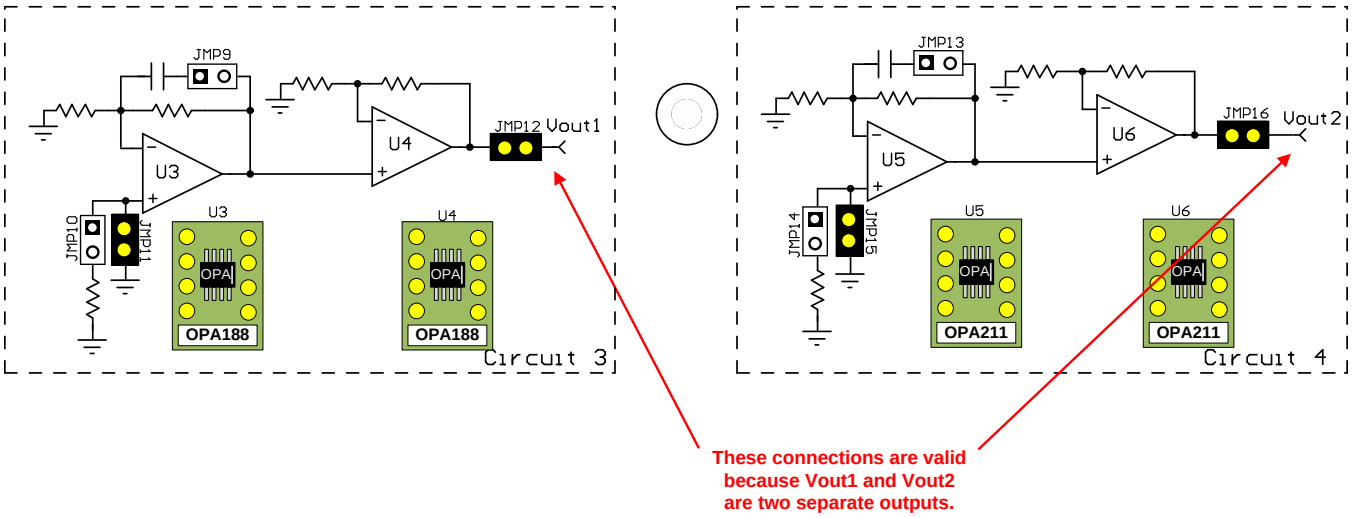

Figure 7. Correct Connection: Outputs are Connected to Separate BNC Connectors

4 Schematic, PCB Layout, and Bill of Materials

This section contains the complete bill of materials and schematic diagram for the TI-PLABS-AMP-EVM. Each schematic provides details explaining the operation of the circuit.

4.1 Schematics

4.1.1 Circuit 1: Noninverting Amplifier

Figure 8 shows the schematic for circuit 1, the noninverting amplifier. The gain of this circuit is 11 V/V when JMP2 is installed, and 101 V/V when JMP1 is installed. JMP3 and JMP4 connect the input and output to BNC connectors.

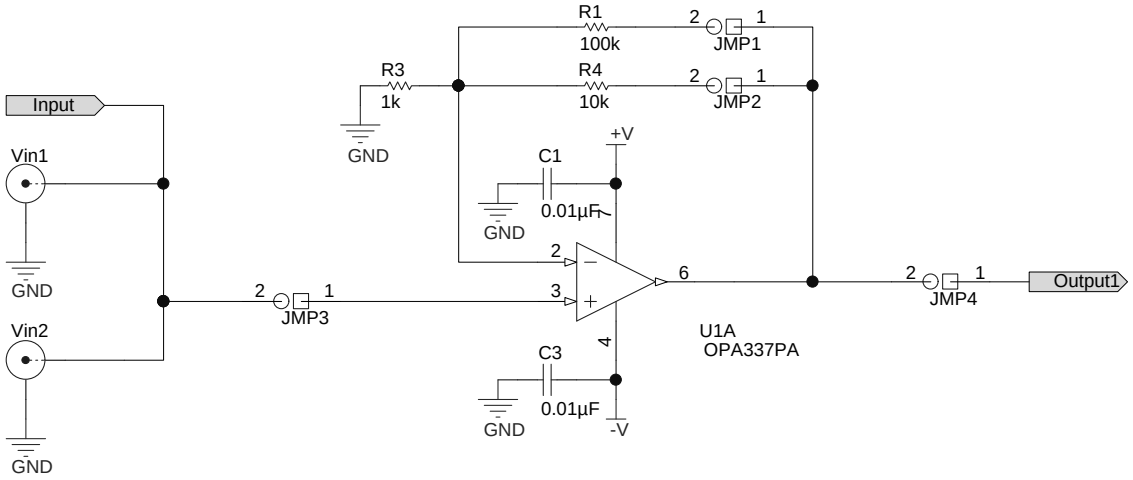

Figure 8. Circuit 1: Noninverting Amplifier

4.1.2 Circuit 2: Inverting Amplifier

Figure 9 shows the schematic for circuit 2, the inverting amplifier. The gain of this circuit is –20 V/V when JMP6 is installed, and –1 V/V when JMP5 is installed. JMP7 and JMP8 connect the input and output to BNC connectors.

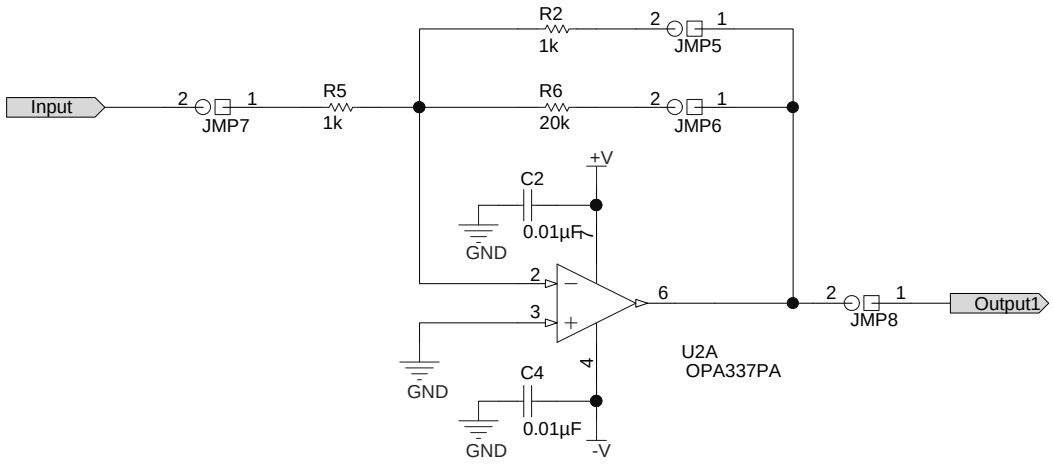

Figure 9. Circuit 2: Inverting Amplifier

4.1.3 Circuit 3 and Circuit 4: Cascaded Amplifiers

Figure 10 shows the schematic for circuit 3, cascaded amplifier 1. Figure 11 shows the schematic for circuit 4, cascaded amplifier 2.These circuits are used in noise and offset experiments because the high gain amplifies the noise and offset signal to a level that a standard scope or DMM can easily measure. The total gain for each circuit is 2121 V/V (gain = 101 × 21 = 2121). Circuit 3 and circuit 4 are identical so that the noise from two different amplifiers are compared. Note that the output of circuit 3 is connected to Vout1, and the output of circuit 4 is connected to Vout2.

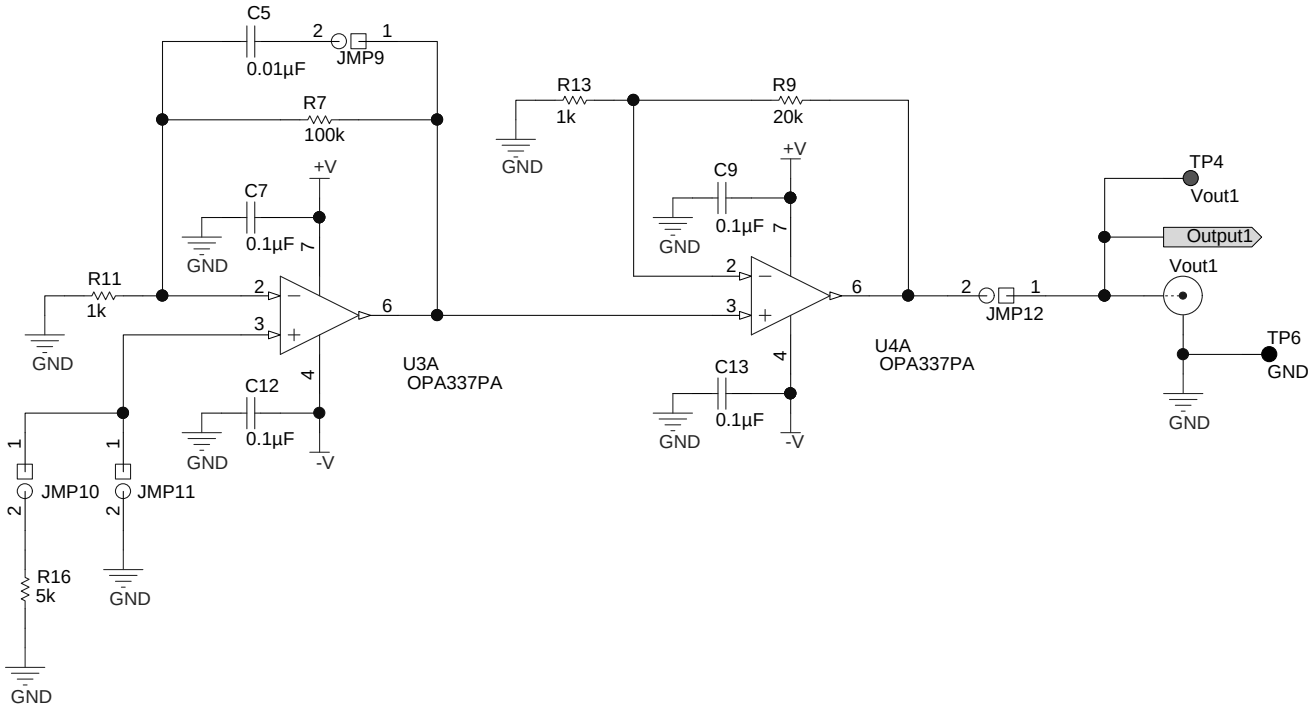

Figure 10. Circuit 3: Cascaded Amplifier 1

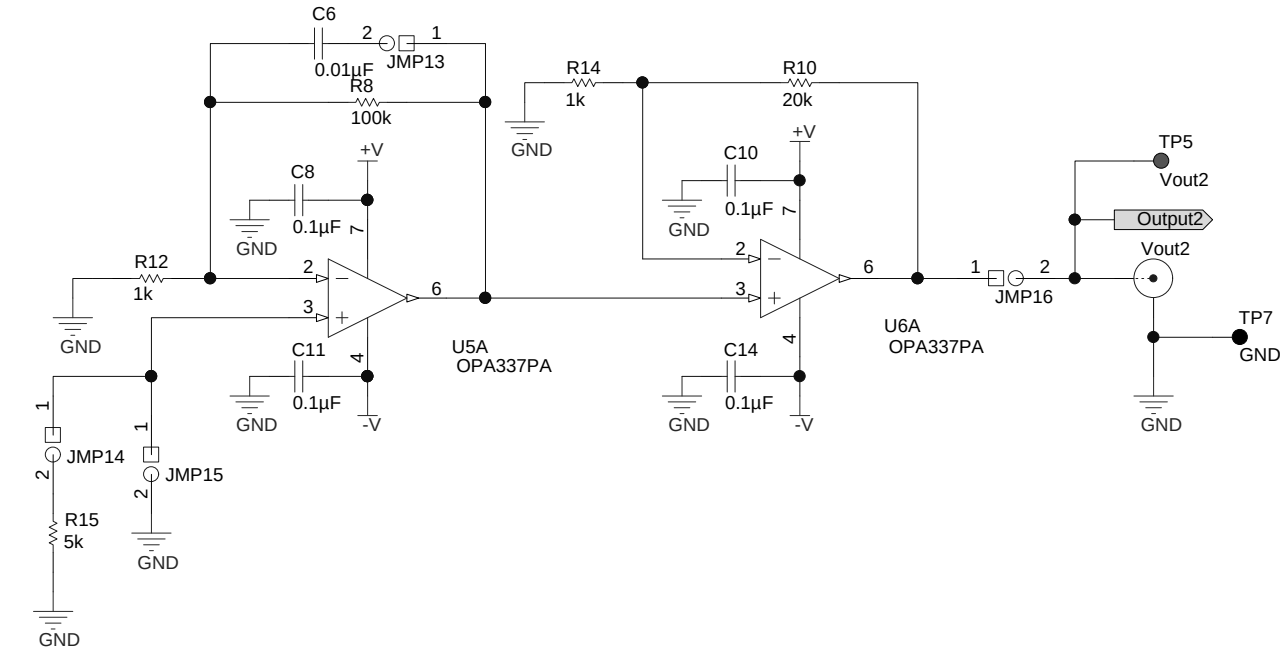

Figure 11. Circuit 4: Cascaded Amplifier 2

4.1.4 Circuit 5: Riso Stability Circuit

Figure 12 shows the schematic for circuit 5, the Riso stability circuit. This circuit shows how an isolation resistance is used to stabilize circuits with capacitive loads.

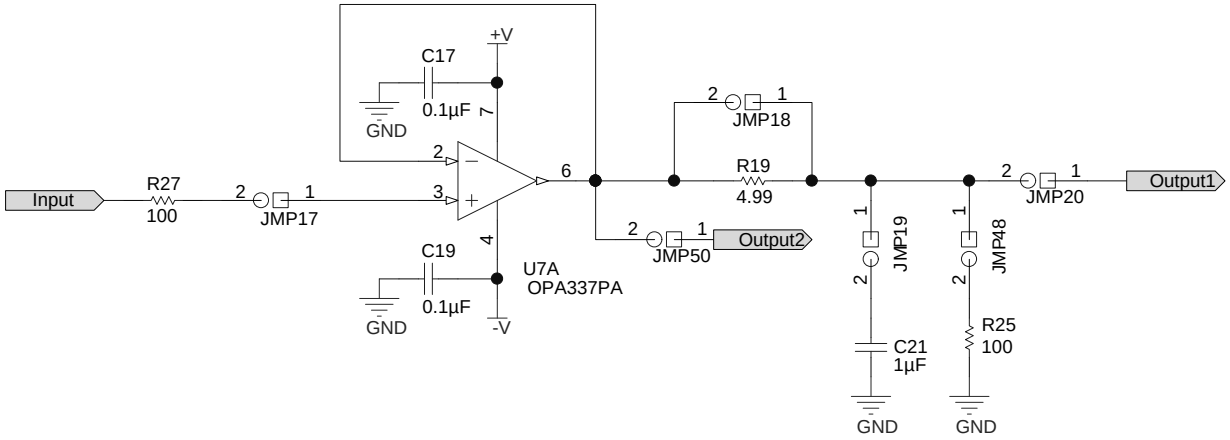

Figure 12. Circuit 5: Riso Stability Circuit

4.1.5 Circuit 6: Riso Dual-Feedback Stability Circuit

Figure 13 shows the schematic for circuit 6, the Riso dual-feedback stability circuit. This circuit shows how this circuit topology is used to stabilize circuits with capacitive load.

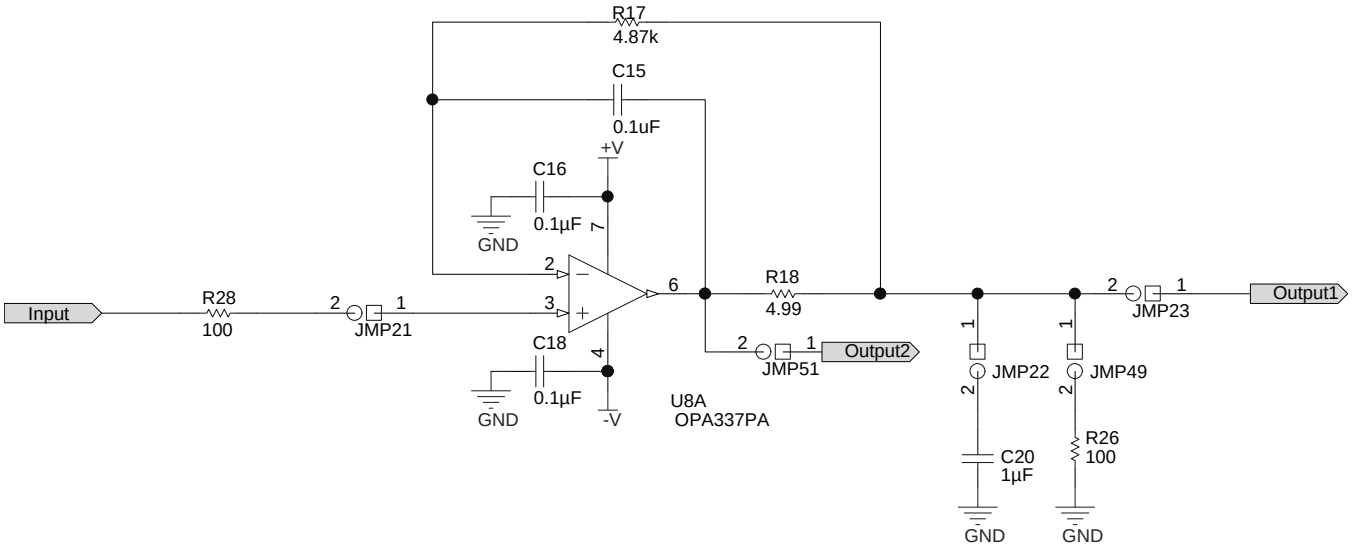

Figure 13. Circuit 6: Riso Dual-Feedback Stability Circuit

4.1.6 Circuit 7: Multiple-Feedback LPF

Figure 14 shows circuit 7, the multiple-feedback low-pass filter (LPF).

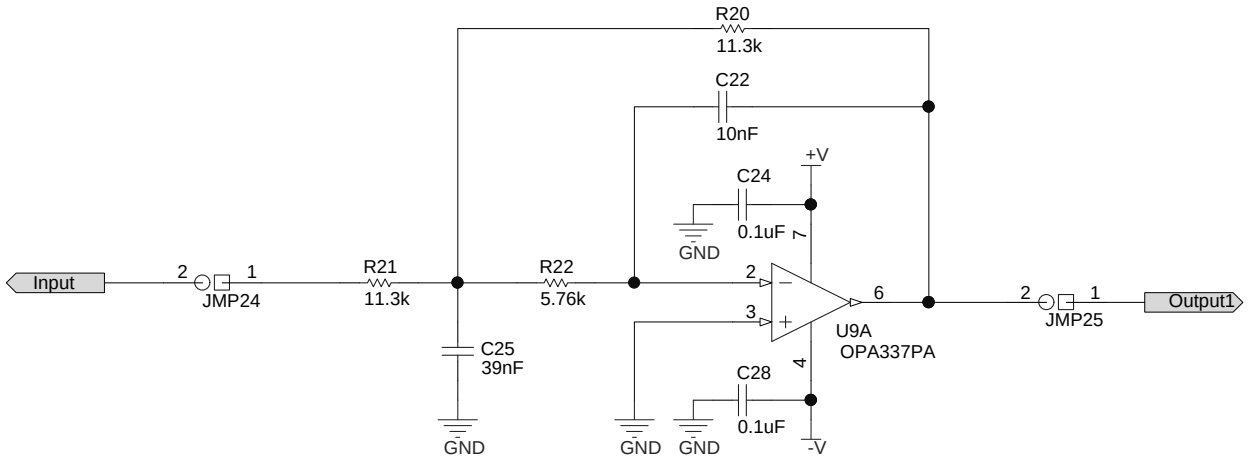

Figure 14. Circuit 7: Multiple-Feedback LPF

4.1.7 Circuit 8: Sallen-Key LPF

Figure 15 shows circuit 8, the Sallen-Key LPF.

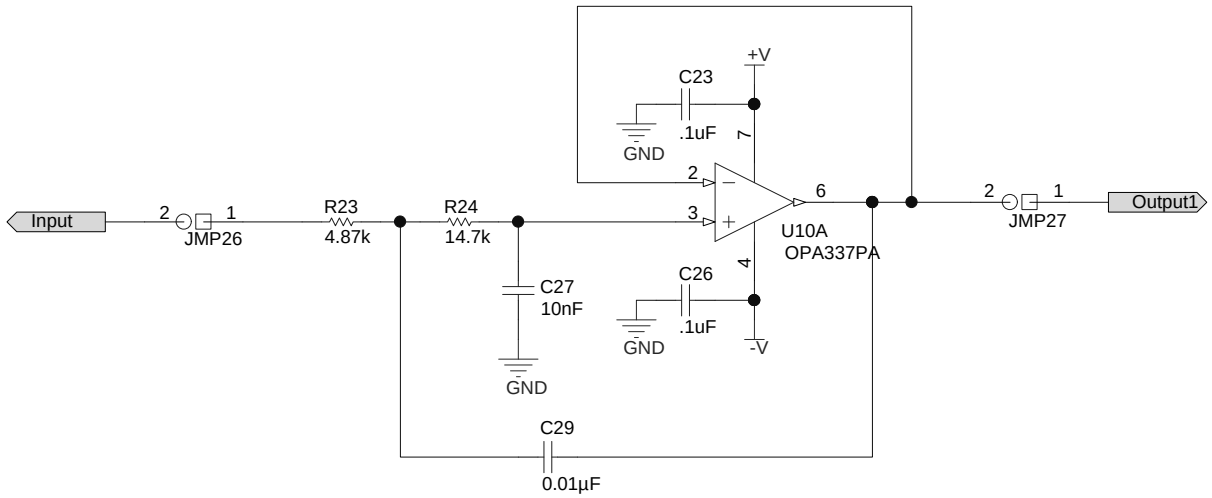

Figure 15. Circuit 8: Sallen-Key LPF

4.2 PCB Layout

Figure 16 shows the layout of the overview for the TI-PLABS-AMP-EVM board. The board is designed so that the silkscreen shows the schematic of the key sections of the board. Jumper placement is incorporated into the silk screen so that circuit configuration is intuitive.

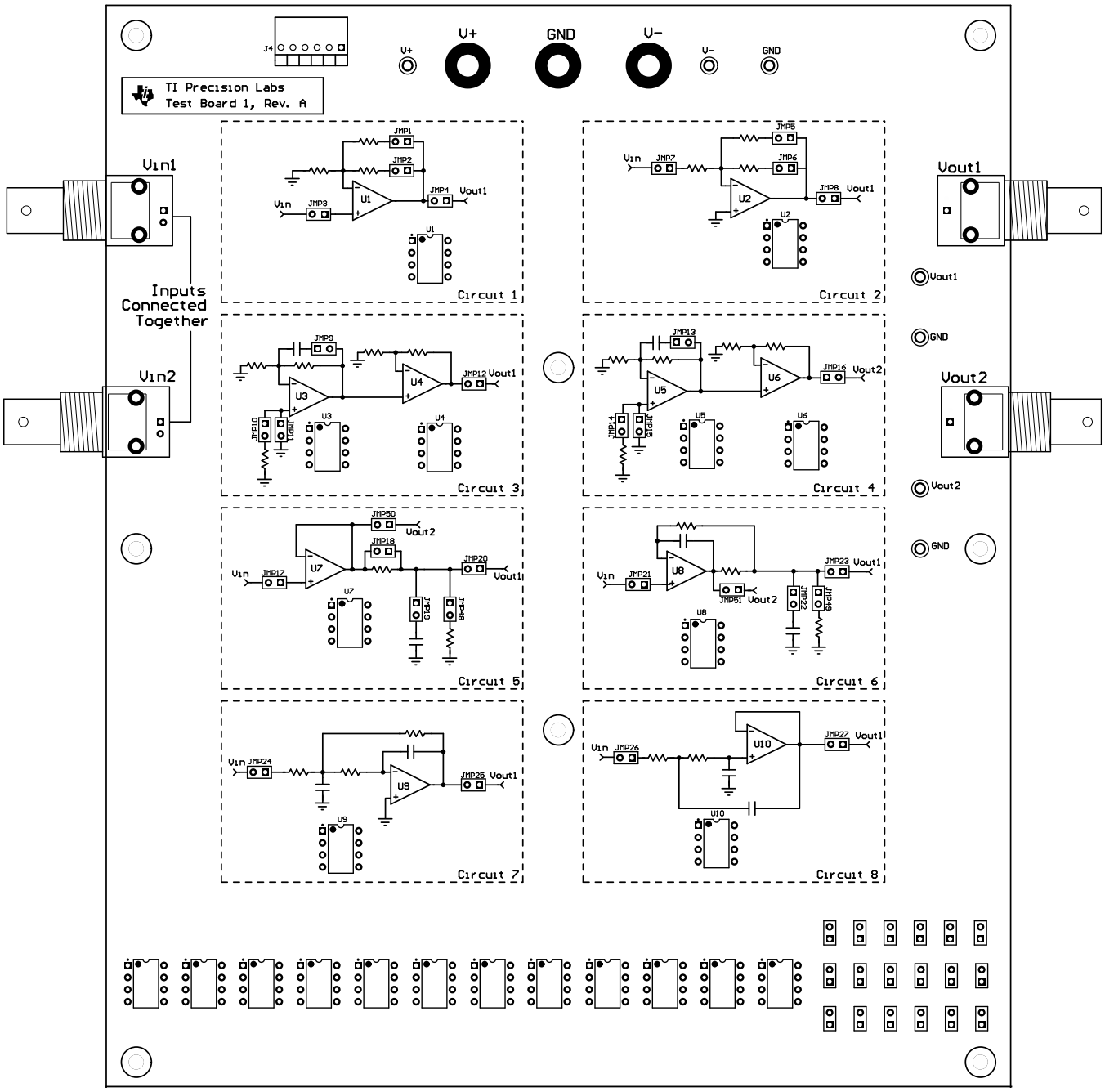

Figure 16. PCB Components Layout

4.3 TI-PLABS-AMP-EVM Bill of Materials

Table 3 lists the bill of materials for the TI-PLABS-AMP-EVM PCB.

Table 3. Bill of Materials

Qty	Designator	Description	Manufacturer	Manufacturer Part Number	Digikey Part Number
2	C20, C21	2.2nF	TDK Corporation	C2012C0G1H222J060AA	445-7507-1-ND
20	C1–C4, C7–C14, C16–C19, C23, C24, C26, C28	0.1µF	Kemet	C0805C104K5RACTU	399-1170-1-ND
4	C5, C6, C22, C27	1nF, CAP CER 1000PF 50V 5% NP0 0805	Kemet	C0805C102J5GACTU	399-1136-2-ND
1	C15	150pF	Kemet	C0805C151K5RACTU	399-9176-1-ND
2	C30, C31	CAP, TANT, 10µF, 20V, ±20%, 1 Ω, 3528-21 SMD	AVX	TPSB106M020R1000	478-4087-1-ND
1	C25	3.9nF, CAP CER 3900PF 50V 5% C0G 0805	TDK Corporation	C2012C0G1H392J060AA	445-7510-2-ND
1	C29	2nF, CAP CER 2000PF 50V 5% NP0 0805	Murata Electronics North America	GRM2165C1H202JA01D	490-1627-1-ND
2	D1, D2	Diode, TVS, Uni, 28V, 1500W, SMC	Diodes Inc	SMCJ28A-13-F	SMCJ28A-FDICT-ND
3	GND, V+, V-	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
8	H1–H8	STANDOFF HEX 4-40THR ALUM 1/2 "L	Keystone	2203	2203K-ND
8	H1–H8	MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	H703-ND
1	J4	2.5 WTB HEADER RA W/KINK 6CKT	Molex	534260610	WM3425-ND
1	J4-A	2.5MM CRIMP HOUSING POS LOCK 6CI	Molex	511030600	WM9191-ND
6	J4-1–J4-6	CONN TERM RCPT 22-28AWG CRIMP	Molex	503518000	WM3320CT-ND
49	Jumpers all	CONN HEADER 2POS 0.100" SGL GOLD	Samtec	TSW-102-07-G-S	SAM1029-02-ND
9	R2, R3, R5, R11–R14, R25, R26	RES 1kΩ 1/8W 1% 0805 SMD	Yageo	RC0805FR-071KL	311-1.00KCRCT-ND
11	R27–R37	RES 100 Ω 1/8W 1% 0805 SMD	Yageo	RC0805FR-07100RL	311-100CRCT-ND
2	R4, R38	RES 10kΩM 1/8W 1% 0805 SMD	Yageo	RC0805FR-0710KL	311-10.0KCRCT-ND
3	R6, R9, R10	RES 20kΩ 1/8W 1% 0805 SMD	Yageo	RC0805FR-0720KL	311-20.0KCRCT-ND
3	R1, R7, R8	RES 100kΩ 1/8W 1% 0805 SMD	Yageo	RC0805FR-07100KL	311-100KCRCT-ND
2	R15, R16	RES 4.99kΩ 1/8W 1% 0805 SMD	Yageo	RC0805FR-074K99L	311-4.99KCRCT-ND
2	R18, R19	RES 787 Ω 1/8W 1% 0805 SMD	Yageo	RC0805FR-07787RL	311-787CRCT-ND
1	R17	RES 78.7kΩ 1/8W 1% 0805 SMD	Yageo	RC0805FR-0778K7L	311-78.7KCRCT-ND
4	R20–R24	RES 2.26kΩ 1/8W 1% 0805 SMD	Panasonic Electronic Components	ERJ-6ENF2261V	P2.26KCTR-ND
1	R22	RES 1.13kΩ 1/8W 1% 0805 SMD	Panasonic Electronic Components	ERJ-6ENF1131V	P1.13KCCT-ND
3	TP1, TP4, TP5	TEST POINT PC COMPACT 0.063"D RED	Keystone	5005	5005K-ND
3	TP2, TP6, TP7	TEST POINT PC COMPACT 0.063"D BLK	Keystone	5006	5006K-ND
1	TP3	TEST POINT PC COMPACT 0.063"D YLW	Keystone	5009	5009K-ND
22	U1–U18, U21–U24	IC SOCKET 8PIN MS TIN/TIN 0.300	Mill-Max	110-44-308-41-001000	ED90048-ND
4	Vin1, Vin2, Vout1, Vout2	CONN BNC JACK R/A 50 Ω PCB	TE Connectivity	1-1634612-0	A97555-ND
20		Shunt, LP W/Handle 2 pos	TE Connectivity	881545-2	A26242-ND
1	N/A	HOOK-UP STRND 24AWG RED 100'	General Cable/Carol Brand	C2015A.12.03	C2015R-100-ND
1	N/A	HOOK-UP STRND 24AWG BLACK 100'	General Cable/Carol Brand	C2015A.12.01	C2015B-100-ND
1	N/A	HOOK-UP STRND 24AWG YELLOW 100'	General Cable/Carol Brand	C2015A.12.05	C2015Y-100-ND
7	N/A	DIP Adapter boards, assembled and labeled as per DIP Adapter build files	N/A	N/A	N/A
3	N/A	Terminal Strip, 32 position	Samtec	TS-132-G-AA	N/A
2	N/A	IC, OPAMP 8-SOIC	Texas Instruments	OPA211AIDR	
2	N/A	IC, OPAMP 8-SOIC	Texas Instruments	OPA188AIDR	
1	N/A	IC, OPAMP 8-SOIC	Texas Instruments	OPA277UA	

Revision History

Changes from Original (January 2015) to A Revision	Page
• Changed *Precision-Labs-EVM* to *TI-PLABS-AMP-EVM* throughout document	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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