User's Guide

ADC32RF5xEVM User Guide

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1 Overview

The ADC32RF5xEVM is an evaluation module (EVM) designed to evaluate the ADC32RF5x family of high-speed, JESD204B interface ADCs. The EVM includes an onboard clocking solution (LMK04832), transformer-coupled analog inputs, full power solution, and easy-to-use software GUI and USB interface. The following features apply to this EVM:

- Transformer-coupled signal input network allowing a single-ended signal source from 30 MHz to 3000 MHz.
- LMK04832 system clock generator that generates field-programmable gate array (FPGA) reference clocks for the high-speed serial interface.

The ADC32RF5xEVM is designed to work seamlessly with TI's TSW14J58 EVM JESD204B/C data capture/ pattern generator card, through the High Speed Data Converter Pro (HSDC Pro) software tool for high-speed data converter evaluation. It is also designed to work with many of the developments kits from leading FPGA vendors that contain an FMC or FMC+ connector.

1.1 Required Hardware

The following is **included** in the EVM evaluation kit:

- ADC32RF5x evaluation board (EVM)
- Power supply cable
- USB 2.0 TypeA to Mini-B cable

The following list of equipment are items that are **not included** in the EVM evaluation kit, but are required items (in order to achieve the best performance) for the evaluation of this product:

- TSW14J58 EVM data capture board
- 6-V, 5-A power supply
- 12-V, 2-A power supply
- USB 2.0 TypeA to Mini-B cable
- USB 3.0 TypeA to Micro-B cable
- Low-noise signal generator (qty. 2) (Examples: HP HP8644B, Rohde & Schwarz SMA100A)
- Bandpass filter for clock input
- Bandpass filter for desired analog input
- High quality signal path cables

1.2 Required Software

The following software is required to operate the ADC32RF5x EVM and is available online. See the References section for links.

- ADC32RF5x EVM GUI

The following software is required to operate the TSW14J58 EVM and is available online. See the References section for links.

- High Speed Data Converter Pro, version 5.2 or higher

1.3 Evaluation Board Feature Identification

The EVM features are shown in Figure 1-1 .

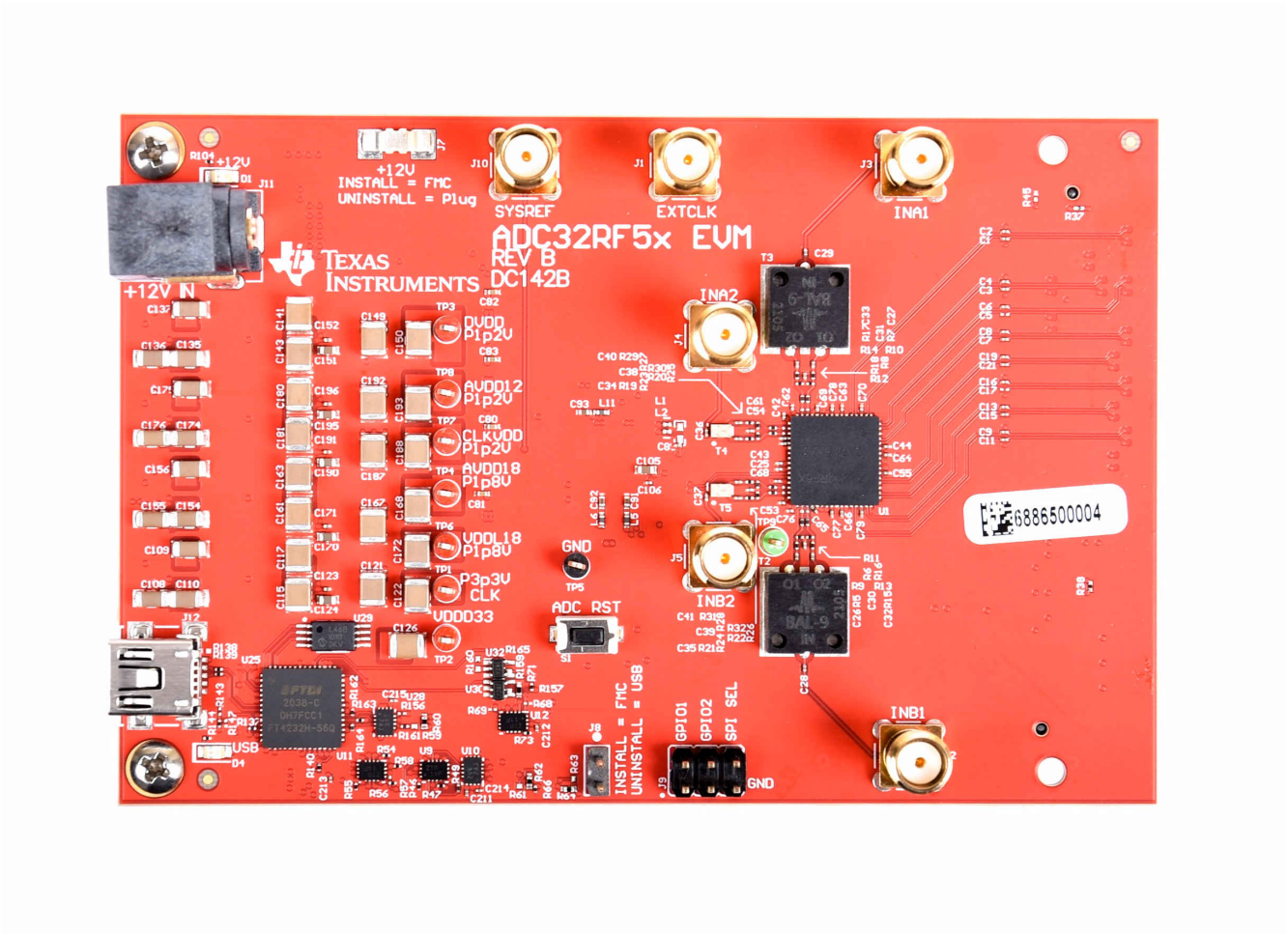

Figure 1-1. EVM Features

2 Quick Start Guide

The EVM test procedure to obtain a valid data capture from the ADC32RF5xEVM using the TSW14J58EVM data capture board is provided in this section. This is the starting point for all evaluations.

2.1 Introduction

The ADC32RF5xEVM includes the ADC32RF5x analog-to-digital converter with JESD204B interface, LMK04832 clocking chip, and an FMC connector suitable for connection to readily-available FPGA development boards or to the TSW14J58EVM data capture board.

The FPGA on the capture card requires a device clock and SYSREF signal, the LMK04832 clock device supplies these signals to the FMC connector for that purpose, as well as supplying SYSREF to the ADC.

This document conveys all information needed to bring up both the ADC32RF5xEVM and TSW14J58EVM data capture board, and get a valid data capture with good FFT results.

The JESD204B interface requires a number of important parameters to be decided in advance of setting up the data link, such as; number of lanes, number of converters, number of samples per frame, and a value K number of frames per multi-frame, among other parameters. Both sides of a JESD204B link must be set up with the same values for all these parameters, or else the FPGA that receives the data is not able to establish a synchronized link.

Note

Getting these parameters inconsistent between ADC and FPGA is perhaps the biggest single reason for an EVM setup to not function as expected.

The GUI installers that come with the ADC32RF5x and the TSW14J58EVM come with configuration files that are meant to enable quick initial setup of a number of basic configurations. TI **strongly** suggests setting up the EVM and data capture board with a configuration described in this document and getting a working setup before modifying the configuration to be closer to what the end-application requires. In this way, the user can know that the hardware is functioning and that there is a working configuration that they can go back to in the event of difficulty developing their own configuration.

This document introduces the software that must be installed on a PC, and presents a basic setup for the Bypass and DDC modes available in the ADC32RF5xEVM. The operating modes explained in this document are:

- **Bypass Mode**
  - **2x Averaging**
- **DDC (Decimation)**
  - **8x complex decimation**
  - **128x complex decimation**

2.2 Software Setup

The proper software must be installed before beginning evaluation. See *Required Software* for a list of the required software. To avoid potential issues, the software should be installed before connecting the ADC32RF5xEVM and TSW14J58EVM to the computer for the first time. Appendix A.1 contains links to find the software on the TI website.

2.2.1 ADC32RF5xEVM GUI Installation

1. Download the GUI installer from the EVM tool folder at https://www.ti.com/tool/ADC32RF54EVM
2. Extract the installation files from the downloaded zip file.
3. Run *TI-ADC32RF5x.exe* and follow the procedure of the installer to complete installation.

2.2.2 High Speed Data Converter Pro GUI Installation

High Speed Data Converter Pro GUI (HSDC Pro) is used to control the TSW14J58EVM and analyze the captured data. Please see the HSDC Pro GUI user's guide (SLWU087) for more information.

1. Download HSDC Pro GUI installer.
2. Extract the installation files from the downloaded zip file.

3. Run *setup.exe* and follow the installation prompts to complete installation.

2.3 Hardware Setup

A typical test setup using the ADC32RF5xEVM and TSW14J58EVM is shown in Figure 2-1.

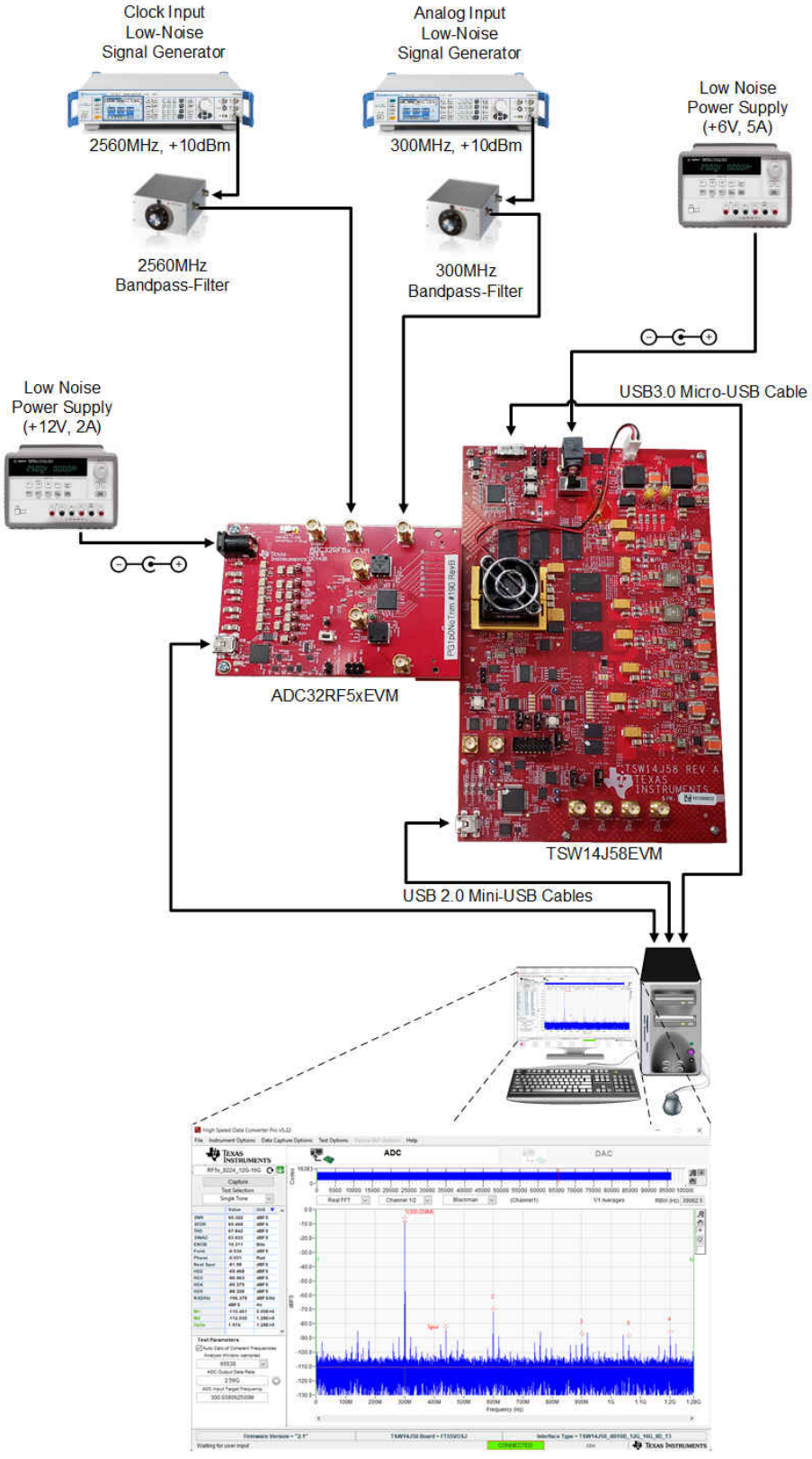

Figure 2-1. ADC32RF5xEVM Bench Setup Block Diagram

3 Quick Start Procedure for Bypass Mode

Bypass mode is the default operating mode for the ADC32RF5x device family. When operating in this mode, the digital decimation filters that the ADC32RF5x offers is bypassed. Additionally, the user has the option to enable averaging of each internal pair of ADCs per individual channel. Operating in bypass mode without averaging provides the lowest power consumption for ADC32RF5x devices.

TSW14J58EVM

1. Connect the ADC32RF5xEVM to the TSW14J58EVM using the FMC connectors.
2. Connect a 6V, 5A minimum power supply to connector J2.
3. Connect a USB 2.0 TypeA to Mini-B cable to connector J23.
4. Connect a USB 3.0 TypeA to Micro-B cable to connector J1.
5. Turn on the power supply and toggle the power switch (SW5) to the "ON" position. The fan should start spinning and the current draw should settle around 2.1 A.

ADC32RF5xEVM

1. Connect a 12 V , 2 A minimum power supply to the connector J11.
2. Connect a USB 2.0 TypeA to Mini-B cable to connector J12.
3. Connect a filtered 2.56 GHz clock signal (**+10 dBm**) to input J1 (EXTCLK), then enable the signal generator output.
4. Connect a filtered 300 MHz input signal (**+10 dBm**) to input J3 (INA1), then enable the signal generator output.

GUI Setup

1. Open High Speed Data Converter Pro (HSDC Pro) and select the TSW14J58. If no device is found, verify that power is on and both USB cables are connected.
2. Select the device firmware labeled **ADC32RF5x_8224_12G-16G** and update the firmware by pressing **Yes** on the pop-up window and waiting for the **Downloading Firmware** message to finish.
3. Enter **2.56 G** into the ADC Output Data Rate field. A message will appear stating "*New lane rate is 12.8G due to ADC Output Data Rate change*". When this appears, press OK.
4. Enter **300 M** into the ADC Input Target Frequency field and tick the checkbox "*Auto Calculation of Coherent Frequencies*". You will notice that the 300M changes to 300.039 M.
5. Open the ADC32RF5x GUI. Verify that the green USB Status indicator is illuminated as shown in Figure 3-1 below. If the indicator is red (simulation mode), verify that the USB cable is connected and that the ADC32RF5xEVM is powered on and press the Reconnect USB button.

Figure 3-1. USB Status Indicator

3.1 2x Averaging in Bypass Mode

This mode uses internal averaging to provide better performance at the tradeoff of higher power consumption.

Procedure

1. In the bypass mode box of the GUI, ensure that the settings match those shown in Figure 3-2

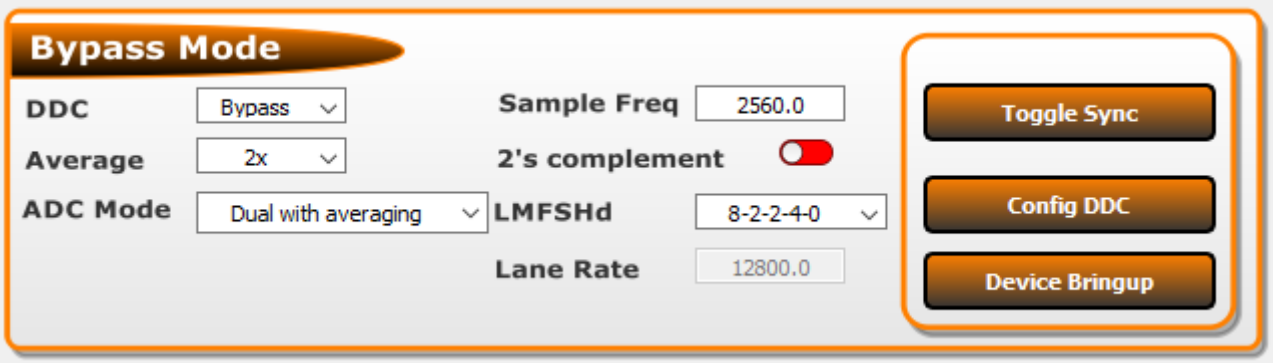

Figure 3-2. Bypass Mode Settings

2. Once these settings are verified, press the **Device Bringup** button.
3. Wait until after the message **Device Bringup Completed** appears in the Log.
4. Under the **Analog and Clock** tab, toggle **Dither Enable** to the **off** position.
5. In HSDC Pro, press the **Capture** button. You should now see something similar to Figure 3-3.
6. Adjust signal generator output such that the measured fundamental power in HSDC Pro is at the user's desired level. (shown below is -12 dBFs)

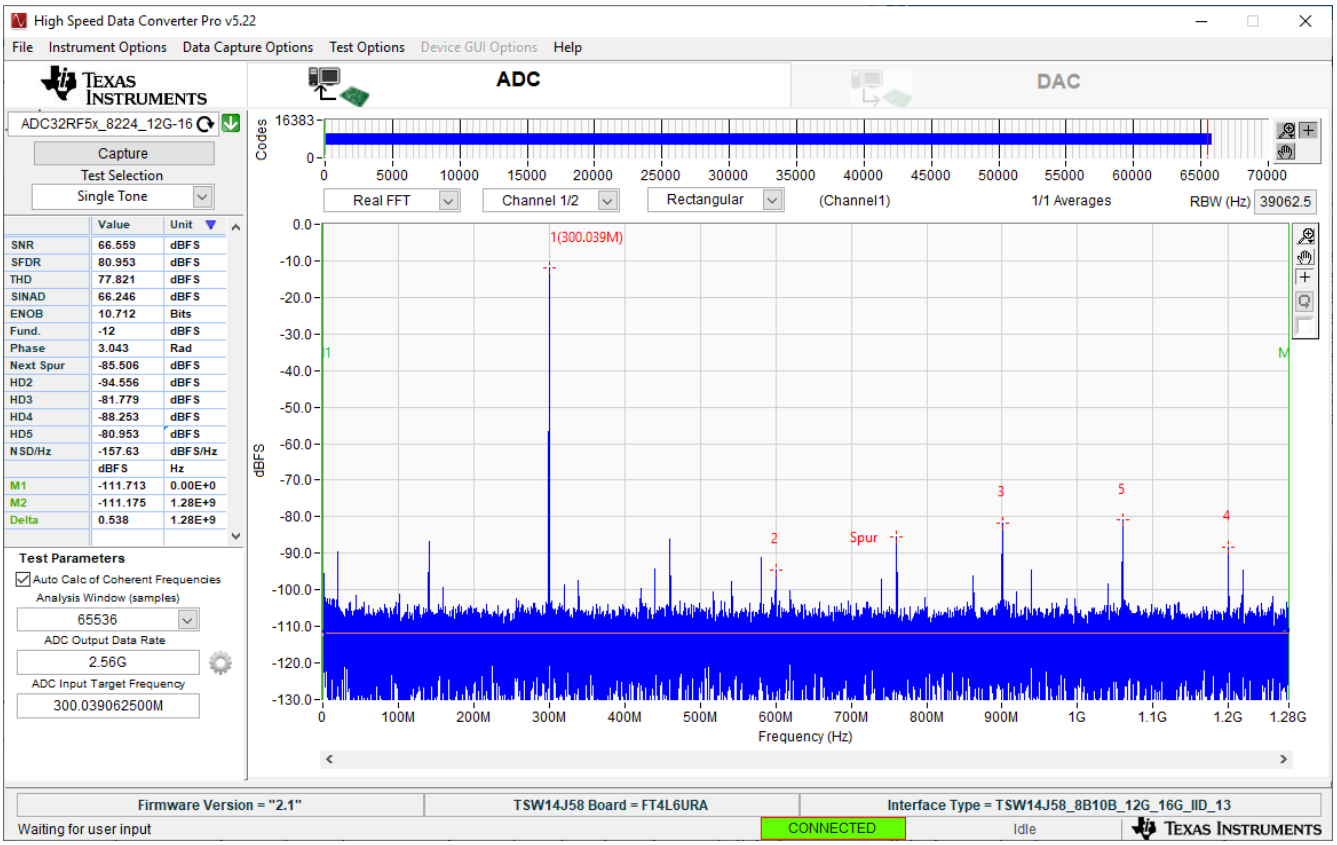

Figure 3-3. 300.039 MHz, bypass mode, 2x averaging, dither off

4 Quick Start Procedure for Complex Decimation Mode

The ADC32RF5x device family provides up to two digital down converters (DDC) per ADC channel supporting a wide range of instantaneous bandwidth IBW coverage - from single wide band mode with 8x complex decimation to up to two narrow band channels with as high as 128x complex decimation.

When operating in complex decimation mode, the appropriate NCO is used as an intermediate frequency to the complex mixer. Similar to the bypass operating mode, the user has the option to enable averaging of each internal pair of ADCs. This section will provide two example configurations for operating the ADC32RF5xEVM in 8x and 128x decimation modes.

4.1 8x Complex Decimation

This example uses a coherent 790 MHz input on the channel A input with the ADC in a 1x averaging mode with dither enabled.

Procedure

1. In the **Bypass Mode** box, use the DDC dropdown to change to **Complex Mode**. The usser will notice the box title changes to **Complex Mode** to reflect the current DDC operating mode.
2. Use the **Decimation** dropdown to change the decimation to **8**.
3. Set the **LMFSHd** setting to **4-4-2-1-0.**
4. Set the channel INA1 **NCO0** and **NCO1** to 800 (MHz).
5. Change **LMK divider** from 8 to 16.
6. Once these settings are verified and match Figure 4-1, press the **Device Bringup** button.

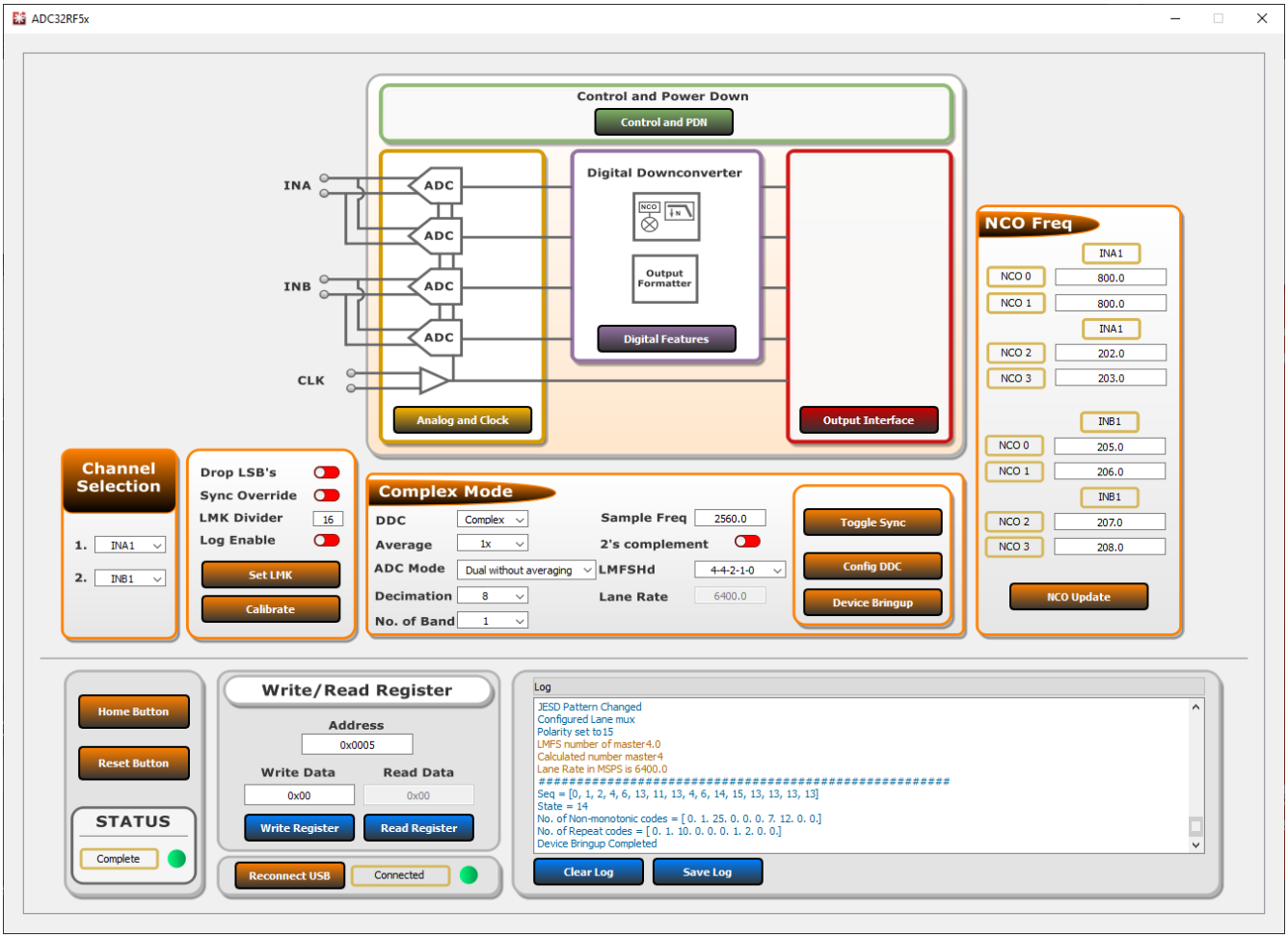

Figure 4-1. ADC32RF5xEVM GUI, 8x complex decimation, 800 MHz NCO

7. Wait until after the message **Device Bringup Completed** appears in the Log.

8. In HSDC Pro, connect to the TSW14J58EVM and select **ADC32RF5x_4421_6G-8G** as the INI file shown in Figure 4-2.

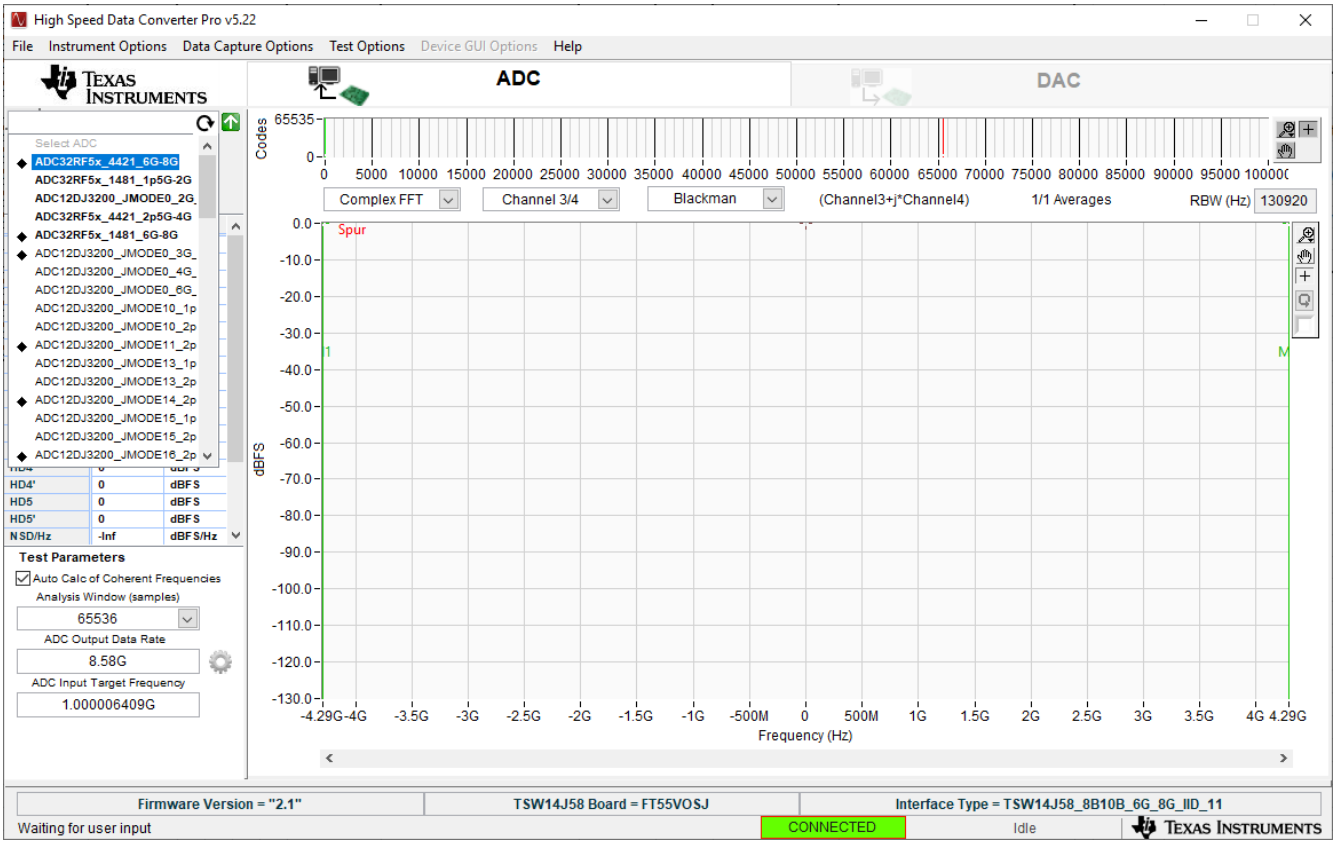

Figure 4-2. ADC32RF5x_4421_6G-8G INI file

9. Update the firmware by pressing **Yes** on the pop-up window and waiting for the **Downloading Firmware** message to finish.
10. Open the Additional Device Parameters menu by clicking on the gear next to the ADC Output Data Rate field.
11. Check the tickbox labeled "Enable?" and then enter the parameters shown in Figure 4-3.

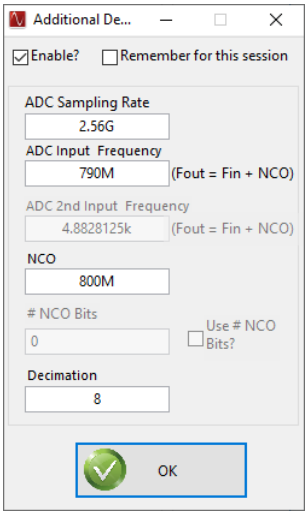

Figure 4-3. Additional Device Parameters , 8x complex decimation

12. Once completed, press OK.
13. Check the tickbox labeled **Auto Calculation of Coherent Frequencies** and you will see the **ADC Input Target Frequency** change from 790 M to the coherent frequency. Set the signal generator connected to channel A input to this coherent frequency.

14. Change the view window from **Real FFT** to **Complex FFT** and select channel 1/4.
15. Press the **Capture** button. You should now see something similar to Figure 4-4.
16. Adjust signal generator output such that the measured fundamental power in HSDC Pro is at the user's desired level.

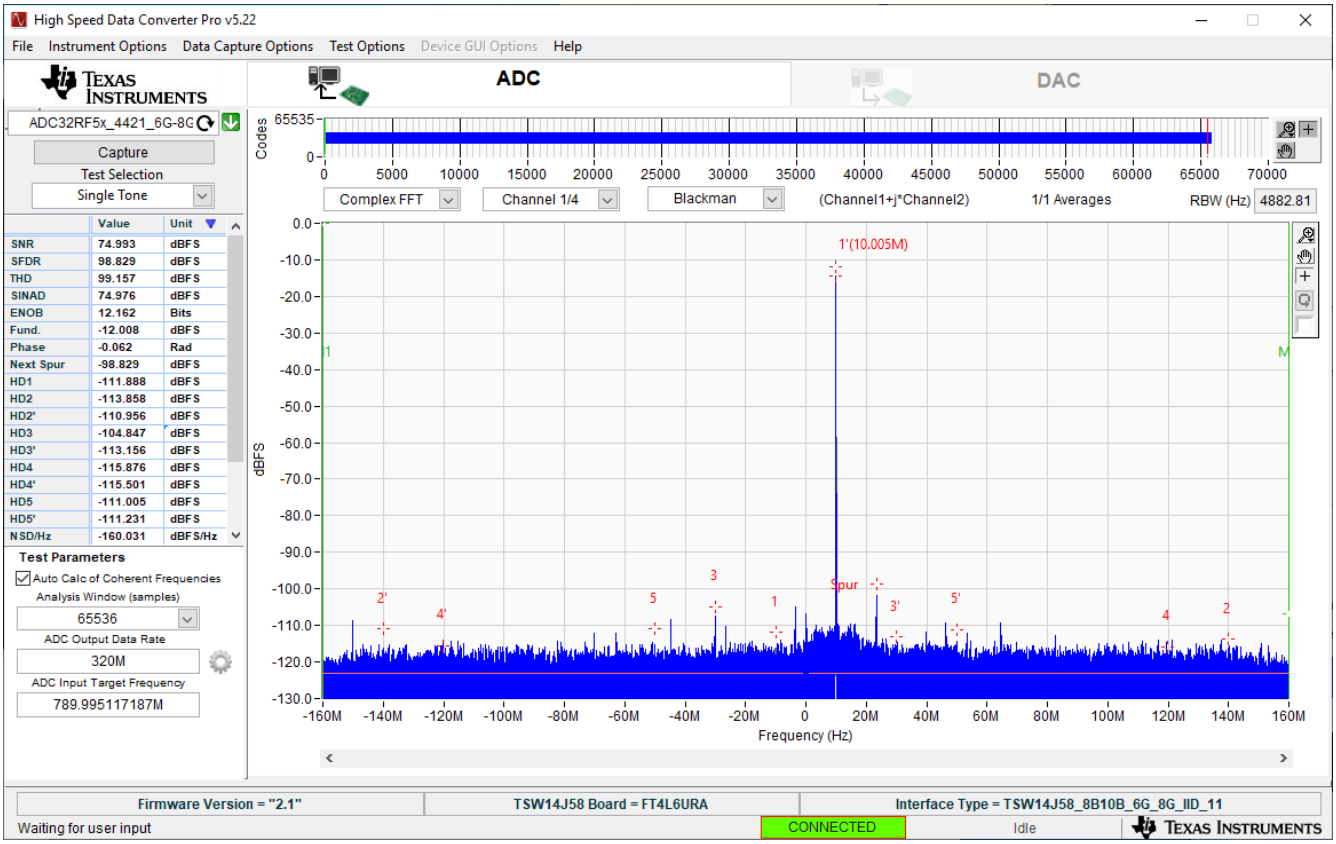

Figure 4-4. 789.995 MHz input, 8x complex decimation, 1x averaging, dither on

4.2 128x Complex Decimation

This example uses a coherent 1.003 GHz input on the channel B input with the ADC in a 2x averaging mode with dither enabled.

Procedure

1. Under the **Analog and Clock** tab, toggle **Dither Enable** to the on position and set **Dither Amplitude_1** to 3.
2. In the **Bypass Mode** box, use the DDC dropdown to change to **Complex Mode**. You will notice that the box title changes to **Complex Mode** to reflect the current DDC operating mode. Press the **Home Button** to change back to the home screen.
3. Set **Average** to **2x** and change **ADC Mode** to **Dual with averaging**.
4. Use the **Decimation** dropdown to change the decimation to **128**.
5. Set the **LMFSHd** setting to **1-4-8-1-0.**
6. Set the channel INB1 **NCO0** and **NCO1** to 1000 (MHz).
7. Change **LMK divider** from 8 to 32.
8. Once these settings are verified and match Figure 4-5, press the **Device Bringup** button.

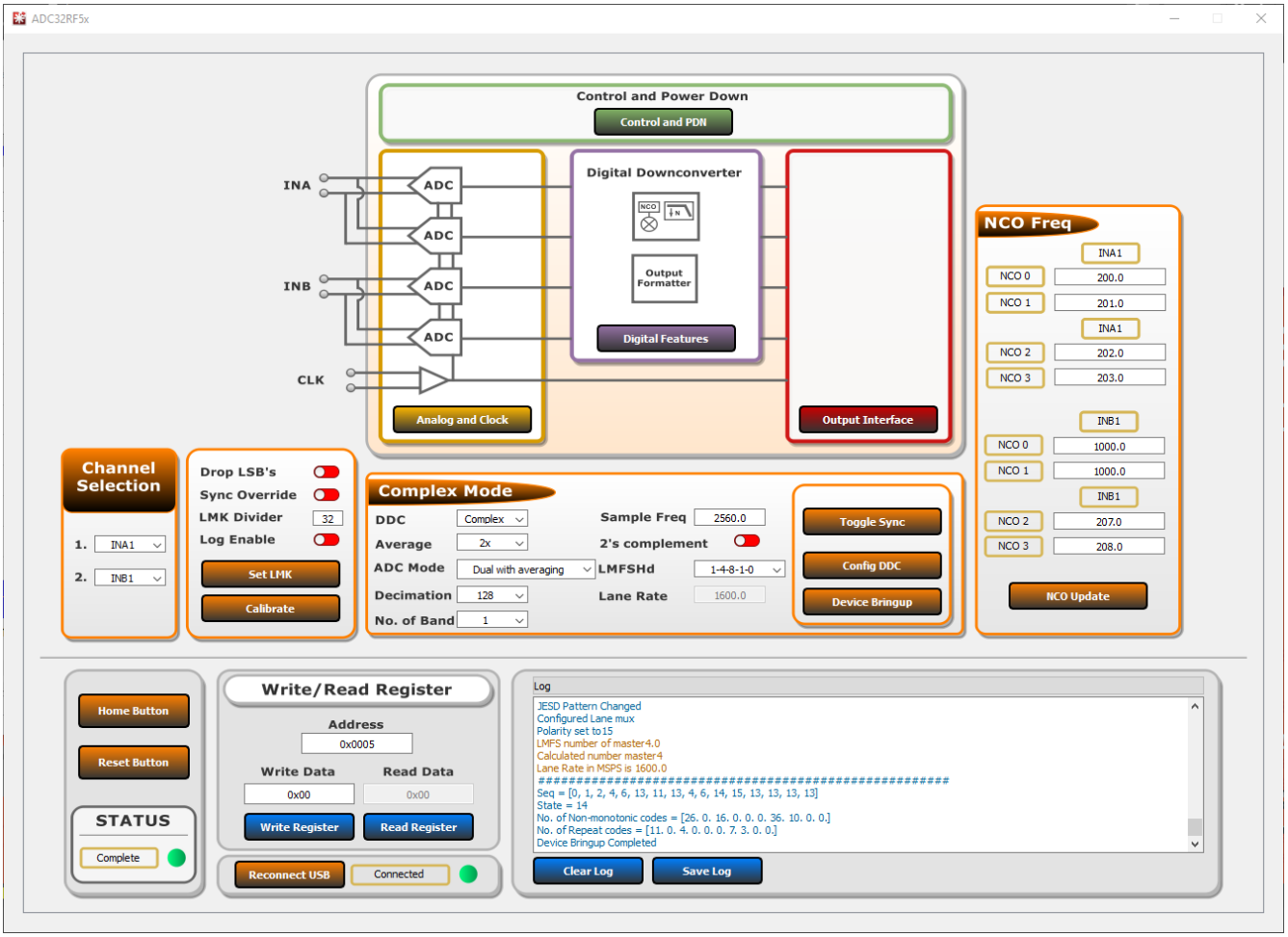

Figure 4-5. ADC32RF5xEVM GUI, 128x complex decimation, 1GHz NCO

9. Wait until after the message **Device Bringup Completed** appears in the Log.
10. In HSDC Pro, connect to the TSW14J58EVM and select **ADC32RF5x_1481_1p5G-2G** as the INI file shown in Figure 4-6 below.

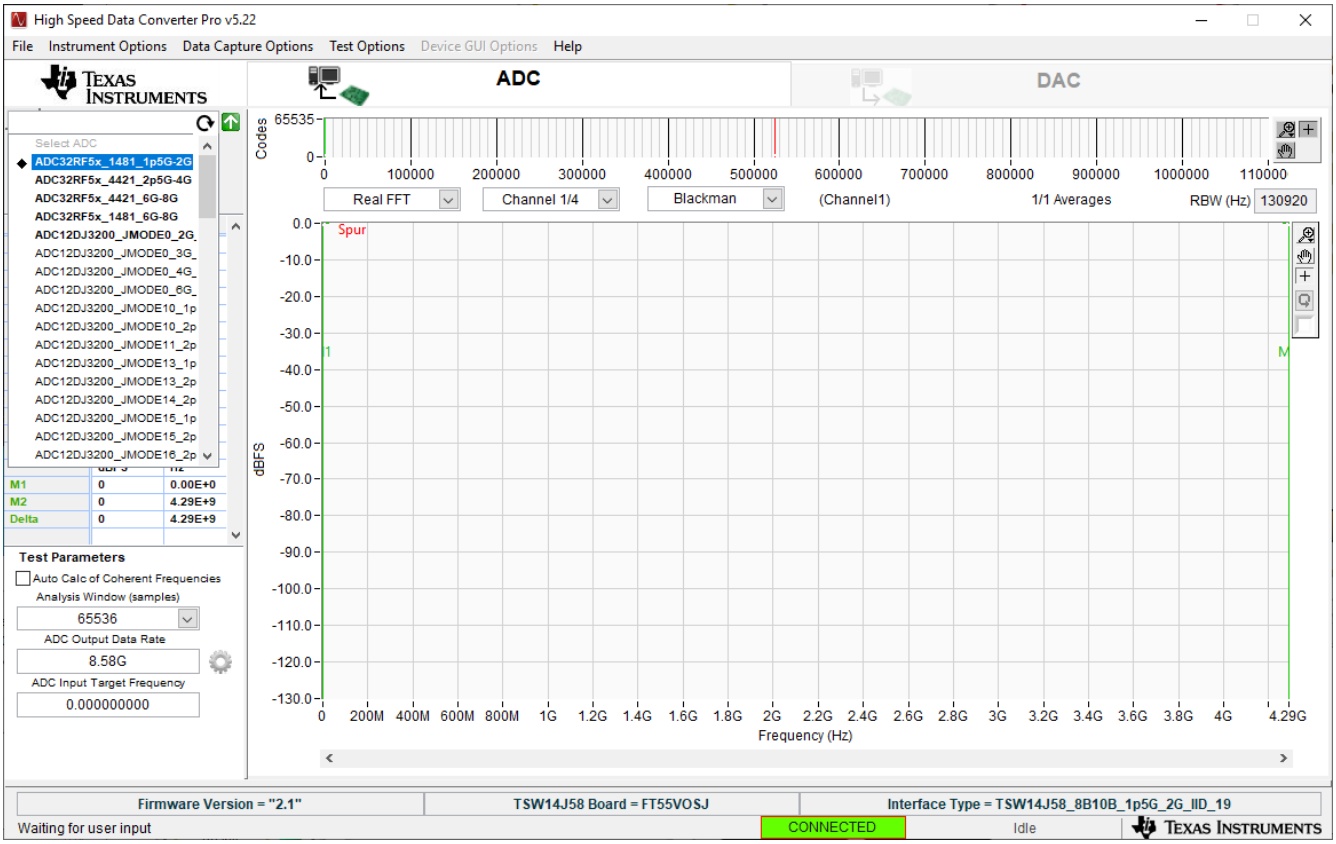

Figure 4-6. ADC32RF5x_1481_1p5G-2G INI file

11. Update the firmware by pressing **Yes** on the pop-up window and waiting for the **Downloading Firmware** message to finish.
12. Open the Additional Device Parameters menu by clicking on the gear next to the ADC Output Data Rate field.
13. Check the tickbox labeled "Enable?" and then enter the parameters shown in Figure 4-7 below.

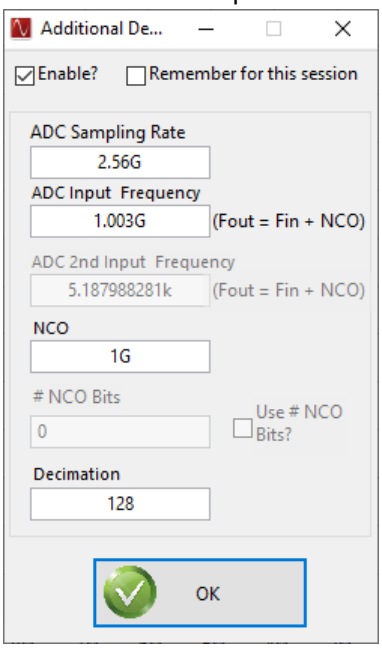

Figure 4-7. Additional Device Parameters , 128x complex decimation

14. Once completed, press OK.
15. Check the tickbox labeled **Auto Calculation of Coherent Frequencies** and the user will see the **ADC Input Target Frequency** change from 1.003G to the coherent frequency. Set the signal generator connected to the channel B input to this coherent frequency.
16. Change the view window from **Real FFT** to **Complex FFT** and select channel 3/4.
17. Press the **Capture** button. You should now see something similar to Figure 4-8.
18. Adjust signal generator output such that the measured fundamental power in HSDC Pro is at the user's desired level.

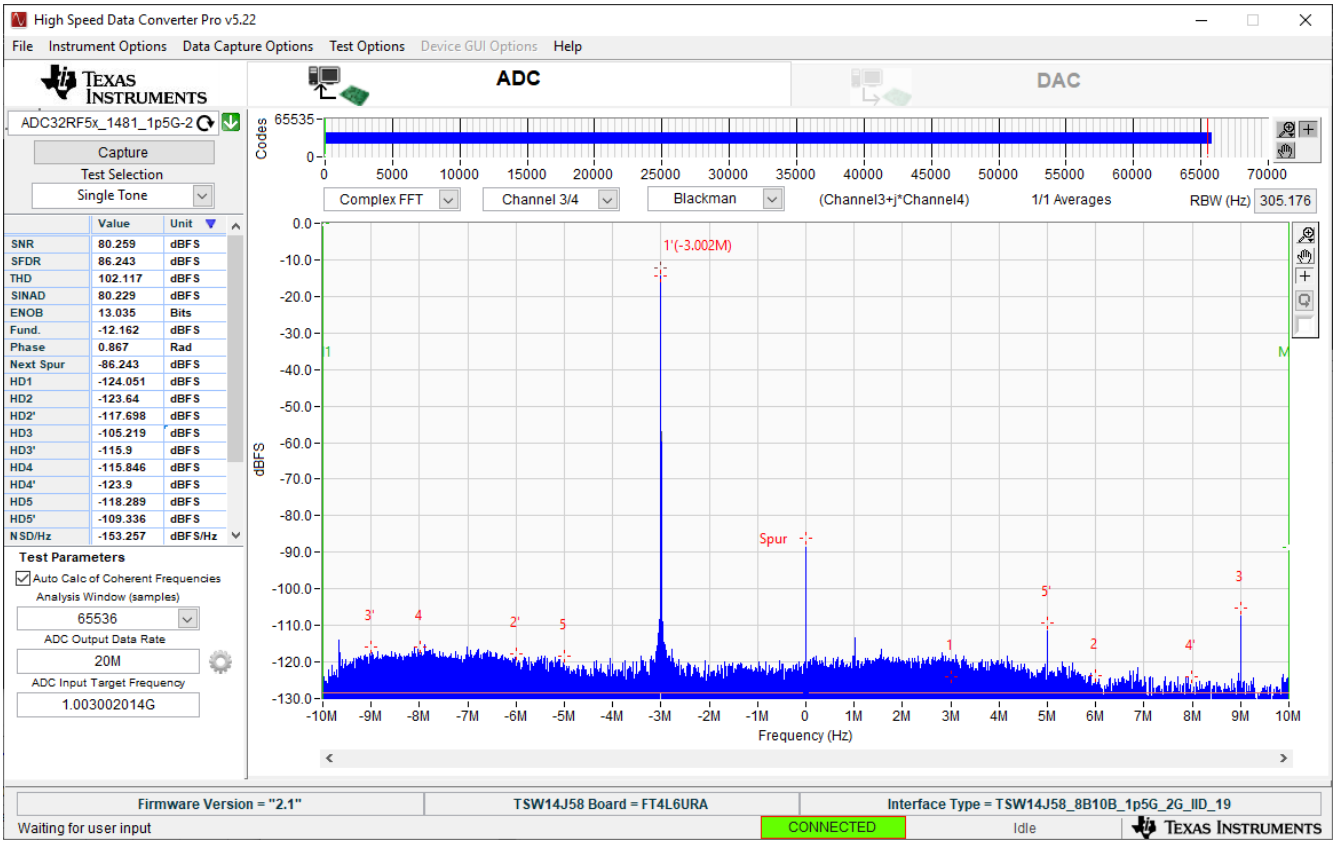

Figure 4-8. 1003.002 MHz input, 128x complex decimation, 2x averaging, dither amplitude 3

5 Operating Modes

This section covers the available operating modes available to users on the ADC32RF5xEVM.

CONFIGURATION	AVERAGING MODE	USABLE CHANNELS
Dual without averaging	1x	CHA1, CHB1
Dual with averaging	2x	CHA1, CHB1
	4x	CHA1 with CHA2 CHB1 with CHB2
Quad without averaging	1x	CHA1, CHA2, CHB1, CHB2
Quad with averaging	2x	CHA1, CHA2, CHB1, CHB2

5.1 Input Comparison

The following figure has been included to provide the user with a range of frequencies for the possible ADC32RF5xEVM averaging modes. For best performance, at input frequencies less than 800 MHz, it is recommended to use the outer inputs (AIN1 or BIN1) in either of the 1x or 2x averaging modes. At frequencies above 800 MHz, both of the inputs (inner vs outer) yield similar performance. The 4x averaging mode yields the best performance for frequencies above 700 MHz (due to phase imbalance between the different baluns at lower frequencies).

The outer channels (AIN1, BIN1) of this EVM evaluates a wideband balun (part number: BAL-0009) while the inner channels (AIN2, BIN2) on this EVM evaluates a *2nd nyquist zone* balun (part number: B0310J50100AHF). The frequency range for each of the 5 operating modes can be seen in Figure 5-1 (fundamental power set to -20 dBFs at each frequency).

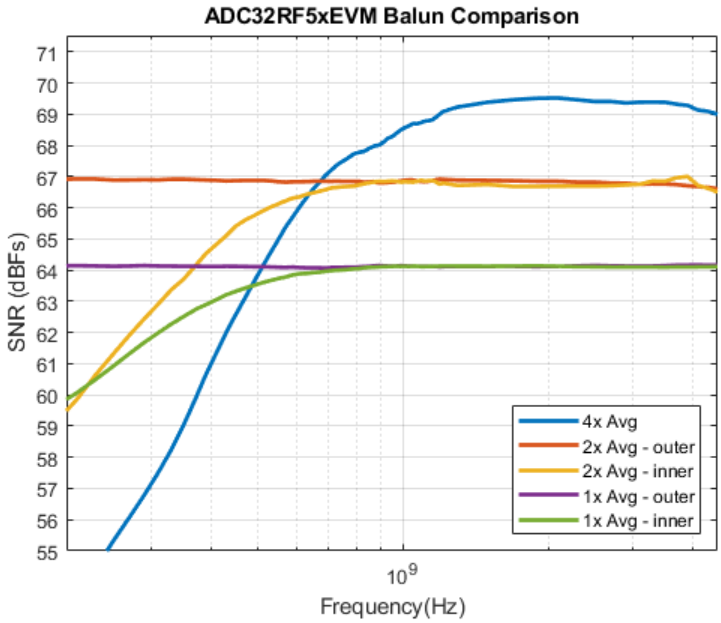

Figure 5-1. Balun Comparison

5.2 Quad ADC Mode

Programming into quad mode enables the functionality of the channel selection menu in the ADC32RF5xEVM GUI. This programming mode **must** be chosen when the user wants to capture using the inner inputs (INA2, INB2) in **1x** or **2x** averaging modes.

Note

Programming the ADC32RF54EVM into "Quad ADC" mode does not allow capture from 4 independent channels simultaneously as this is a dual channel ADC. When configured in this mode, the user can independently select the inputs for channel A and channel B.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2021	*	Initial Release

A Appendix

A.1 References

Use the following links to available documentation and software:

- ADC32RF5x EVM software, available online
- ADC32RF54/55 data sheet (SBAS500)
- TSW14J58 EVM user guide (SLWU094)
- High Speed Data Converter Pro software and user guide (SLWU087)

Note

The EVM schematics, layout, and BOM are available on the ADC32RF54EVM tool page on www.ti.com/tool/ADC32RF54EVM.

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