User's Guide

ADS127L11EVM-PDK Evaluation Module

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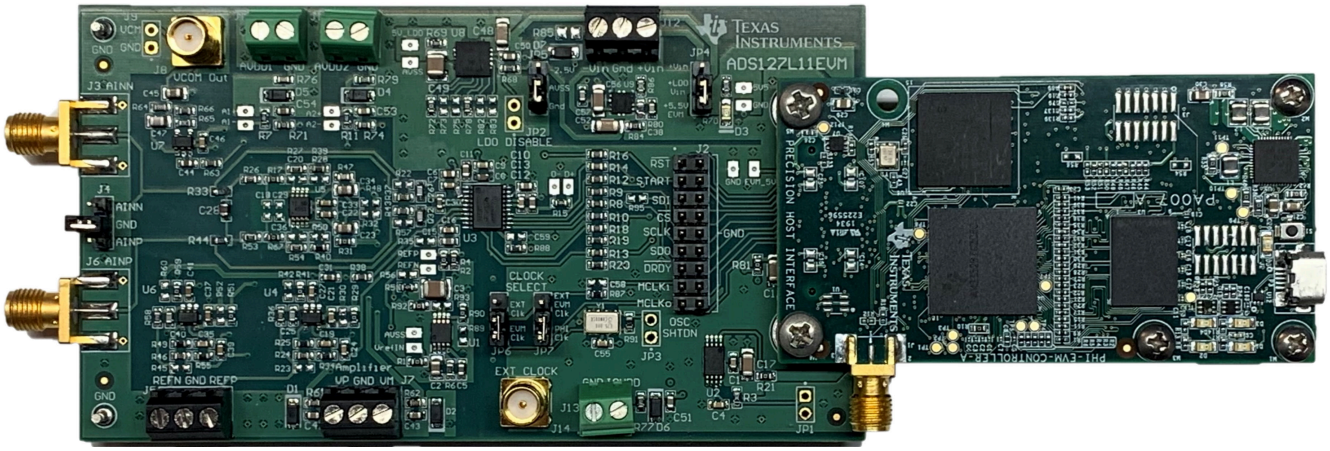
ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS127L11 evaluation module (EVM). This kit is an evaluation platform for the ADS127L11, which is a 24-bit, high-speed, wide-bandwidth, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS127L11 offers excellent ac and dc performance, along with multiple internal digital filter options, making the device useful for a wide variety of data acquisition applications. The ADS127L11EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the *ADS127L11EVM*.



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1 EVM Overview

The ADS127L11EVM is a platform for evaluating the performance of the ADS127L11, which is a 24-bit, high-speed, wide-bandwidth ΔΣ ADC. The evaluation kit includes the ADS127L11EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis. The ADS127L11EVM board includes the ADS127L11 ADC and all the peripheral analog circuits and components required to extract optimum performance from the ADC. The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS127L11
- Supplies power to all active circuitry on the ADS127L11EVM board

1.1 ADS127L11EVM Kit

The ADS127L11 evaluation module kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS127L11 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS127L11 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Windows® 8, and Windows® 10 operating systems
- Easy-to-use evaluation software for 64-bit Microsoft® Windows®
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

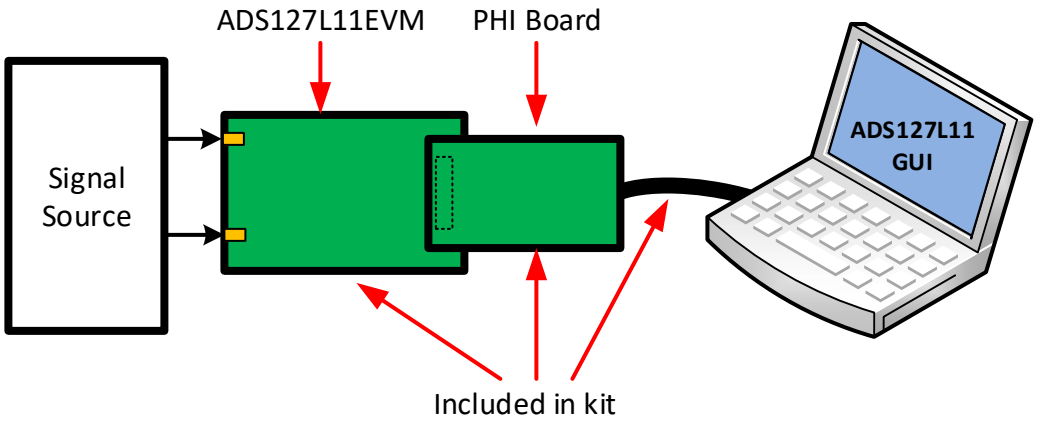

Figure 1-1. System Connection for Evaluation

1.2 ADS127L11EVM Board

The ADS127L11EVM board includes the following features:

- External signal source from differential pair SMA connectors
- Options to use external analog and digital power supplies
- Serial interface header for easy connection to the PHI controller
- Pin connections to monitor digital signals with a logic analyzer
- Onboard ultra-low noise, low-dropout (LDO) regulator for excellent 5-V, single-supply regulation of all analog circuits

1.3 ADS127L11EVM-PDK-GUI Unsupported Features

The following features of the ADS127L11 device are currently not supported in the ADS127L11EVM GUI, but will be on a future version of the software. To ensure proper operation of the EVM, do not modify the corresponding register settings from the default values.

- CONFIG2_REG; bits 4:3, START_MODE, default 00b, only start and stop conversions are supported
- CONFIG4_REG; bit 2, SPI_CRC, default 0b, CRC not supported
- CONFIG4_REG; bit 0, STATUS, default 0b, status readback not supported

2 EVM Analog Interface

The ADS127L11EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit, including jumper configuration for different input test signals and board connectors for signal sources.

2.1 EVM Analog Input Options

For best performance, differential analog input signals can be connected through the SMA connectors (J3 and J6). There is also a header, J4, that can be used to directly connect inputs for dc measurements, or where best ac performance is not needed. For single-ended inputs, header J4 can be used to connect AINN or AINP to GND using the supplied shunt. Then use either J3 or J6 as the single-ended input. The input driver circuit uses the THS4551 fully-differential amplifier in a unity-gain configuration with a single-pole RC filter at the output. Multiple passive components around the amplifier are intentionally left uninstalled to give users the flexibility to customize the input drive circuit for their specific application.

When differential inputs are connected to the SMA connectors (J3 and J6), make sure header J4 does not have any connection to pins 1 or 3. Only connect the included shunt to pin 2, and not between pins 1-2 or 1-3 for differential inputs.

2.2 ADC Connections and Decoupling

The circuit shown in Figure 2-1 shows all connections to the ADS127L11 data converter (U3). Each power-supply connection has a 1-µF and 100-nF decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the GND plane. The supply connections also have a series 0.1-Ω resistor. The purpose of this component is to facilitate current measurement for the ADC. Also, each digital input has a 10-Ω series resistor. These resistors smooth the edges of the digital signals so that they have minimal overshoot and ringing. Although not strictly required, these components may be included in the final design to improve digital signal integrity.

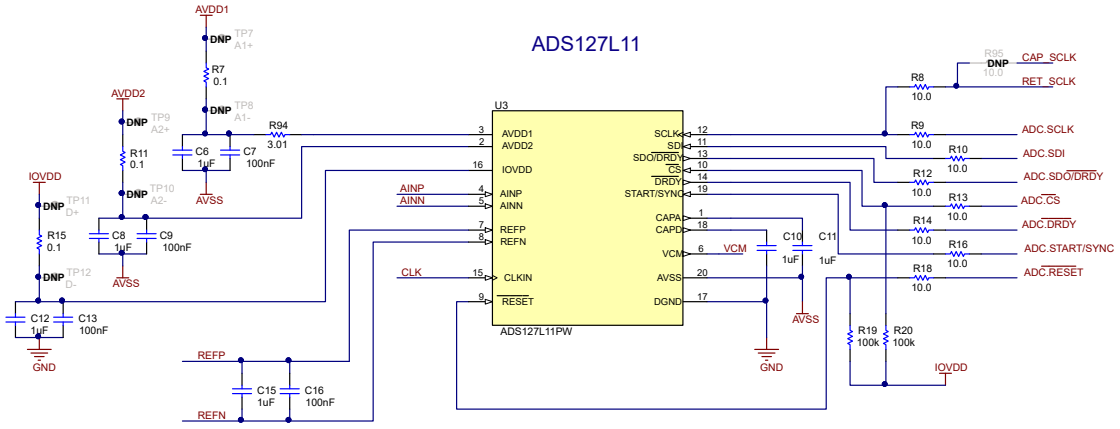

Figure 2-1. ADS127L11 Connections and Decoupling

2.3 ADC Input Drive Amplifiers

The circuit shown in Figure 2-2 is the fully differential amplifier (THS4551) used to drive the ADC. The input applied to J3 and J6 must be a low-distortion differential signal. The common-mode output for the amplifier is controlled by pin 2 on U5 (VOCM). The common-mode signal is set by the data converter (pin 6, VCM). The output of the amplifier connects to an RC filter that connects to the ADC input (R37, R43, C30, C26, and C32). The amplified configuration has several do not populate (DNP) components. These components provide flexibility, but are not required for good performance. The amplifier power supplies are connected by default to the AVDD and AVSS supplies that are also used for the ADC. The amplifier supplies can be changed to external supplies VP and VM by removing the 0-Ω resistors that connect to AVDD and AVSS (0R31 and 0R47), and installing them to connect VP and VM (0R32 and 0R48).

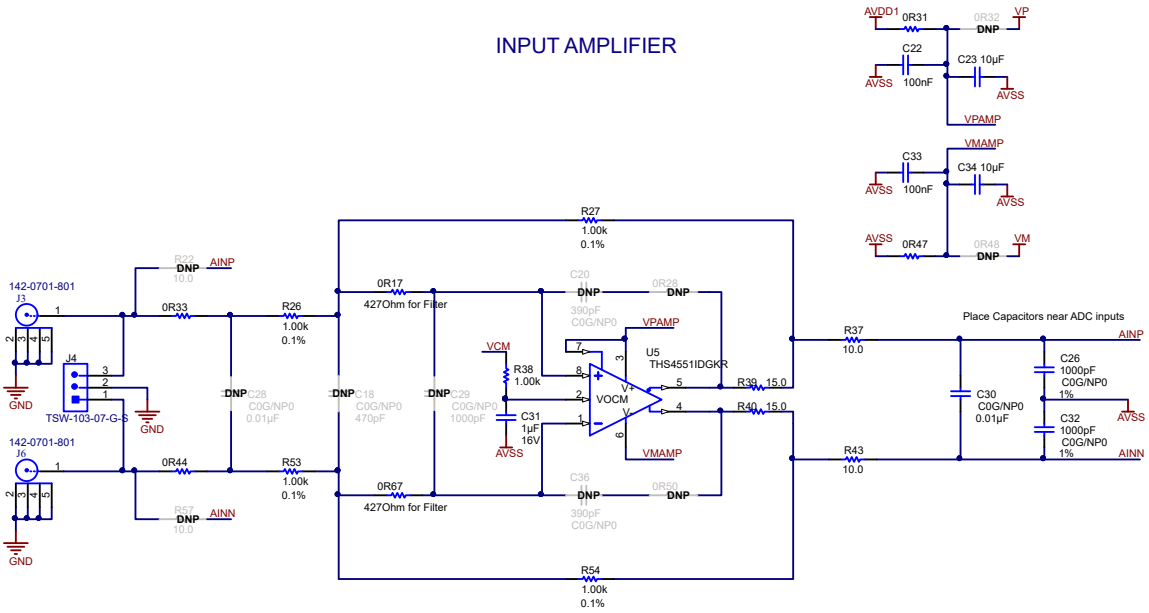

Figure 2-2. ADC Drive Amplifier

2.4 VCOM Buffer

The circuit shown in Figure 2-3 buffers the VCM signal from the ADC and connects this signal to the J8 SMA connector. This process is useful if the VCOM signal must be connected to an external piece of test equipment to set the common-mode voltage. A common use case is to connect this signal to the Audio Precision SYS-2722 to set the signal generators common-mode output. This circuit is not required in your end application and is only used for testing purposes.

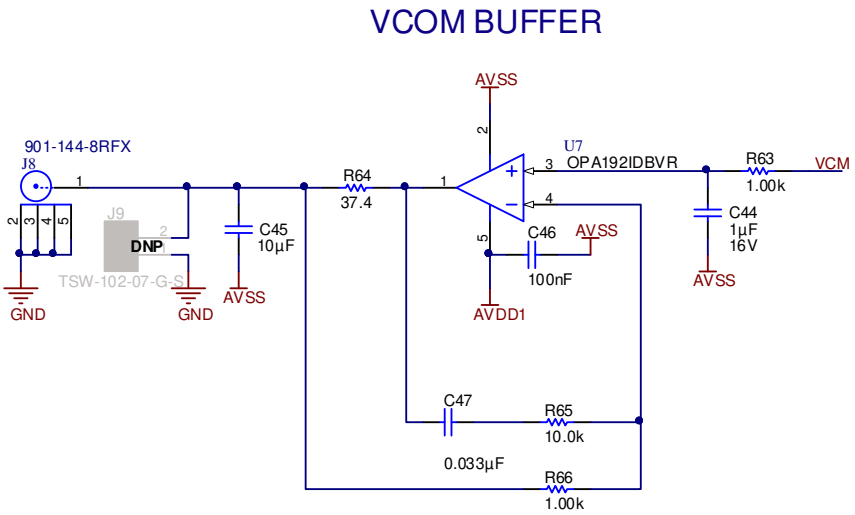

Figure 2-3. VCOM Buffer

2.5 Onboard Voltage Reference

Figure 2-4 shows the REF6225 configuration. This reference includes an integrated wide bandwidth buffer that makes the REF6225 ideal for driving the switched-capacitor input to the ADS127L11. The EVM provides a buffer and connections if you choose to use a different voltage reference. This reference is sufficient to meet the *ADS127L11 24-Bit, Wide-Bandwidth Analog-to-Digital Converter* data sheet specifications for dynamic performance.

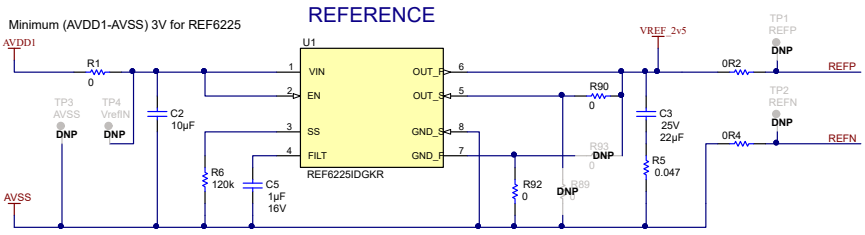

Figure 2-4. Onboard Voltage Reference

2.6 External Voltage Reference

Figure 2-5 shows a reference buffer that allows connection of an external voltage reference to connector J5. This circuit and connection is not required if the onboard voltage reference is used (see Figure 2-4). The amplifier here was selected for low voltage offset and low offset drift. The amplifier topology is designed to drive capacitive loads. For information on this topology, see the Op Amp Stability Videos in TI Precision Labs.

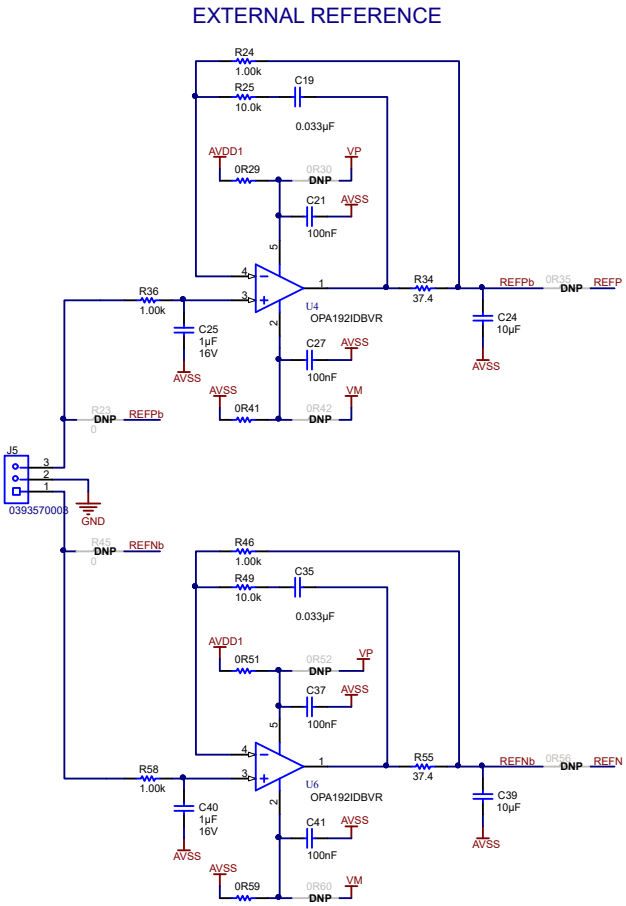

Figure 2-5. External Reference Connection and Buffer

2.7 Clock Tree

Figure 2-6 shows the different clock options for the ADS127L11EVM. The default position for jumper (JP7) 1-2 routes the PHI digital controller board clock to the CLK pin on the ADS127L11 (U3). If the ADS127L11EVM is used without the PHI board, then change the shunt on jumper (JP7) to position 2-3 to directly route the local clock to ADS127L11 (U3).

Jumper (JP6) selects either the local 25-MHz oscillator (Y1) on the ADS127L11EVM board, or an external clock supplied on the SMA connector (J14). The default position for jumper (JP6) 1-2 selects the local 25-MHz oscillator (Y1). The ADS127L11EVM-PDK-GUI software by default uses the 24-MHz PHI clock source, but can select the board clock source, 25-MHz (Y1) oscillator, or SMA connector (J14).

If the local 25-MHz oscillator (Y1) is used, then remove the shunt on jumper (JP3) to enable the oscillator. If an external clock source is used, use a CMOS square-wave signal with an amplitude equal to IOVDD (1.8 V with the PHI board) and a frequency within the specified range of the ADS127L11.

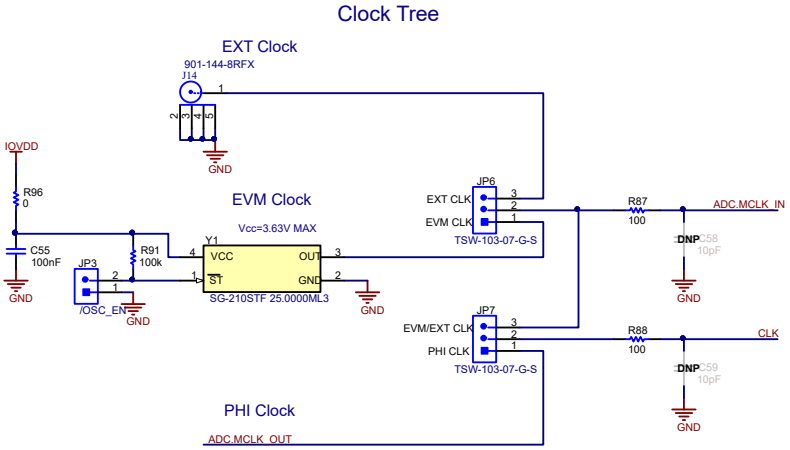

Figure 2-6. Clock Tree

3 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS127L11 ADC (over SPI) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS127L11 platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 Serial Interface (SPI)

The ADS127L11 ADC uses SPI serial communication in mode 1 (CPOL = 0, CPHA = 1). Because the serial clock (SCLK) frequency can be as fast as 40 MHz, the ADS127L11 EVM offers 10-Ω resistors between the SPI signals to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 10-Ω resistors slow down the signal edges in order to minimize signal overshoot. J2 provides test points to measure the digital signals.

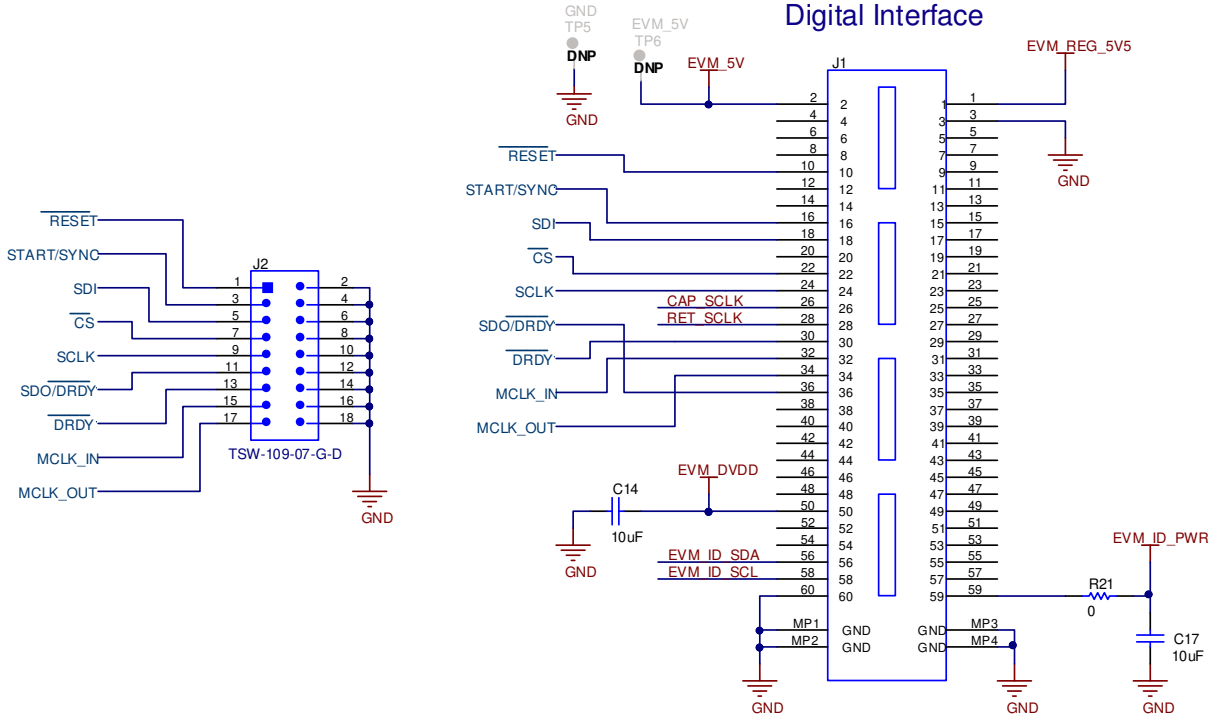

Figure 3-1. Connection to Digital Signals on PHI and Test Points

3.2 I2C Bus for Onboard EEPROM

The circuit shown in Figure 3-2 is used with our EVM controller (PHI), for EVM identification. This circuit is not required by the ADS127L11 for operation. The jumper (JP1) is a write protect and does not need to be changed for EVM operation.

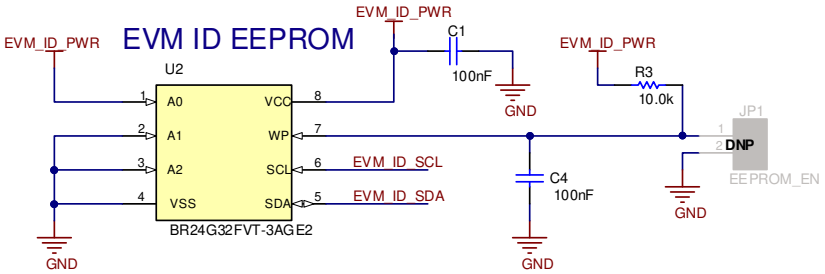

Figure 3-2. EEPROM for EVM ID

4 Power Supplies

The default state of the EVM is that all power supplies are generated using the USB power from the PHI controller. This section shows how external power connections can be made. Also, this section shows the default configuration for AVDD is generated with a 5-V low-dropout regulator (LDO).

4.1 Power Connection and Configuration

Figure 4-1 shows connections to external supplies for the amplifier, reference, and data converter. The default state of the EVM is that the power is provided by the PHI digital controller board via the USB port. The external power connections can be used in cases where the PHI does not provide the needed voltage. For example, the PHI does not provide negative voltages, so if a negative AVSS is needed an external power supply is required. To use the external power connections for AVDD and IOVDD, change the 0-Ω resistor connections (R71, R74, and R81).

Connector J12 can optionally be used to supply power to the onboard 5-V and –2.5-V regulators. In this case, the allowable voltage range for –VinExt is –15.5 V < –VinExt < –3.5 V and +VinExt is 6 V< +VinExt < 15.5 V.

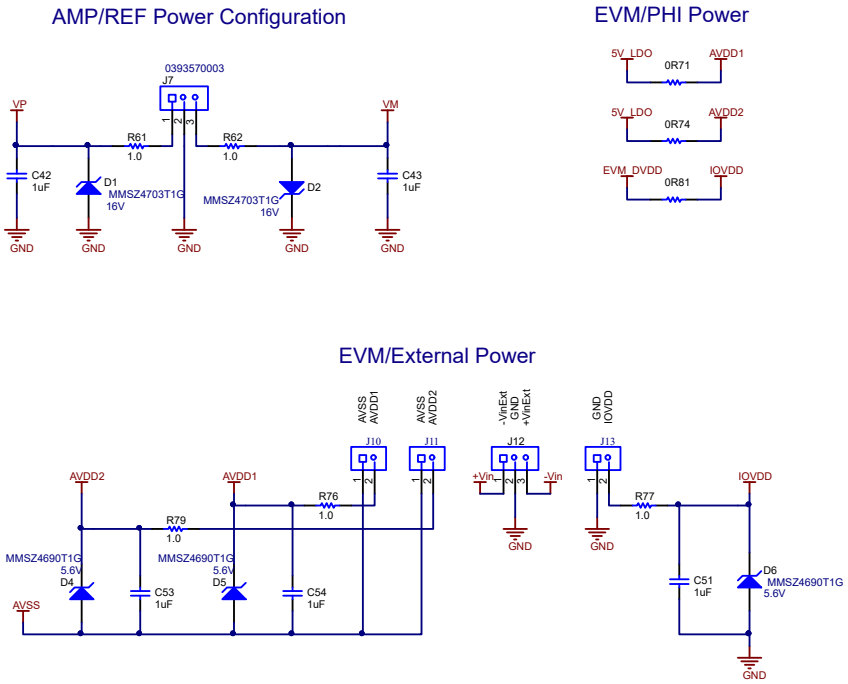

Figure 4-1. Power Connection and Configuration

4.2 Low Dropout Regulator (LDO)

Figure 4-2 shows how the 5.5-V power from the PHI is regulated to 5 V using a low-noise TPS7A4700 LDO. By default, the shunt on (JP4) 1-2 routes 5.5 V from the PHI to the LDO. The 5-V LDO can also be supplied by external power on J12 by moving the shunt on (JP4) to position 2-3. The 5-V LDO output is used for the AVDD connections and can be reprogrammed to different output voltages using R72, R73, R75, R78, R82, and R83.

There is an additional LDO that generates –2.5 V for AVSS, using the low-noise TPS7A3001 LDO. This LDO is only supplied by external power on J12. By default, AVSS is connected to GND with a shunt on (JP5) 1-2. If AVSS must be set to –2.5 V, then connect an external negative supply to J12 and move the shunt on (JP5) to position 2-3.

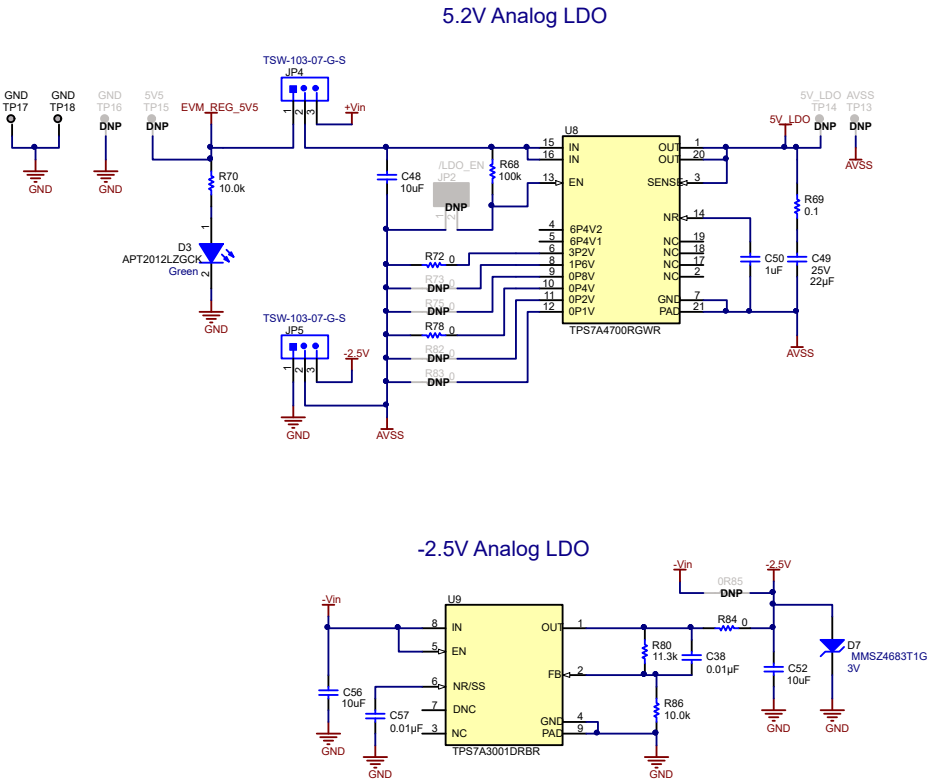

Figure 4-2. 5.5 V to 5 V LDO

5 ADS127L11EVM Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS127L11 EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

As shown in Figure 5-1, accept the license agreements and follow the on-screen instructions to complete the installation.

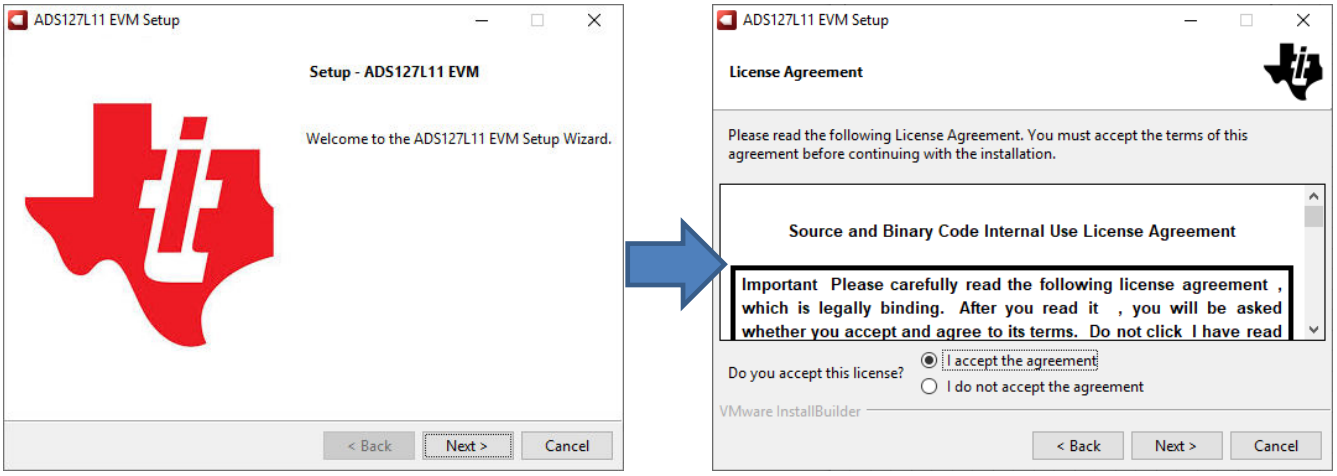

Figure 5-1. Software Installation and Prompts

As a part of the ADS127L11 EVM GUI installation, a prompt with a *Device Driver Installation* appears on the screen, as shown in Figure 5-2. Click *Next* to proceed.

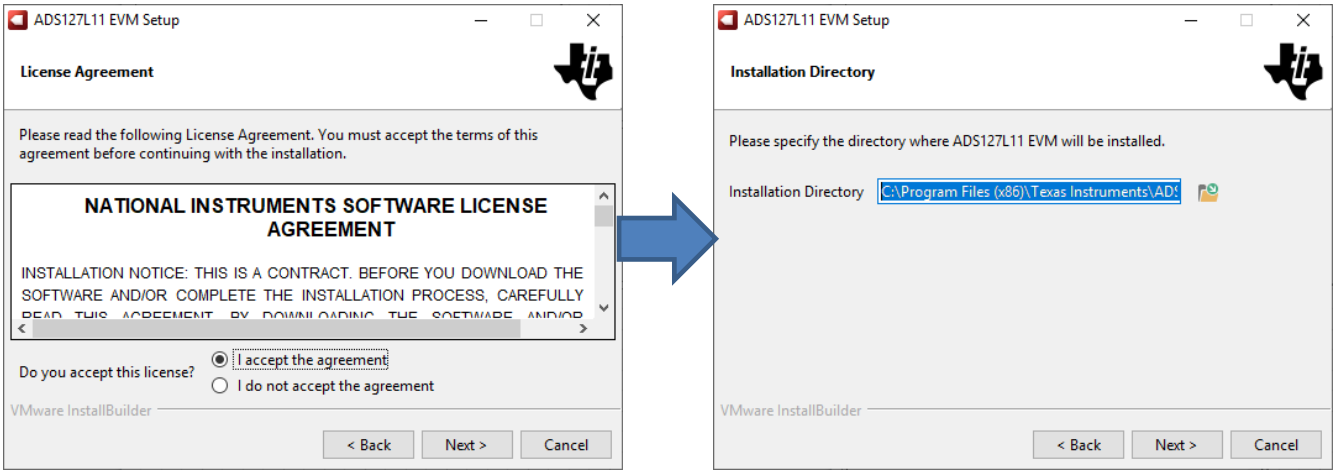

Figure 5-2. Software Installation and Prompts

The ADS127L11 EVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 5-3, if not already installed.

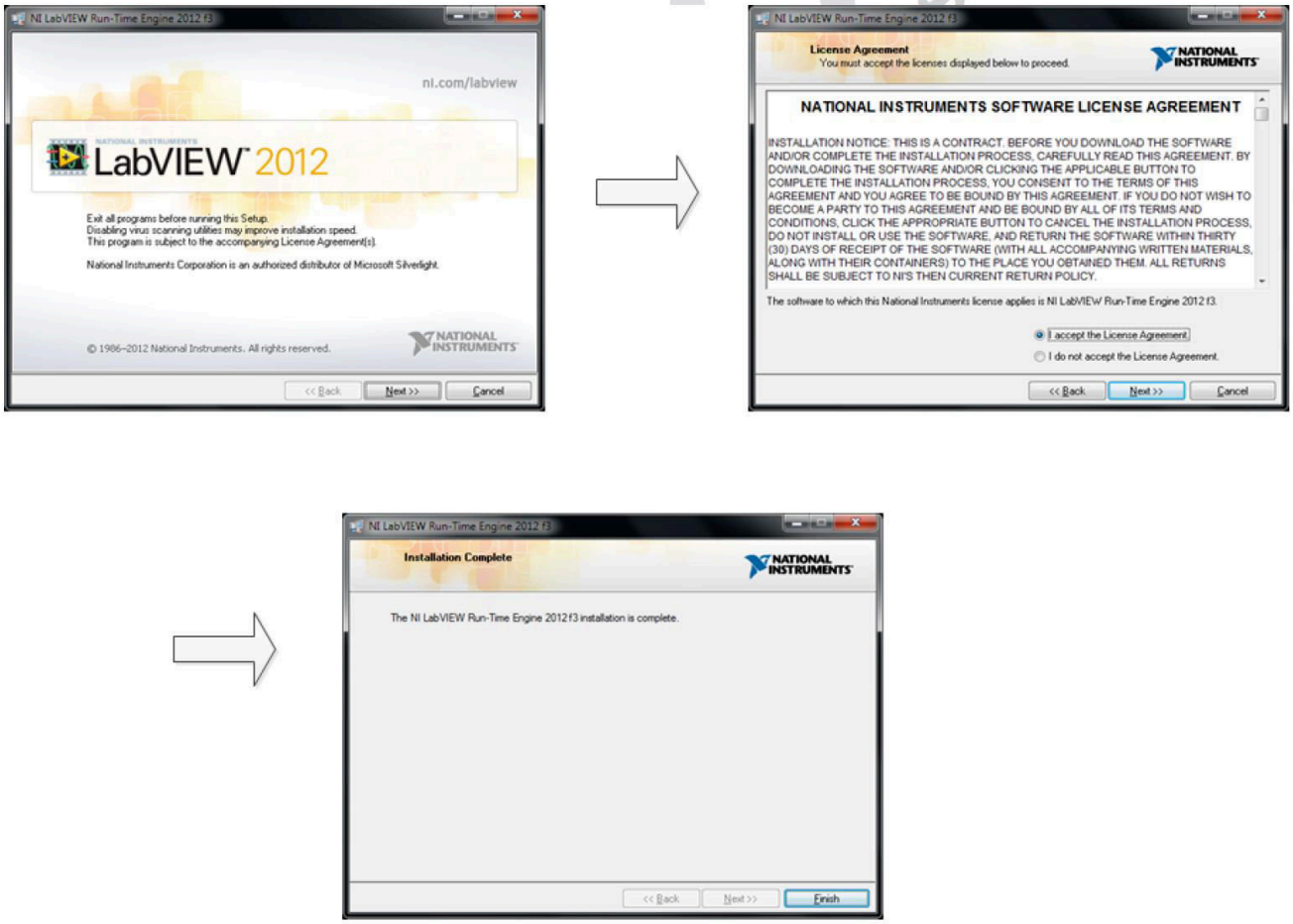

Figure 5-3. LabVIEW Run-Time Engine Installation

6 EVM Operation

6.1 Connecting the Hardware

After installing the software, connect the EVM as shown in Figure 6-1:

1. Physically connect P2 of the PHI to J1 of the ADS127L11EVM. Install the screws to assure a robust connection.
2. Connect USB on PHI to the computer first.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 6-1 shows the resulting LED indicators.
3. Start the software GUI as shown in Figure 6-2. You will notice that the LEDs blink slowly as the FPGA firmware is loaded on the PHI. This loading takes a few seconds then the AVDD and DVDD power supplies will turn on.
4. Connect the signal generator. The input range is 0 V to 5 V. A common input signal applied is a 4.9-V_{PP} signal with a 2.5-V offset. This signal is adjusted just below the full-scale range to avoid clipping.

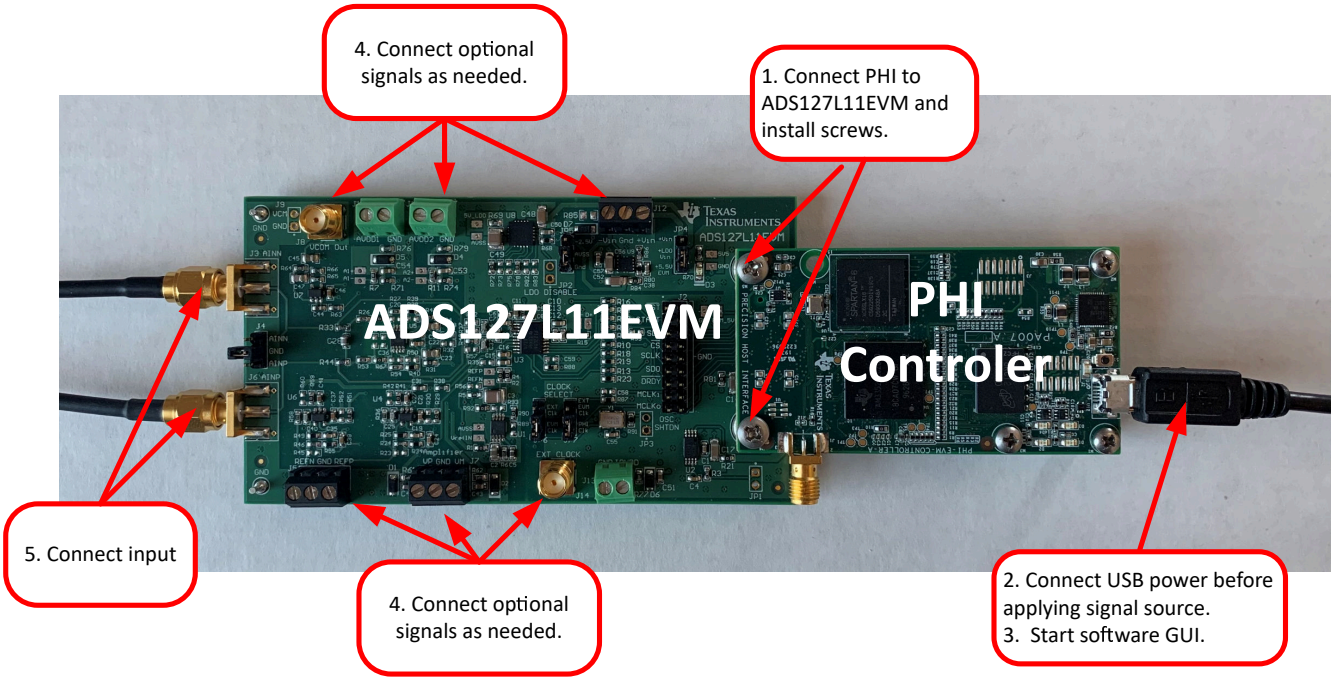

Figure 6-1. Connecting the Hardware to the ADS127L11

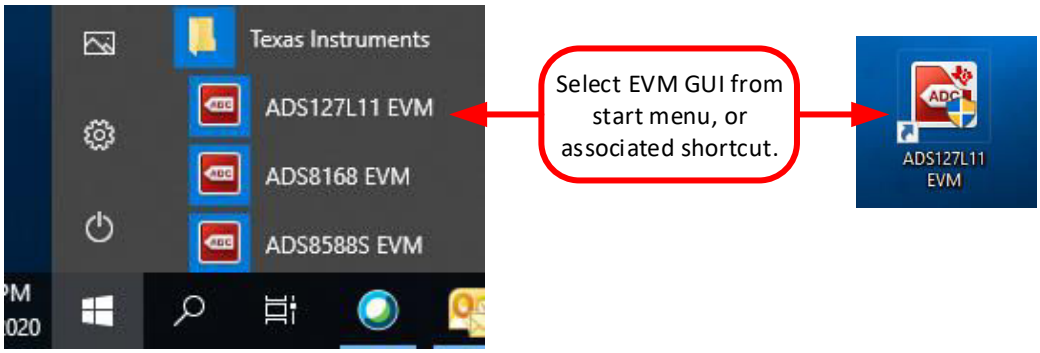

Figure 6-2. Launch the EVM GUI Software

6.2 Optional Connections to the EVM

Figure 6-3 shows optional connections to power, clock, and VCM. These connections are not required for initial setup of the EVM but may be helpful to configure the EVM more closely to your end application configuration. Review the schematic and hardware sections of this document to understand how these connections are used.

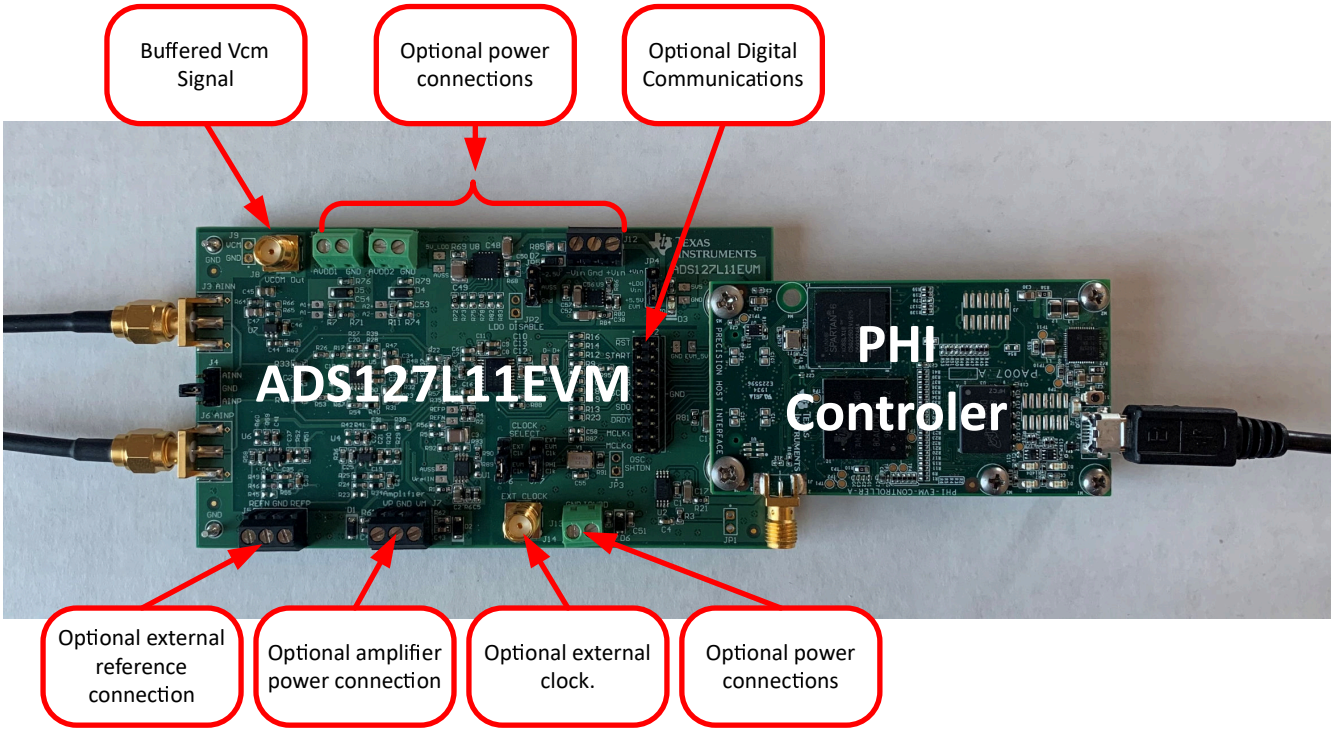

Figure 6-3. Optional Connections to the EVM

6.3 EVM GUI Global Settings for ADC Control

Figure 6-4 shows that the EVM global controls are located on the left-hand side of the GUI. These controls include the number of samples, master clock frequency, SCLK frequency, sampling rate, and others. In the upper left-hand side of the GUI is the *Pages* control that allows access to the other key pages in the GUI. Figure 6-4 also shows the ADC register settings. The registers can be used to set the different device modes such as filter settings and power settings.

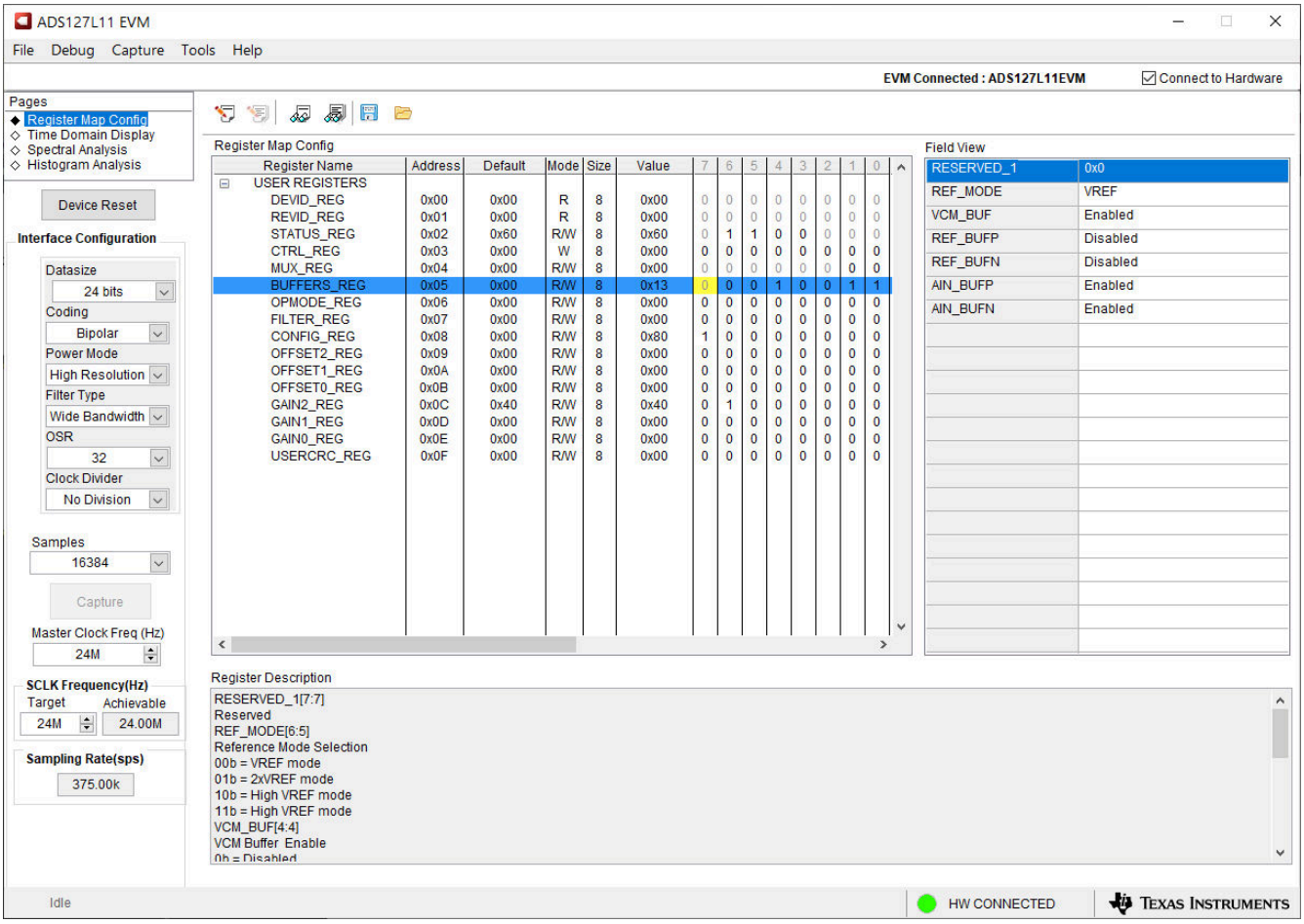

Figure 6-4. EVM GUI Global Settings for ADC Control

6.4 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS127L11 EVM, as per the current interface mode settings indicated in Figure 6-5 by using the *Capture* button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

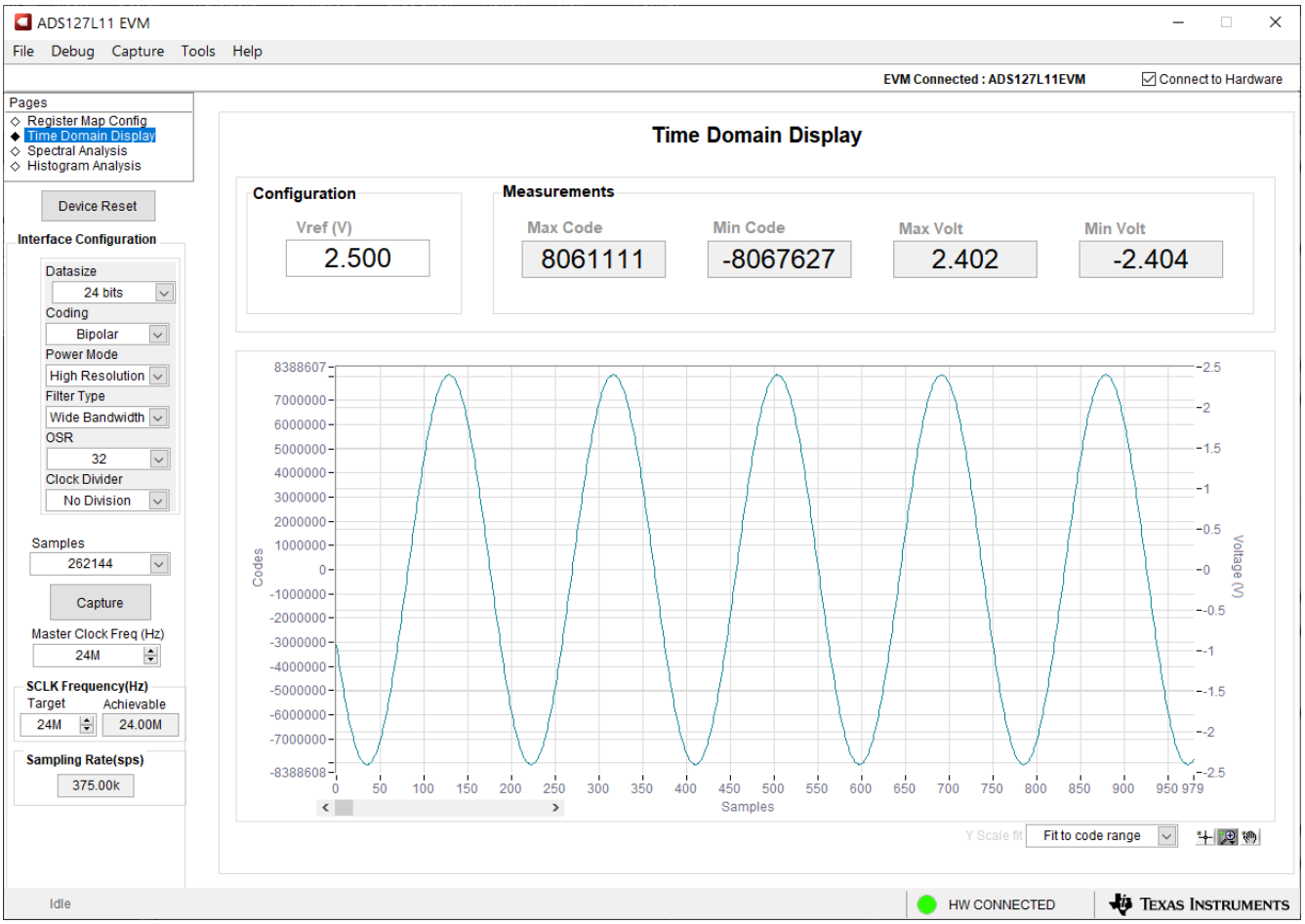

Figure 6-5. Time Domain Display

6.5 Frequency Domain Display

The spectral analysis tool, shown in Figure 6-6, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS127L11 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The None option corresponds to not using a window (or using a rectangular window) and is not recommended.

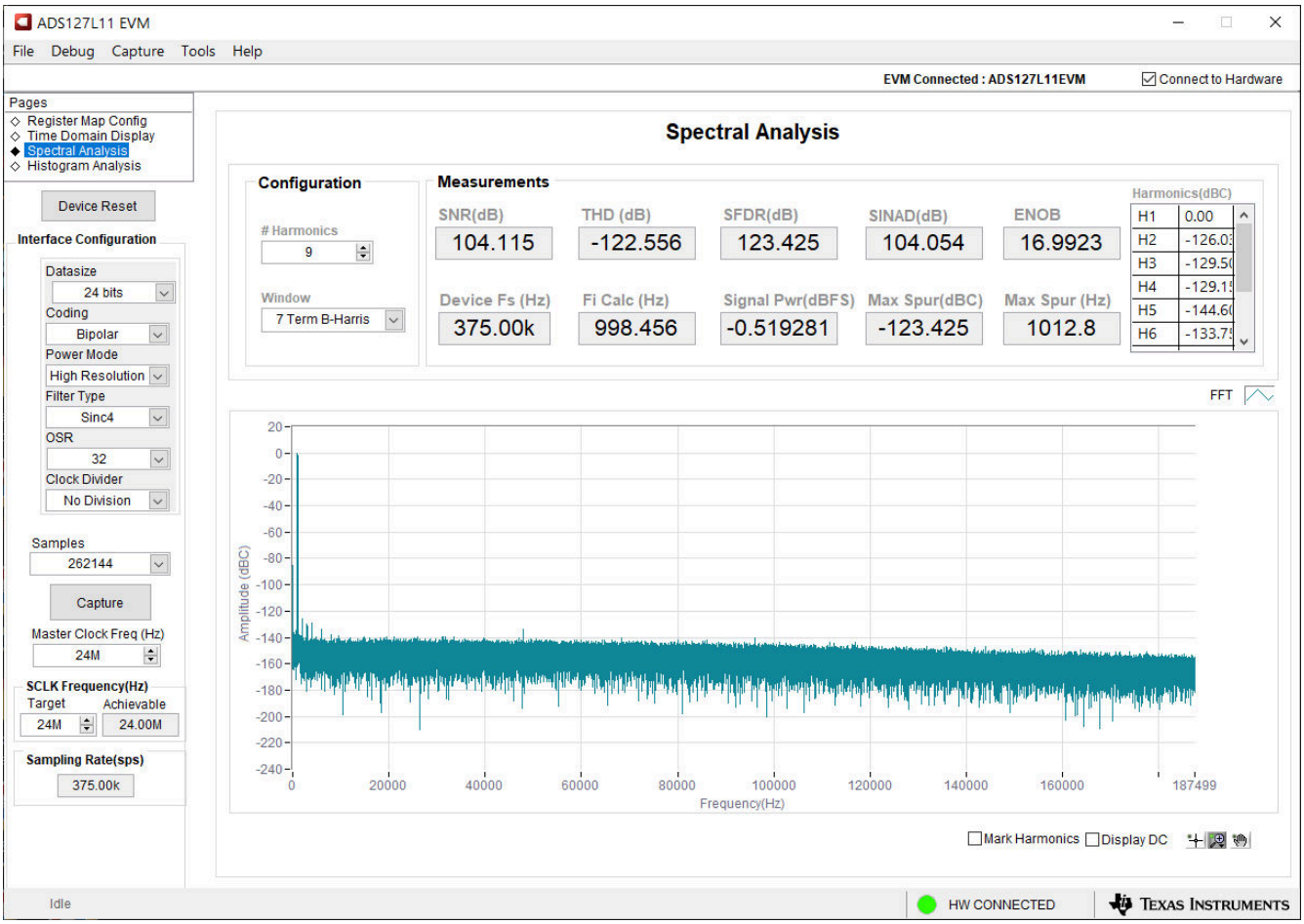

Figure 6-6. Frequency Domain Display

6.6 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel. As shown in Figure 6-7, the histogram corresponding to a dc input is displayed on clicking the Capture button.

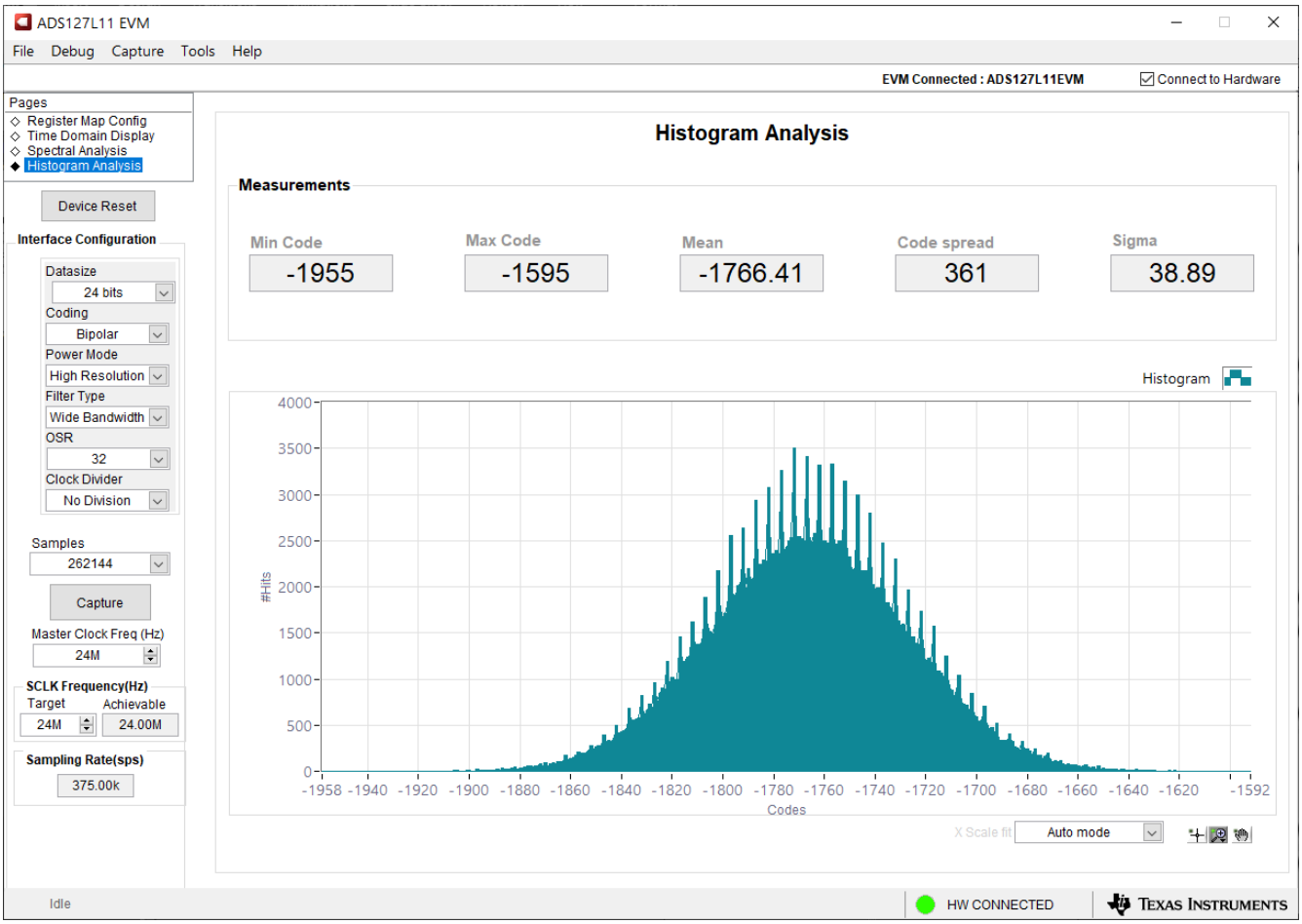

Figure 6-7. Histogram Display

7 Bill of Materials, Schematics, and Layout

This section contains the ADS127L11EVM bill of materials, PCB layout, and the EVM schematics.

7.1 Bill of Materials

Table 7-1 lists the bill of materials for the ADS127L11EVM.

Table 7-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC105	Any
C1, C4, C7, C9, C13, C16, C21, C22, C27, C33, C37, C41, C46, C55	14	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C2, C23, C24, C34, C39, C45	6	10uF	CAP, CERM, 10 µF, V,+/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata
C3, C49	2	22uF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C5, C25, C31, C40, C44	5	1uF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C105K080AC	TDK
C6, C8, C10, C11, C12, C15, C42, C43, C50, C51, C53, C54	12	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C14, C17, C48, C52, C56	5	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C19, C35, C47	3	0.033uF	CAP, CERM, 0.033 µF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	0805	CGA4J2C0G1H333J125AA	TDK
C26, C32	2	1000pF	CAP, CERM, 1000 pF, 25 V,+/- 1%, C0G/NP0, 0603	0603	C0603C102F3GACTU	Kemet
C30, C38, C57	3	0.01uF	CAP, CERM, 0.01 µF, 25 V,+/- 1%, C0G/NP0, 0603	0603	C0603C103F3GACTU	Kemet
D1, D2	2	16V	Diode, Zener, 16 V, 500 mW, SOD-123	SOD-123	MMSZ4703T1G	ON Semiconductor
D3	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D4, D5, D6	3	5.6V	Diode, Zener, 5.6 V, 500 mW, SOD-123	SOD-123	MMSZ4690T1G	ON Semiconductor
D7	1	3V	Diode, Zener, 3 V, 500 mW, SOD-123	SOD-123	MMSZ4683T1G	ON Semiconductor
H1	1		Cable, USB-A to micro USB-B, 1 m - Kitting item		102-1092-BL-00100	CnC Tech
H2, H3	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
H4, H5, H6, H7	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H8, H9	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H10	1		PHI-EVM Controller Kitting item Edge# 6591636		PA007	Texas Instruments
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J2	1		Header, 100mil, 9x2, Gold, TH	9x2 Header	TSW-109-07-G-D	Samtec
J3, J6	2		Connector, End launch SMA, 50 ohm, SMT	End Launch SMA	142-0701-801	Cinch Connectivity
J4, JP4, JP5, JP6, JP7	5		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J5, J7, J12	3		Terminal Block, 3.5 mm, 3x1, Tin, TH	Terminal Block, 3.5 mm, 3x1, TH	0393570003	Molex
J8, J14	2		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
J10, J11, J13	3		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
JP1, JP3	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
LBL1	1			PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R2, R4, R17, R21, R29, R31, R33, R41, R44, R47, R51, R59, R67, R71, R72, R74, R78, R81, R84, R90, R92, R96	23	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R3, R25, R49, R65, R70, R86	6	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R5	1	0.047	RES, 0.047, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF47MV	Panasonic
R6	1	120k	RES, 120 k, 0.1%, 0.1 W, 0603	0603	RG1608P-124-B-T5	Susumu Co Ltd
R7, R11, R15, R69	4	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF10CV	Panasonic
R8, R9, R10, R12, R13, R14, R16, R18	8	10.0	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
R19, R20, R68, R91	4	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R24, R36, R38, R46, R58, R63, R66	7	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R26, R27, R53, R54	4	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic
R34, R55, R64	3	37.4	RES, 37.4, 1%, 0.1 W, 0603	0603	RC0603FR-0737R4L	Yageo
R37, R43	2	10.0	RES, 10.0, 0.1%, 0.1 W, 0603	0603	TNPW060310R0BEEA	Vishay-Dale
R39, R40	2	15.0	RES, 15.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060315R0FKEA	Vishay-Dale
R61, R62, R76, R77, R79	5	1.0	RES, 1.0, 5%, 0.4 W, AEC-Q200 Grade 0, 0805	0805	ESR10EZPJ1R0	Rohm
R80	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K3L	Yageo
R87, R88	2	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RFKEA	Vishay-Dale
R94	1	3.01	RES, 3.01, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06033R01FKEA	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	6	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP17, TP18	2		Terminal, Turret, TH, Double	Keystone1573-2	1573-2	Keystone
U1	1		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6225IDGKR	Texas Instruments
U2	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U3	1		24-bit, wide-bandwidth, low-power, delta-sigma analog-to-digital converter, PW0020A (TSSOP-20)	PW0020A	ADS127L11PW	Texas Instruments
U4, U6, U7	3		Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with E-trim, 4.5 to 36 V, -40 to 125 degC, 5-Pin SOT-23 (DBV), Green (RoHS & no Sb/Br), Tape and Reel	DBV0005A	OPA192IDBVR	

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U5	1		Low Noise, Precision, 150MHz, Fully Differential Amplifier, DGK0008A (VSSOP-8)	DGK0008A	THS4551IDGKR	Texas Instruments
U8	1		36V, 1A, 4.17µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U9	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	DRB0008A	TPS7A3001DRBR	Texas Instruments
Y1	1		Oscillator, 25 MHz, SMD	SMD, 2x2.5mm	SG-210STF 25.0000ML3	Epson

7.2 Board Layouts

Figure 7-1 shows the PCB layouts for the ADS127L11 EVM.

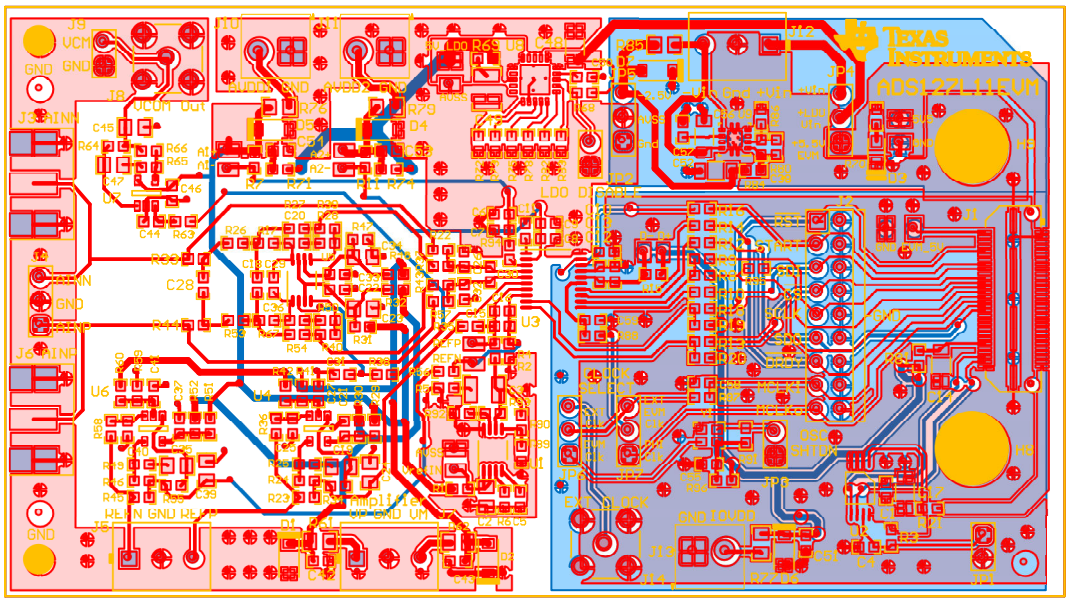

Figure 7-1. PCB Layouts for the ADS127L11 EVM

7.3 Schematics

This section shows the schematics for the ADS127L11EVM.

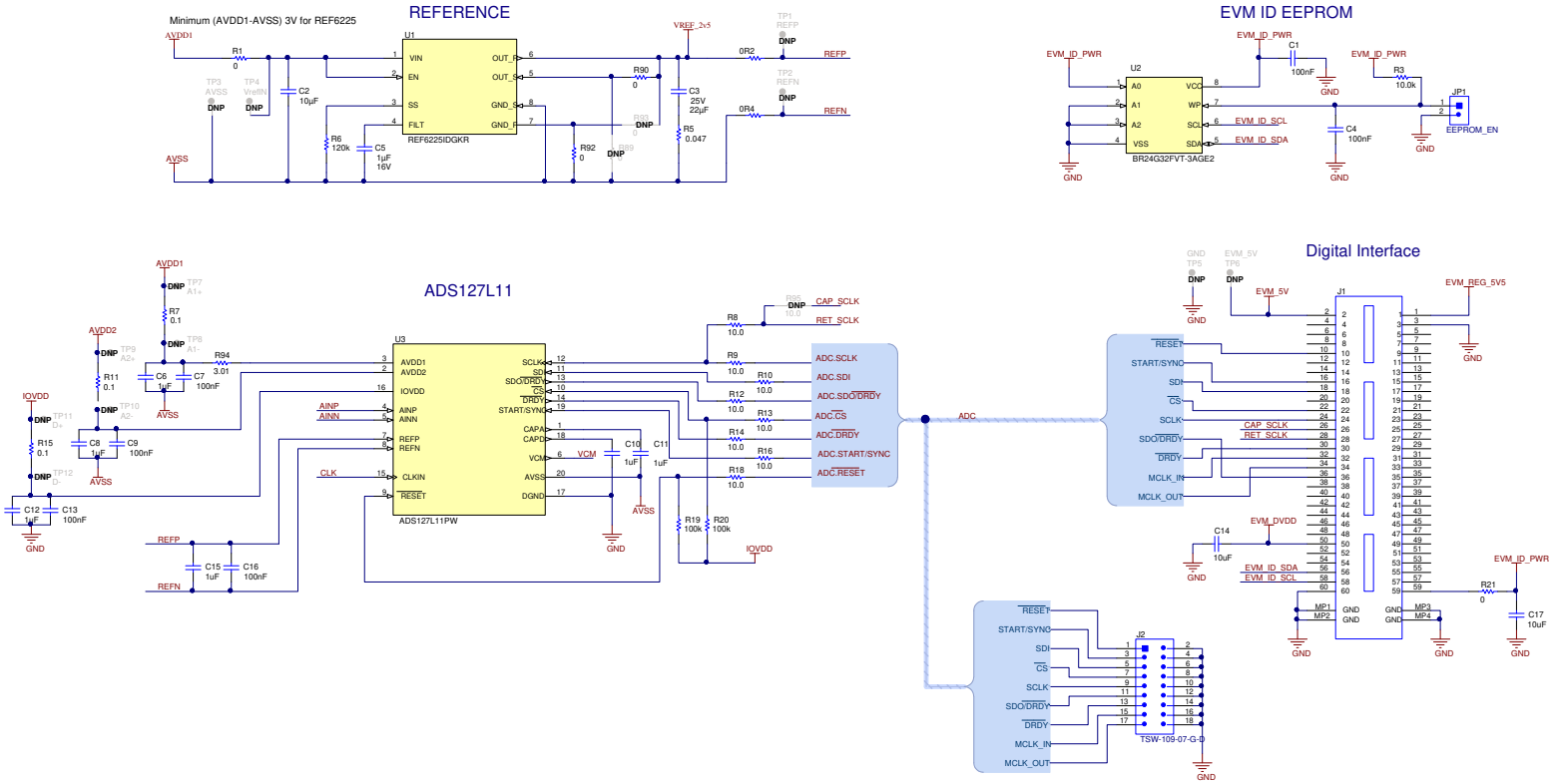

Figure 7-2. ADS127L11EVM ADC Connections and Reference Schematic

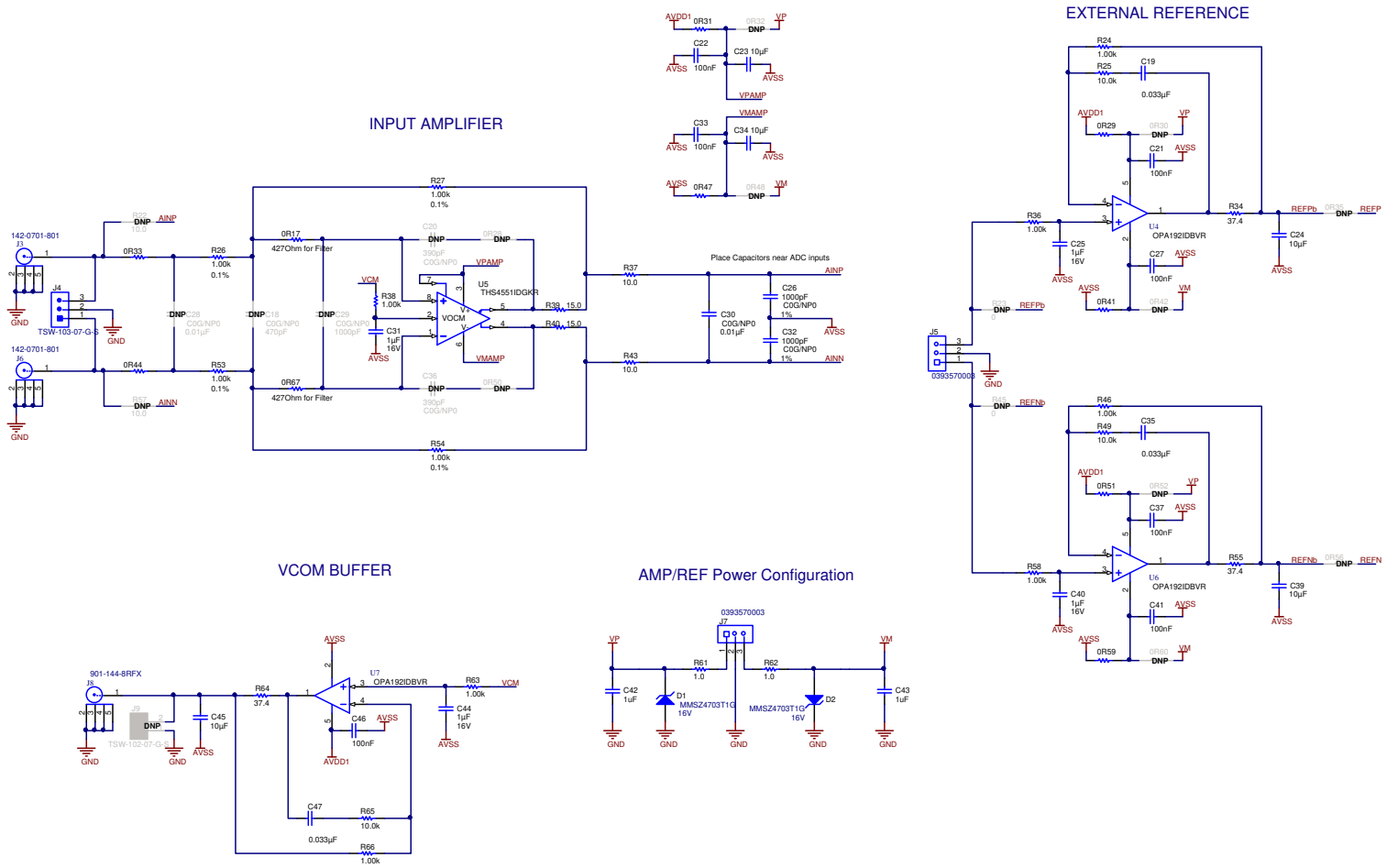

Figure 7-3. ADS127L11EVM Input Amplifier, VCOM buffer, and External Reference Schematic

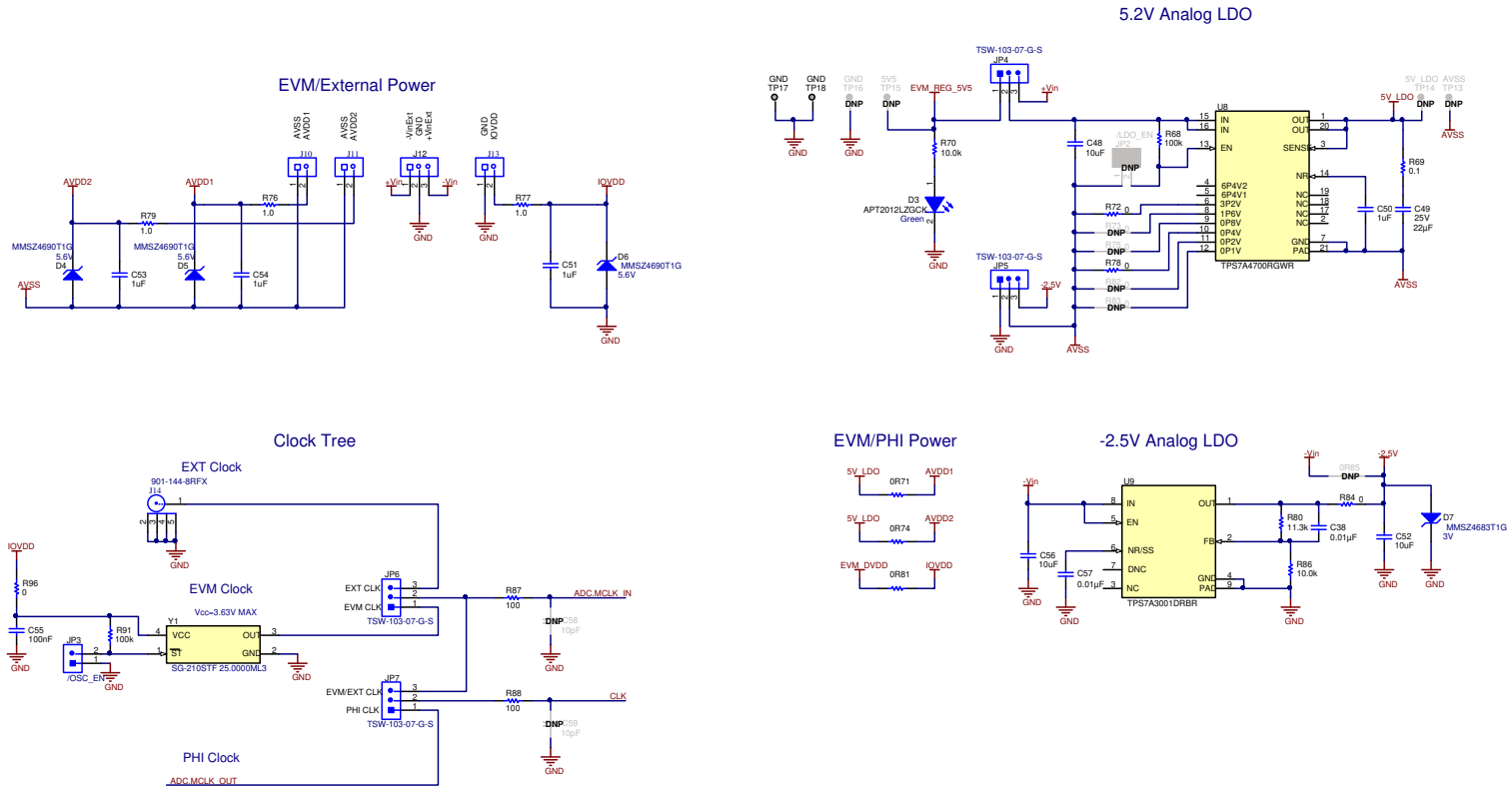

Figure 7-4. ADS127L11EVM Clock Tree and Power Schematic

8 References

- Texas Instruments, *ADS127L11 24-Bit, Wide-Bandwidth Analog-to-Digital Converter* data sheet

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