

FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay
- Zero ground bounce
- Undershoot clamp diodes on all switch and control pins
- Four enables control five bits each
- TTL-compatible input and output levels
- Available in 48-pin QVSOP package

APPLICATIONS:

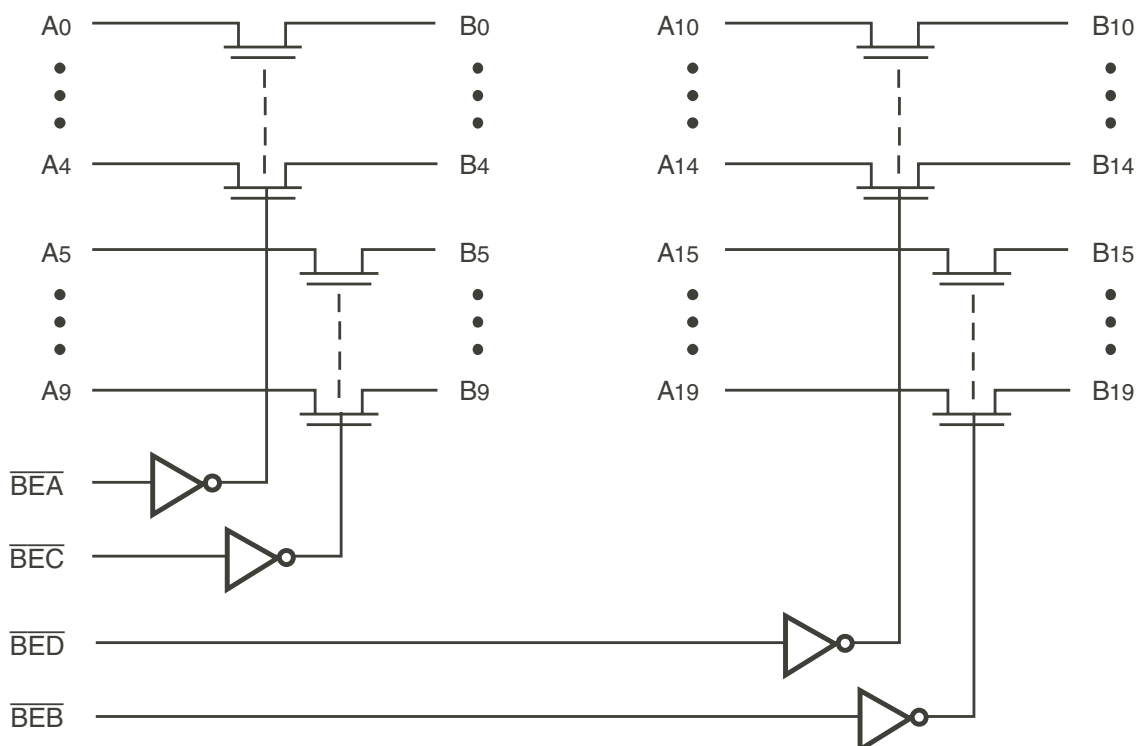
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Power conservation
- Capacitance reduction and isolation
- Bus isolation
- Clock gating

DESCRIPTION:

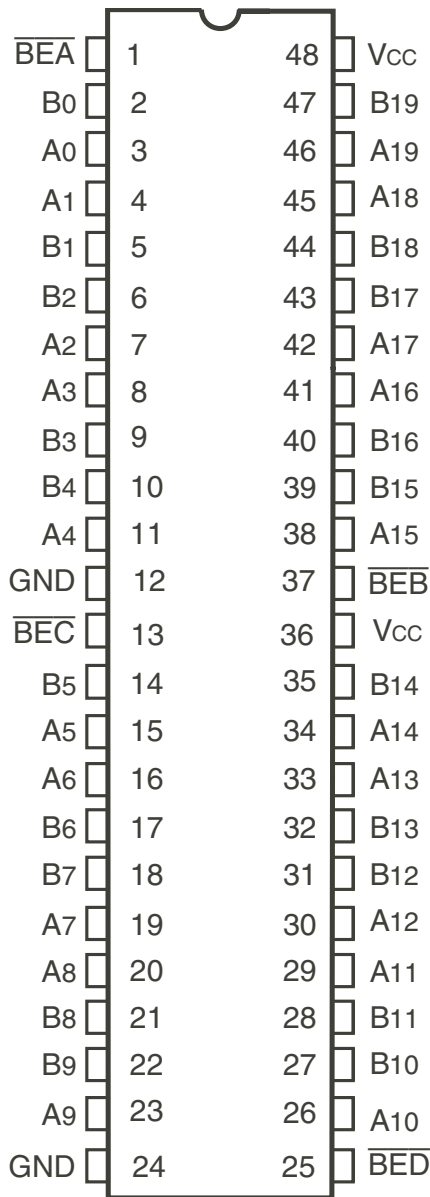
The QS32X384 provides a set of twenty high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS32X384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable (BE) signals turn the switches on. Four Bus Enable signals are provided, one for each of five bits of the 20-bit bus. The '384 family of QuickSwitch products is ideal for switching wide digital buses, as well as hotplug buffering, and 5V to 3V conversion.

The QS32X384 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	I/O	Description
A0 - A19	I/O	Bus A
B0 - B19	I/O	Bus B
$\overline{\text{BEA}}$	I	Enable, 0 - 4
$\overline{\text{BEB}}$	I	Enable, 15 - 19
$\overline{\text{BEC}}$	I	Enable, 5 - 9
$\overline{\text{BED}}$	I	Enable, 10 - 14

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
$V_{\text{TERM}}^{(2)}$	Supply Voltage to Ground	-0.5 to +7	V
$V_{\text{TERM}}^{(3)}$	DC Switch Voltage V_{S}	-0.5 to +7	V
$V_{\text{TERM}}^{(3)}$	DC Input Voltage V_{IN}	-0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width $\leq 20\text{ns}$)	-3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation ($T_{\text{A}} = 85^{\circ}\text{C}$)	0.5	W
T_{STG}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC} .

CAPACITANCE ($T_{\text{A}} = +25^{\circ}\text{C}$, $F = 1\text{MHz}$, $V_{\text{IN}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$)

Pins	Typ.	Max. ⁽¹⁾	Unit
Control Inputs	3	5	pF
Quickswitch Channels (Switch OFF)	5	7	pF

NOTE:

- This parameter is guaranteed but not production tested.

FUNCTION TABLE⁽¹⁾

$\overline{\text{BEA}}$	$\overline{\text{BEB}}$	B0 - B4	B15 - B19	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0 - A4	Hi-Z	Connect
H	L	Hi-Z	A15 - A19	Connect
L	L	A0 - A4	A15 - A19	Connect
$\overline{\text{BEC}}$	$\overline{\text{BED}}$	B5 - B9	B10 - B14	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A5 - A9	Hi-Z	Connect
H	L	Hi-Z	A10 - A14	Connect
L	L	A5 - A9	A10 - A14	Connect

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

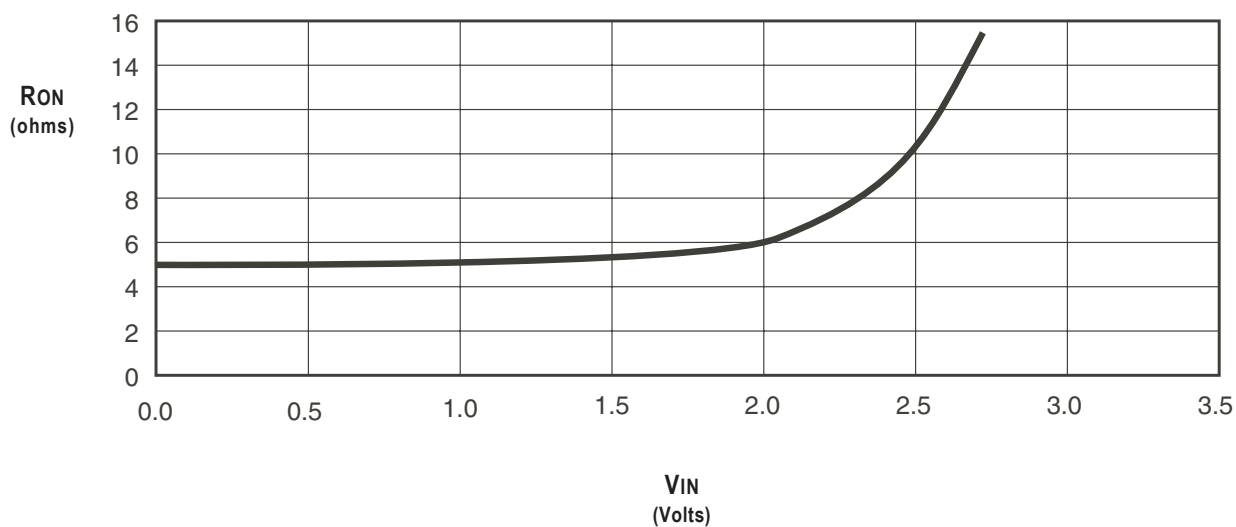
Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	± 0.01	± 1	μA
I_{OZ}	Off-State Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$, Switches OFF	—	± 0.01	± 1	μA
R_{ON}	Switch ON Resistance	$V_{CC} = \text{Min}$, $V_{IN} = 0\text{V}$, $I_{ON} = 30\text{mA}$	—	5	7	Ω
		$V_{CC} = \text{Min}$, $V_{IN} = 2.4\text{V}$, $I_{ON} = 15\text{mA}$	—	10	15	
V_P	Pass Voltage ⁽²⁾	$V_{CC} = 5\text{V}$, $I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

NOTES:

- Typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^{\circ}\text{C}$.
- Pass voltage is guaranteed but not production tested.

TYPICAL ON RESISTANCE vs V_{IN} AT $V_{CC} = 5\text{V}$



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Max.	Unit
I _{CCQ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0	3	mA
ΔI _{CC}	Power Supply Current per Control Input HIGH ⁽²⁾	V _{CC} = Max., V _{IN} = 3.4V, f = 0	2.5	mA
I _{CCD}	Dynamic Power Supply Current per MHz ⁽³⁾	V _{CC} = Max., A and B Pins Open, Control Input Toggling at 50% Duty Cycle	0.25	mA/MHz

NOTES:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to ΔI_{CC}.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

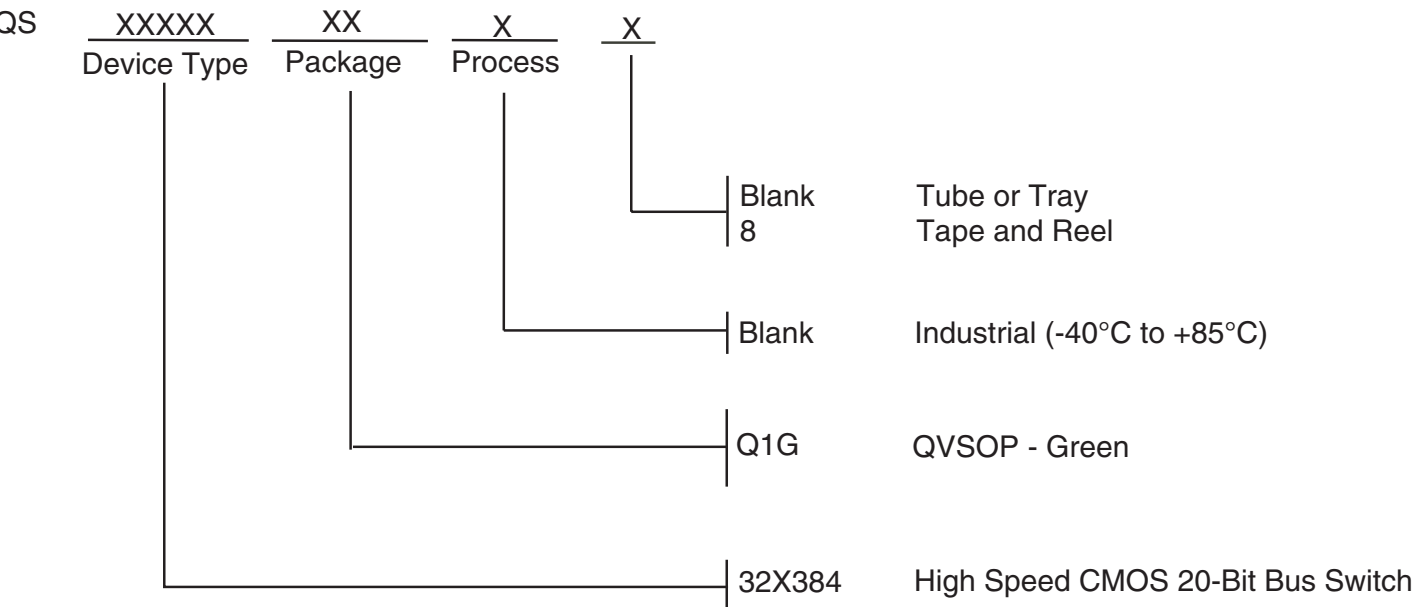
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Parameter	Min. ⁽¹⁾	Typ.	Max.	Unit
t _{PLH} t _{PHL}	Data Propagation Delay ^(2,4) Ax to Bx, Bx to Ax	—	—	0.25 ⁽³⁾	ns
t _{PZL} t _{PZH}	Switch Turn-on Delay B _{EN} to Ax, Bx	1.5	—	6.5	ns
t _{PLZ} t _{PHZ}	Switch Turn-off Delay ⁽²⁾ B _{EN} to Ax, Bx	1.5	—	5.5	ns

NOTES:

- Minimums are guaranteed but not production tested.
- This parameter is guaranteed but not production tested.
- The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

ORDERING INFORMATION



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