Description

The P9415-R is a highly integrated single-chip wireless power transmitter/receiver IC (TRx) that can be configured to receive or transmit an AC power signal through magnetic induction.

When the device is configured as a wireless power transmitter, it uses an on-chip full/half-bridge inverter, a PWM generator, a modulator/demodulator for communication, and a microcontroller to produce an AC power signal to drive external L-C tank. As a receiver, the P9415-R receives an AC power signal from a wireless transmitter and converts it into rectified output voltage, which can be used to power devices or supply the charger input in mobile applications. The P9415-R integrates a high-efficiency Synchronous Full Bridge Rectifier and control circuitry to modulate the load to send message packets to the Transmitter (Tx) to optimize power delivery.

The P9415-R features Multiple-time programmable (MTP) non-volatile memory that enables customers to customize the design parameters such as default output voltage and FOD thresholds.

The P9415-R includes over-temperature and voltage protection. Fault conditions associated with power transfer are managed by an industry-leading 32-bit ARM® Cortex®-M0 processor offering a high level of programmability while consuming extremely low standby power. The processor can also control GPIOs to indicate operating and fault modes. The device is available in an ultra-small 53-WLCSP package.

Typical Applications

- Wireless power solution for mobile applications

Features

- Delivers up to 15W as a receiver
- WattShare™ (TRx)mode with up to 5W Tx capability
- 24kB Multiple-time programmable (MTP) non-volatile memory
- WPC 1.3 Specification hardware ready
- 2.5V Under-Voltage Lockout (UVLO) threshold for expanding the charging area
- Internal reverse current sense for WattShare™ mode
- Reliable VRECT over-voltage clamping
- Internal IOUT filtering to remove the battery charger current ripple
- Supports Bi-Directional communications
- Supports X-Y alignment coils
- The device is capable of delivering 30W using a custom firmware
- Embedded 32-bit ARM® Cortex®-M0 processor
- Supports I2C 400kHz standard interface and GPIOs
- Package: 6 × 9 ball array, 2.82 × 4.22 × 0.50 mm, 53-WLCSP with 0.40mm ball pitch

Typical Applications Schematic

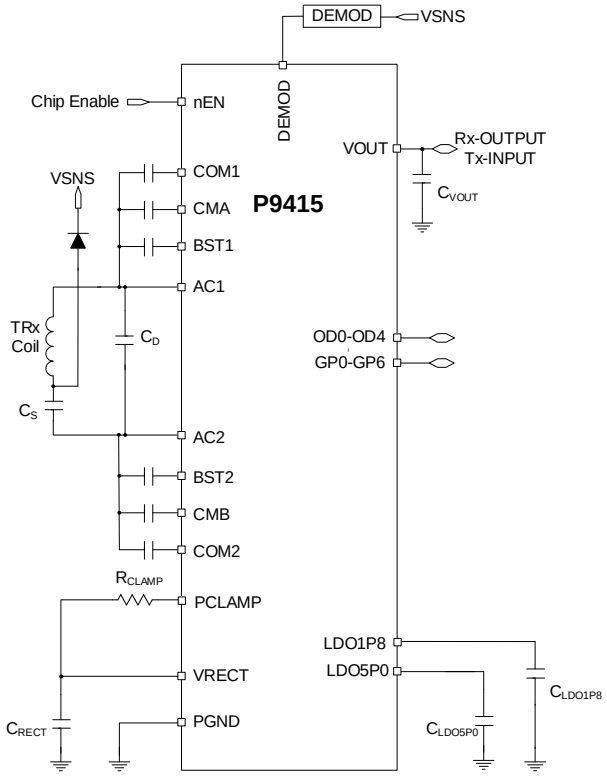

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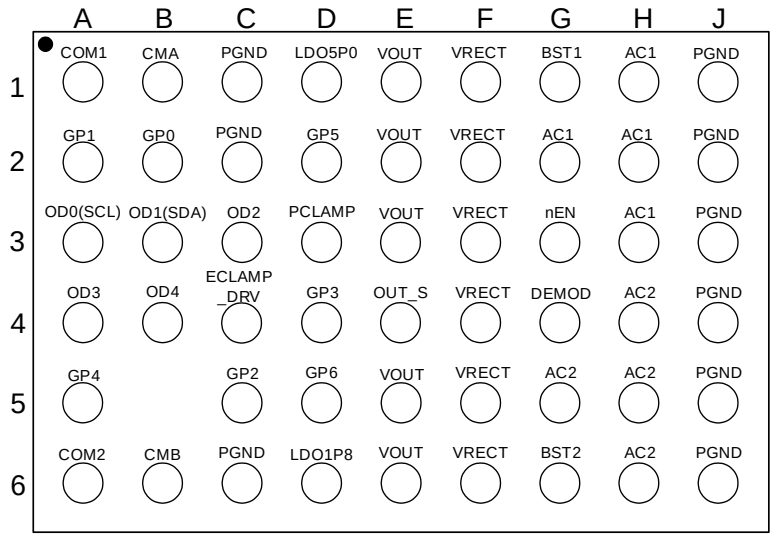
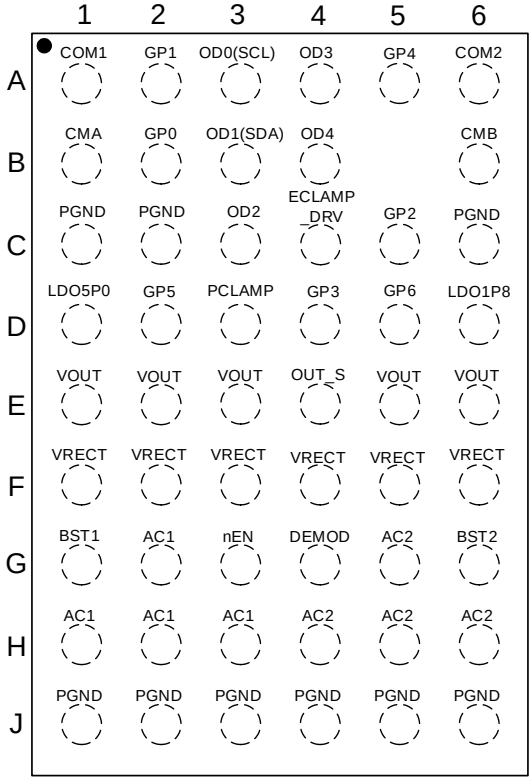
Figure 1. Pin Assignments



P9415 CSP-53 (Ball View)



P9415 CSP-53 (Top View)

2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
A1	COM1	O	High-voltage open-drain modulation FET. Connect a capacitor from AC1 to COM1.
A2	GP1 / Q_MAIN	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin is used to set the default Q factor reported in the EPP mode. Default Q factor = Q factor main (based on GP1 voltage) + Q factor offset (based on GP3 voltage). To use the firmware default Q factor, connect this pin to GND.
A3	OD0 / SCL	I/O	Clock for I2C Serial Interface with AP (SCL). Connect a pull-up resistor to the system I/O supply.
A4	OD3 / ALIGN_X	I/O	AC input for coil alignment guide in the X-direction. This pin can be left floating if not used.
A5	GP4 / I2C_ADDR_SEL	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. The pin is used to select the device I2C slave address. When this pin is pulled to LDO1P8, the I2C Address is 0x3F and when this pin pulled to GND, the I2C Address is 0x3B.
A6	COM2	O	High-voltage open-drain modulation FET. Connect a capacitor from AC2 to COM2.
B1	CMA	O	High-voltage open-drain modulation FET. Connect a capacitor from AC1 to CMA.
B2	GP0 / PWRGD	I/O	Power good output pin. Connect this pin to the application processor (AP). The P9415-R drives this pin HIGH to notify the AP host that received power is good in Rx mode. Tx mode does not use this pin. It can be left floating if not used; do not connect it to the ground.
B3	OD1 / SDA	I/O	Data for I2C Serial Interface with AP (SDA). Connect a pull-up resistor to the system I/O supply.
B4	OD4 / ALIGN_Y	I/O	AC input for coil alignment guide in the Y direction. This pin can be left floating if not used.
B6	CMB	O	High-voltage open-drain modulation FET. Connect a capacitor from AC2 to CMB.
C3	OD2 / $\overline{\text{INT}}$	I/O	Interrupt output pin ($\overline{\text{INT}}$). Connect this pin to the application processor (AP) I/O voltage rail using an external pull-up resistor. The P9415-R drives this pin LOW to notify the AP host of status changes. This pin can be left floating if not used.
C4	ECLAMP_DRV	O	Push-Pull output driver for External Power Clamp FET gate control (Connect a resistor from Vrect to the external FET to GND). This pin can be left floating if not used.
C5	GP2 / THERMISTOR	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be used to measure coil temperature with an external thermistor. The P9415-R interrupts the processor when the coil voltage goes below 0.6V. During the startup phase, this pin is set as a high-impedance. Pull this pin to 1.8V with a resistor if not used (Thermistor).
D1	LDO5P0	O	Internal 5V LDO for chip power only (always On when VRECT is powered). Connect a capacitor to the ground.

Pin Number	Name	Type	Description
D2	GP5 / INHIBIT	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. When this pin is LOW, Rx mode is turned on. When it is HIGH, the P9415-R cannot go into Rx mode. If this pin is driven high in the power transfer phase, an EPT will be sent to the TX. VRECT protection is ON in INHIBIT mode. If not used, connect this pin to GND (INHIBIT). This pin is not used in Tx mode.
D3	PCLAMP	I	High voltage open-drain input for linear clamping during OVP events. Connect a resistor from this pin to VRECT for > 5W operation. Short directly to VRECT for 5W or lower power applications.
D4	GP3 / Q_OFFSET	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin is used to set the default Q factor reported in the EPP mode. Default Q factor = Q factor main (based on GP1 voltage) + Q factor offset (based on GP3 voltage). To use the firmware default Q factor, connect this pin to GND.
D5	GP6 / EPP_DISABLE	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. When this pin is HIGH, Rx EPP mode is disabled and the P9415-R operates in BPP mode. Connect this pin to GND to enable EPP mode by default.
D6	LDO1P8	O	1.8V LDO for Internal Core (always on when VRECT is powered). Connect a capacitor to the ground.
E1, E2, E3, E5, E6	VOUT	O	Main LDO output pin. Connect a capacitor to the ground. Connect an external voltage to this pin in Tx mode.
E4	OUT_S	I	Optional output voltage sensing pin. Connect this pin to VOUT pins.
F1, F2, F3, F4, F5, F6	VRECT	O	Filter cap for the internal rectifier output. Connect a capacitor to the ground.
G1	BST1	O	Bootstrap capacitor for driving high side N-MOSFET of the internal rectifier. Connect a capacitor from AC1 to BST1.
G2, H1, H2, H3	AC1	I/O	Connect to the RX LC tank (due to symmetry may connect to Rx coil or Resonance Capacitor).
G3	nEN	I	Active-low enable pin. When it is pulled-up High by the AP GPIO, the rectifier will be set in Diode mode without ASK signal modulation and the P9415-R is not enabled. While it is pulled-down Low, the rectifier can be set in any predefined modes.
G5, H4, H5, H6	AC2	I/O	Connect to the RX LC tank (due to symmetry may connect to Rx coil or Resonance Capacitor).
G4	DEMOD	I	Tx mode Communication Demodulator input. Connect to LC node via diode and DEMOD filter. This pin can be left floating if TRx mode is not used.
G6	BST2	O	Bootstrap capacitor for driving the high side N-MOSFET of the internal rectifier. Connect a capacitor from AC2 to BST2.
C1, C2, C6, J1, J2, J3, J4, J5, J6	PGND	GND	Power Ground. All PGND pins must be connected tied together externally.

[a] Note: I = Input (Digital or Analog), O = Output (Digital).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the P9415-R at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol/Pins	Parameter	Minimum	Maximum	Units
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	°C
HBM	ESD – Human Body Model	-	2000	V
CDM	ESD – Charged Device Model	-	500	V
CMA, CMB, COM1, COM2, PCLAMP, VRECT, AC1, AC2	Maximum voltage	-0.3	26.5	V
BST1, BST2	Maximum voltage	-0.3	AC1+5, AC2+5	V
LDO1P8, GP0-GP6	Maximum voltage	-0.3	2	V
LDO5P0, DEMOD, nEN, ECLAMP_DRV, OD0-OD4	Maximum voltage	-0.3	6	V
PGND	Maximum voltage	-0.3	0.3	V
VOUT	Maximum voltage	-0.3	21	V
CMA, CMB, COM1, COM2	Maximum RMS current		500	mA
AC1, AC2	Maximum RMS current		2	A
VOUT Output Current	Maximum RMS current		1.9	A

4. Thermal Characteristics

Table 3. Thermal Characteristics[a][b][c][d]

Symbol	Parameter	Value	Units
θ_{JA}	Theta JA. Junction to ambient.	45	°C/W
θ_{JB}	Theta JB. Junction to board.	4.36	°C/W
θ_{JC}	Theta JC. Junction to case.	0.2	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)	MSL 1	-

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

[d] For the WLCSP (AWQ53) package, connecting 8 PGND balls and at least two other CSP balls (10 thermal balls total) to internal/external ground planes from top to bottom sides of the PCB is recommended for improving the overall thermal performance.

5. Electrical Characteristics

V_{RECT} = 5.5 V[a], C_{LDO1P8_OUT} = C_{LDO5P0_OUT} = 2.2µF, C_{MLDO_VOUT} = 10 µF, nEN = 0V, unless otherwise noted. T_J =-5°C to 125°C, Typical values are at 25°C.

Table 4. Device Characteristics

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
V_{RECT} and Under-voltage Lock-out (Rx Mode)						
$V_{IN\_VRECT\_Rx}$[b][e]	V_{RECT} Input Operating Voltage Range Rx		3.5		23.5	V
$V_{UVLO\_RISING\_Rx}$	UVLO Rising Rx	Rising voltage on VRECT, no load		2.55	2.8	V
$V_{UVLO\_HYS\_Rx}$	UVLO Hysteresis Rx	Falling hysteresis voltage on VRECT (LDO shutdown)		150		mV
Over-voltage Protection						
V_{OVP}	Over-voltage Protection	OVP interrupt rising voltage on VRECT (Default setting)		14.7 (BPP) 18 (EPP)		V
$V_{OVP\text{-}HYS}$	Over-voltage Hysteresis			1.5		V
V_{PCLAMP}	Pclamp Over-voltage Protection	Pre-clamp OVP, rising voltage on V_{RECT}		13.2 (BPP) 16.2 (EPP)		V
Quiescent Current						
$I_{RECT\text{-}ACTIVE}$	I_{RECT} Active Current	No external load on VRECT, LDO5P0, LDO1P8; Rectifier not switching		6	15	mA
LDO1P8 Drop Out Regulator (For Internal Usage Only)[f]						
V_{LDO1P8}[f]	LDO1P8 output voltage		1.62	1.8	1.98	V
I_{LDO1P8_LMT}	Current Limit			60		mA
$\Delta V_{LDO1P8\_OUT\_LINE}$	Line Regulation	V_{RECT} = 3.5V to 23.5V, I_{OUT} = 10mA	-5		+5	%
$\Delta V_{LDO1P8\_OUT\_LOAD}$	Load Regulation	I_{OUT} = 1mA to 40mA	-5		+5	%
LDO5P0[c] Drop Out Regulator (For Internal Use Only)						
V_{LDO5P0}	LDO5P0 Output voltage		4.5	5	5.5	V
Main Low-Drop-Out Regulator (VOUT)						
V_{MLDO}	Regulated Output Voltage on VOUT	V_{RECT} = 5.5V, I_{OUT} = 1.33A	4.8	5	5.2	V
		V_{RECT} = 9.5V, I_{OUT} = 1.33A	8.8	9	9.2	V
		V_{RECT} = 12.5V, I_{OUT} = 1.33A	11.75	12	12.25	V
V_{MLDO_STEP}	MLDO Output Voltage Step			100		mV
$\Delta V_{MLDO\_VOUT\_LINE}$	Line Regulation	VRECT = 5.5V to 20.5V, V_{OUT} = 5V, I_{OUT} = 20mA		10	120	mV

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
$\Delta V_{MLDO\_VOUT\_LOAD}$	Load Regulation	I_{OUT} = 20mA to 1.33A, V_{OUT} = 5V		30	90	mV
I_{OUT_MAX}	Maximum IOUT V_{OUT} = 5V to 19V	I_{MLDO_ILMT} (default configuration setting)		1.5		A
FET RDS_{ON}						
R_{DSON_MLDO}	Main LDO			40		mΩ
R_{DSON_RECT}	Rectifier			50		mΩ
$R_{DSON\_CMA/CMB/COM1/COM2}$	Communication A/B/1/2			1		Ω
Input Supplies and UVLO (Tx Mode, V_{IN_VOUT} = 7.5V)						
$V_{IN\_VOUT\_Tx}$[b][d]	V_{OUT} Input Operating Voltage Range Tx		4.5	7.5	12	V
$V_{IN\_UVLO\_Tx}$	Under-Voltage Lockout Tx	V_{IN} Rising, power into VOUT pin		3.1	3.4	V
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			67.5		kSa/s
$V_{IN,FS}$[f]	Full scale Input voltage			2.1		V
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		140		°C
		Threshold Falling		130		°C
Enable Input nEN						
V_{IH}	Input Threshold High		1.6			V
V_{IL}	Input Threshold Low				0.25	V
I_{nEN_LKG}	nEN Leakage Current	V_{nEN} = 0V	-1		1	µA
		V_{nEN} = 5.0V		2.5		µA
Open Drain Inputs/Outputs (SCL, SDA, OD2, OD3, OD4)						
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.5	V
I_{LKG}	Input Leakage Current	V = 0V and 5V; Digital or ADC input mode.	-1		1	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.36	V
Push-Pull General Purpose Inputs/Outputs (GP0, GP1, GP2, GP3, GP4, GP5, GP6)						
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.65	V
I_{LKG}	Input Leakage Current	V = 0V and 1.8V; Digital or ADC input mode	-1.5		1.5	µA

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	I_{OH} = 8mA (for all combined GPIOs)	1.44			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA (for all combined GPIOs)			0.4	V
ECLAMP_DRV Output						
V_{OH}	Output High Voltage	I_{OH} = -4mA	4.0	4.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.6		V
SCL, SDA (I^2C Interfaces SCL (OD0), SDA (OD1)						
f_{SCL}	Clock Frequency				400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
V_{IL}	Input Threshold Low				0.7	V
V_{IH}	Input Threshold High		1.4			V
I_{LKG}	Input Leakage Current	V = 0V and 1.8V, pull-ups disabled	-1		1	µA
V_{OL}	Output Logic Low	I_{OL}= 3mA			0.36	V

[a] V_{RECT} may exceed 23.5V but the device EC table limits are not guaranteed under this condition.

[b] Input Voltage Operating Range is dependent upon the type of Transmitter Power Stage (full-bridge, half-bridge) and Transmitting Coil Inductance. WPC Specifications should be consulted for appropriate input voltage ranges by end product type.

[c] Do not externally load. For internal biasing only.

[d] Full power transfer will not occur at the minimum IC operating specification.

[e] LDO1P8 pin can only be loaded as shown in reference schematics.

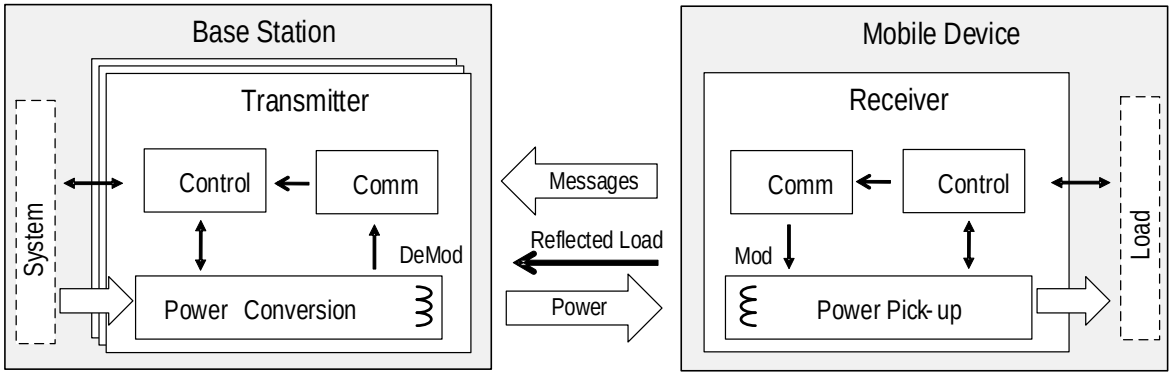
[f] Any open-drain GPIO pin (SCL, SDA, OD2, OD3, OD4) that is connected as an input to the ADC should stay below 2.1V to prevent saturation of the ADC, and any push-pull GPIO pin (GP0, GP1, GP2, GP3, GP4, GP5, GP6) connected to the ADC, the voltage must be ≤ LDO1P8 to avoid interference with the LDO1P8 power supply.

6. Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s), and transmit the power over a strongly-coupled inductor pair (magnetic induction) or over a loosely-coupled inductor pair (magnetic resonance) to a receiver in a mobile device. A WPC[1] system uses near field magnetic induction between coils and can be a free-positioning or magnetically-guided type of system.

In WPC systems, the amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The bit rate for Rx-to-Tx communication link is 2kbps for WPC receivers and is amplitude modulated (ASK) on top of the power link that exists.

Figure 2. Block Diagram of WPC System



[1] For the most current information, see the WPC specification at http://www.wirelesspowerconsortium.com/.

7. Typical Performance Characteristics

The following performance characteristics were taken using a P9243-GB-EVK with WPC MP-A11 coil and P9415-R-EVK evaluation board with default configuration in at T_A = 25°C unless otherwise noted.

Figure 3. System Efficiency vs Output Current, VOUT = 12V

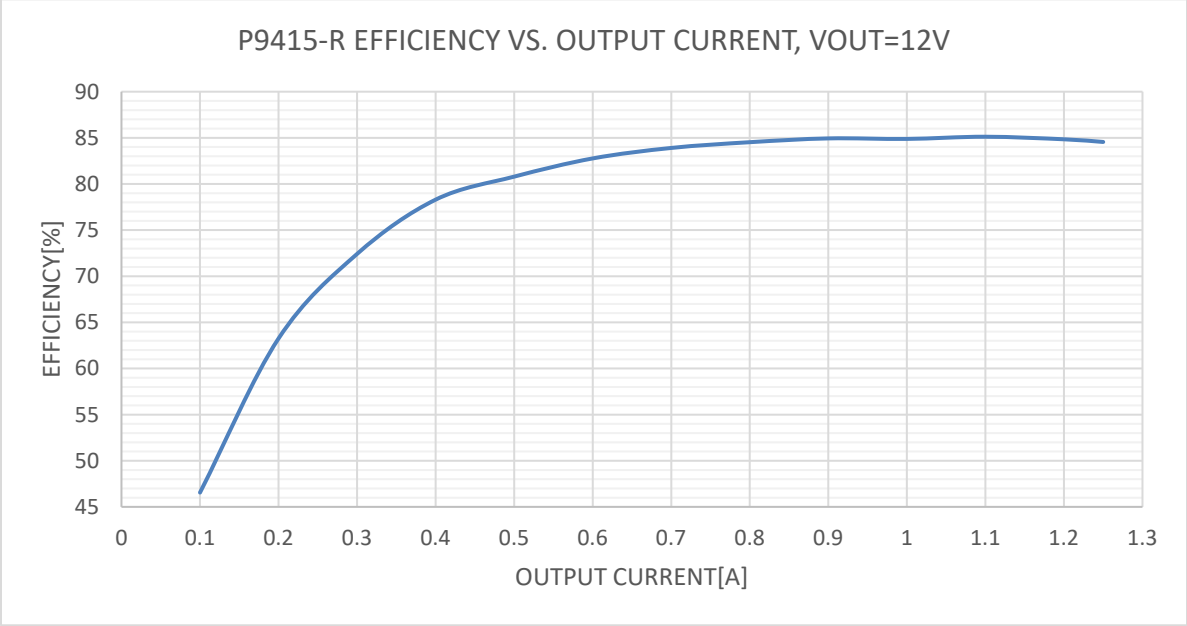


Figure 4. VRECT vs Output Current, VOUT = 12V

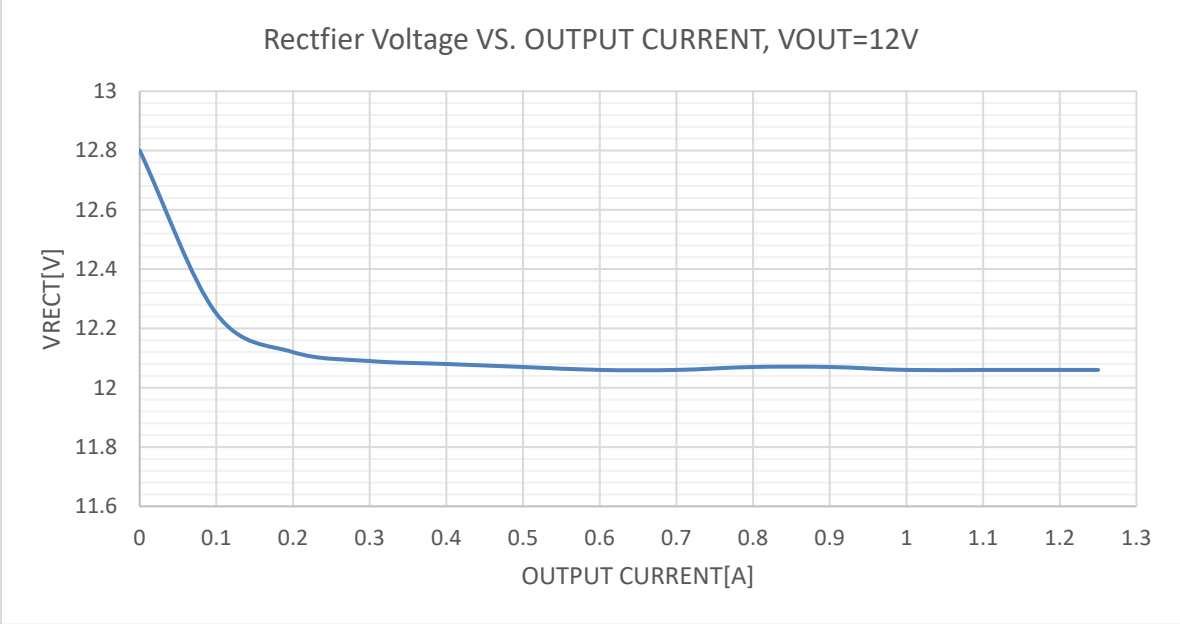


Figure 5. System Efficiency vs Output Current, VOUT = 9V

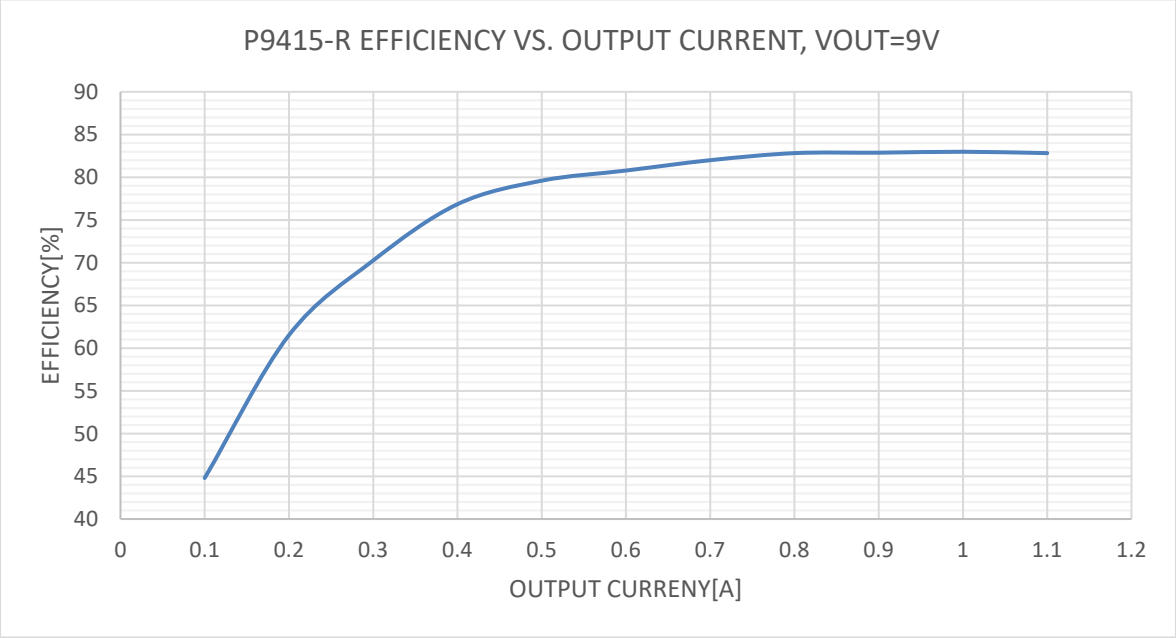


Figure 6. VRECT vs Output Current, VOUT = 9V

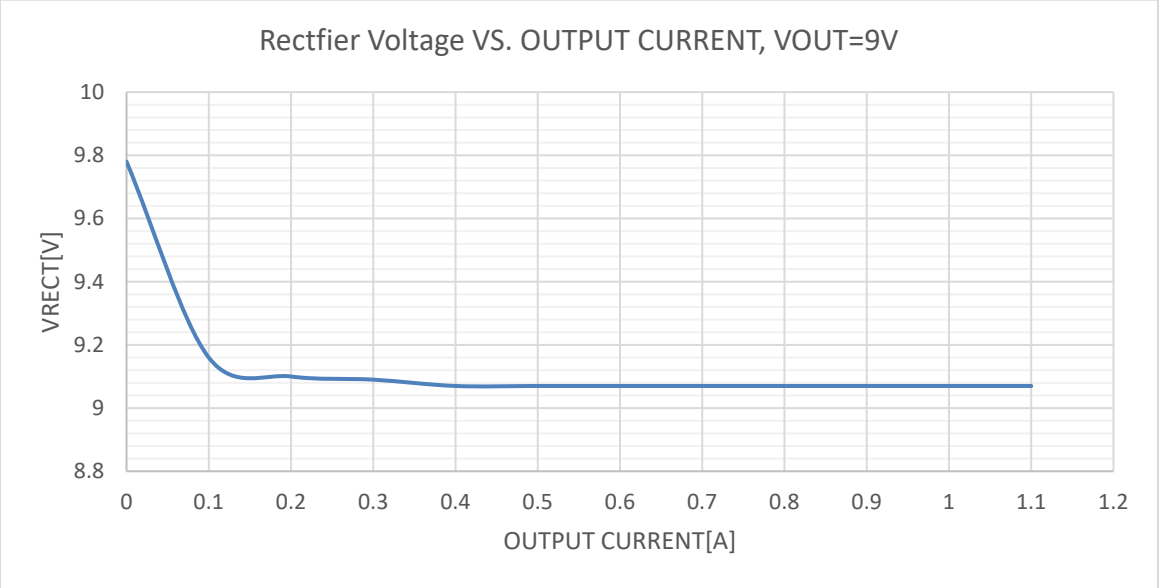


Figure 7. PDIFF (PTX-PRX) vs Iout on NOK9 Transmitter

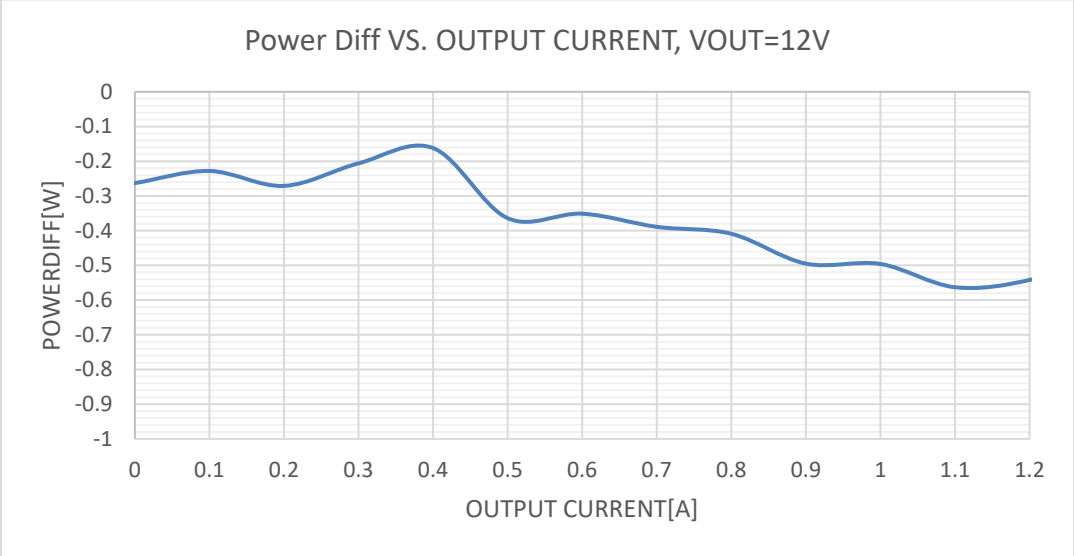


Figure 8. Initial Startup Waveform

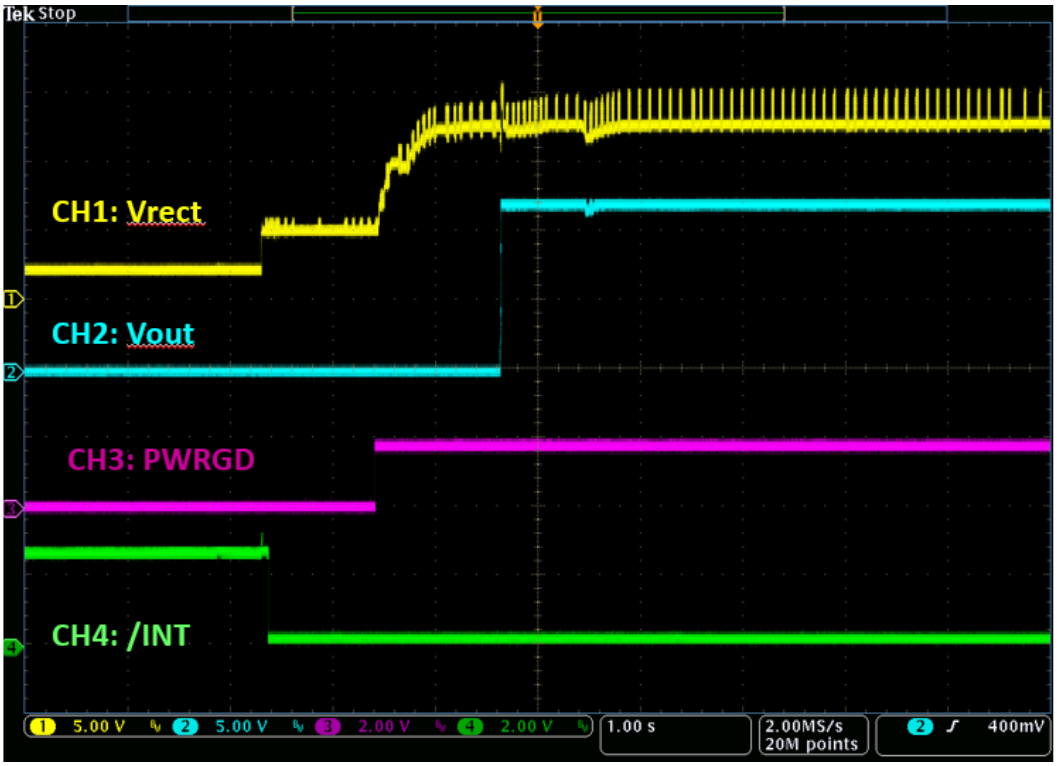


Figure 9. Rx Mode Active Charging Area (Efficiency, 18 x 18 mm)

10	9	8	7	6	5	4	3	2	1	**0**	1	2	3	4	5	6	7	8	9	10 (mm)	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9
0	0	0	0	0	0	0	0	0	80	80	80	80	0	0	0	0	0	0	0	0	0	8
0	0	0	0	0	0	80	81	81	81	81	81	81	80	74	80	0	0	0	0	0	0	7
0	0	0	0	0	81	81	82	82	82	82	82	82	82	81	80	80	0	0	0	0	0	6
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0	0	0	80	81	82	83	83	83	84	84	84	83	83	83	82	81	77	80	0	0	0	4
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0	0	79	80	82	83	83	84	84	84	84	84	84	84	84	84	84	83	82	81	81	0	0	**0**
0	0	80	81	82	83	83	84	84	84	84	84	84	84	84	84	84	83	82	81	80	0	0	1
0	0	79	68	82	83	83	84	84	84	84	84	84	84	84	84	84	83	82	81	80	0	0	2
0	0	79	79	81	82	83	84	84	84	84	84	84	84	84	84	83	83	82	81	80	0	0	3
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0	0	0	0	0	0	79	79	79	80	81	81	81	81	79	80	80	0	0	0	0	0	0	9
0	0	0	0	0	0	0	0	79	80	80	80	80	80	80	0	0	0	0	0	0	0	0	(mm)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Figure 10. Load Transient Response (Iout Change from 0A to 1.3A)

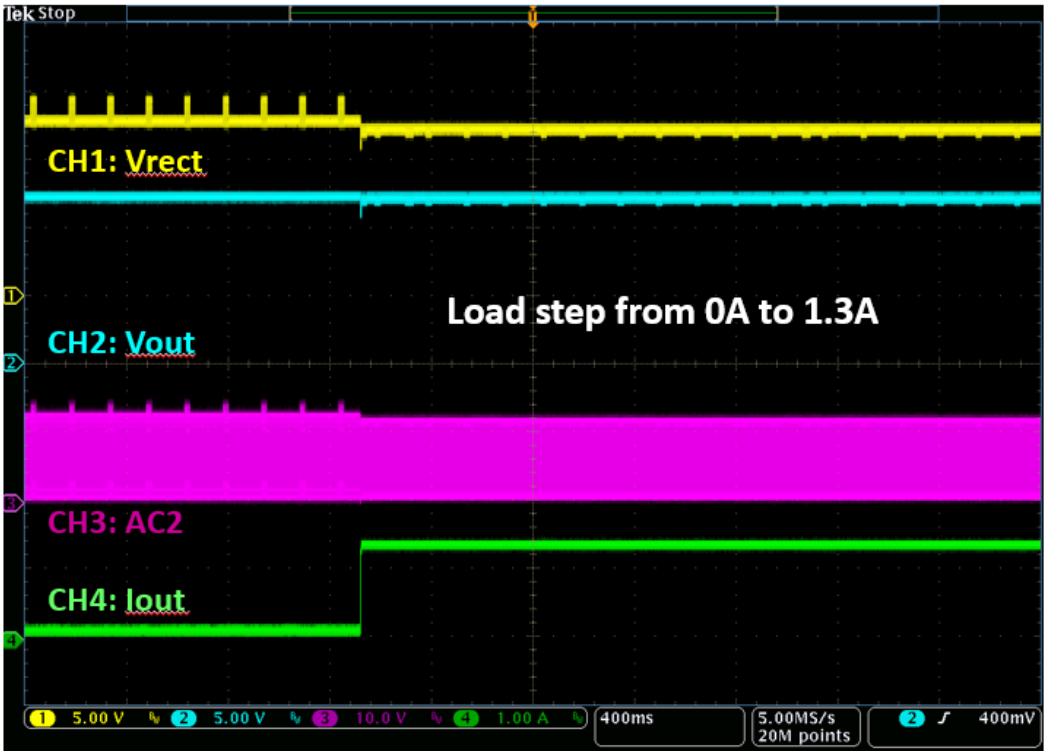


Figure 11. INHIBIT Operation

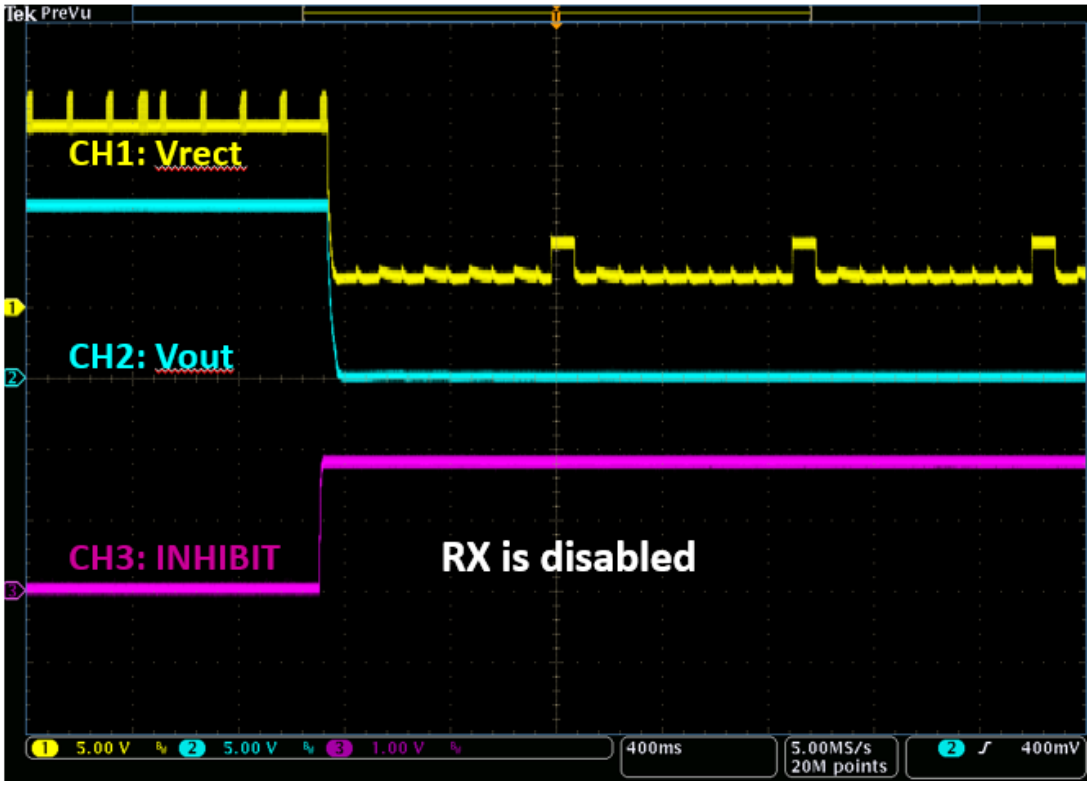


Figure 12. TRx Mode System Efficiency (Test with P9415-R for Rx)

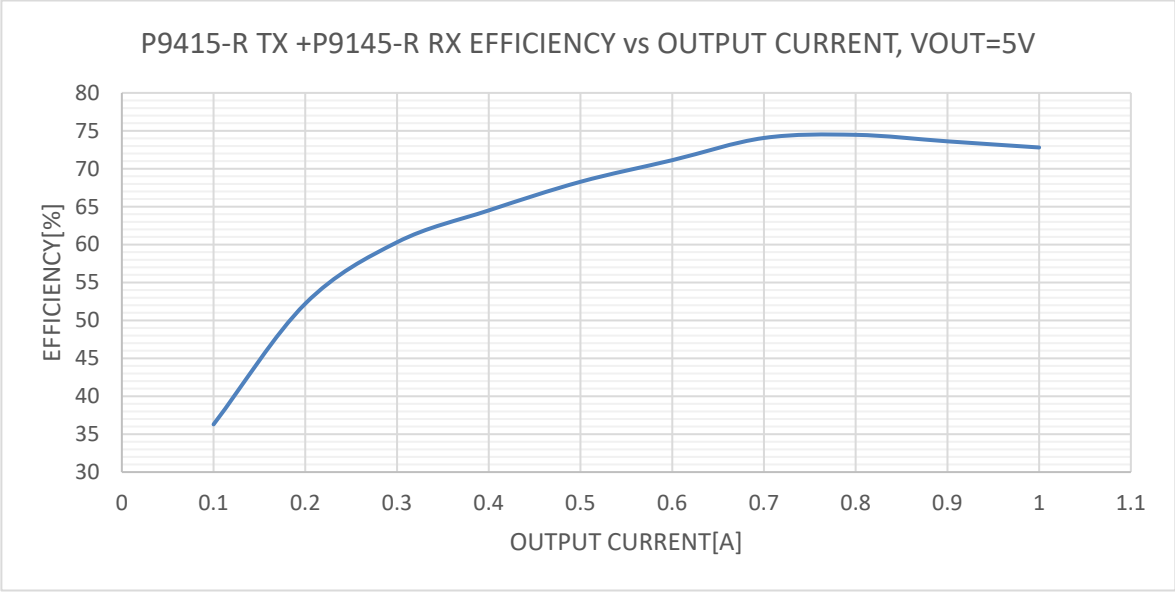
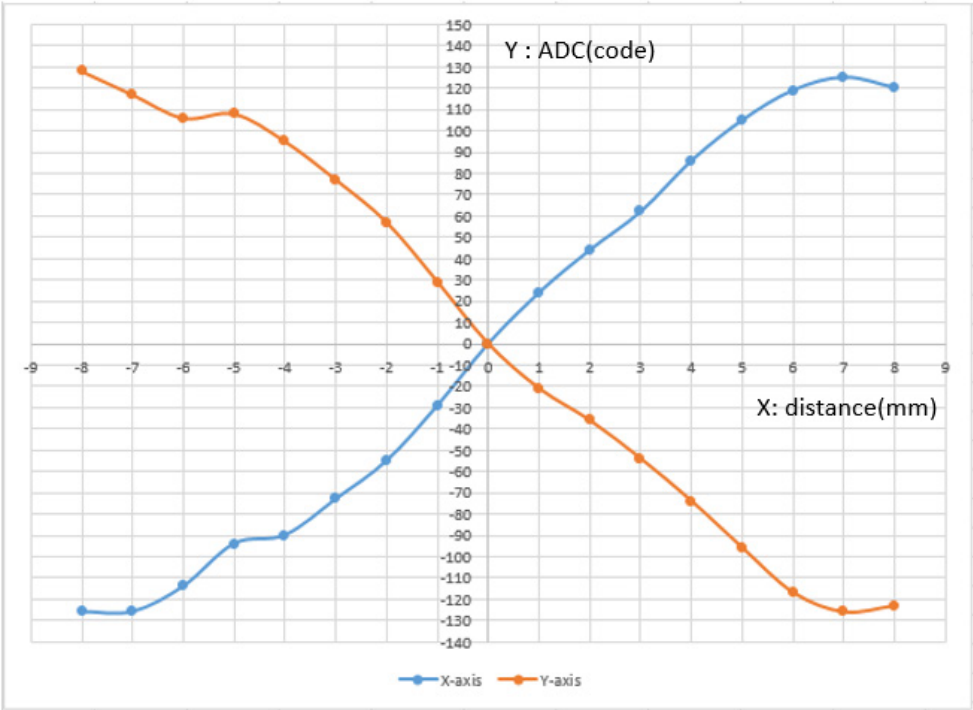


Figure 13. P9415-R TRx Mode Active Charging Area with P9415-R Rx (Efficiency, 17 x 17 mm)

10	9	8	7	6	5	4	3	2	1	0	1	2	3	4	5	6	7	8	9	10 (mm)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	70	70	71	71	70	0	0	0	0	0	0	0	0
0	0	0	0	0	0	70	72	72	72	72	72	72	71	71	70	0	0	0	0	0
0	0	0	0	0	71	72	72	72	73	73	73	73	72	72	71	70	0	0	0	0
0	0	0	0	71	72	72	73	72	72	72	72	72	72	73	72	71	70	0	0	0
0	0	0	69	72	72	73	72	72	72	72	72	72	71	72	72	72	72	0	0	0
0	0	67	71	72	73	72	72	72	73	73	73	73	72	72	72	72	72	71	0	0
0	0	69	72	72	72	72	72	73	73	73	73	73	73	72	71	72	72	72	0	0
0	0	70	71	72	72	72	73	73	73	73	70	73	73	72	71	72	72	71	0	0
0	0	65	71	72	72	72	73	73	73	73	72	73	73	73	72	72	72	71	69	0
0	0	70	71	72	72	72	73	73	72	72	72	73	73	73	72	72	72	71	69	0
0	0	69	71	72	72	72	73	73	73	72	73	73	62	72	71	72	72	71	69	0
0	0	69	71	71	72	71	72	73	73	73	73	73	73	72	71	72	71	70	69	0
0	0	40	71	71	72	71	72	72	73	73	73	73	72	71	72	72	71	71	0	0
0	0	0	69	71	71	72	72	71	72	72	72	71	71	72	72	71	71	0	0	0
0	0	0	67	71	71	71	72	71	71	71	71	71	72	72	71	69	70	0	0	0
0	0	0	0	0	71	71	71	72	72	72	72	72	72	71	71	70	0	0	0	0
0	0	0	0	0	0	70	70	71	71	71	71	71	71	71	70	0	0	0	0	0
0	0	0	0	0	0	0	69	70	71	69	67	71	70	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

10 9 8 7 6 5 4 3 2 1 0 1 2 3 4 5 6 7 8 9 (mm)

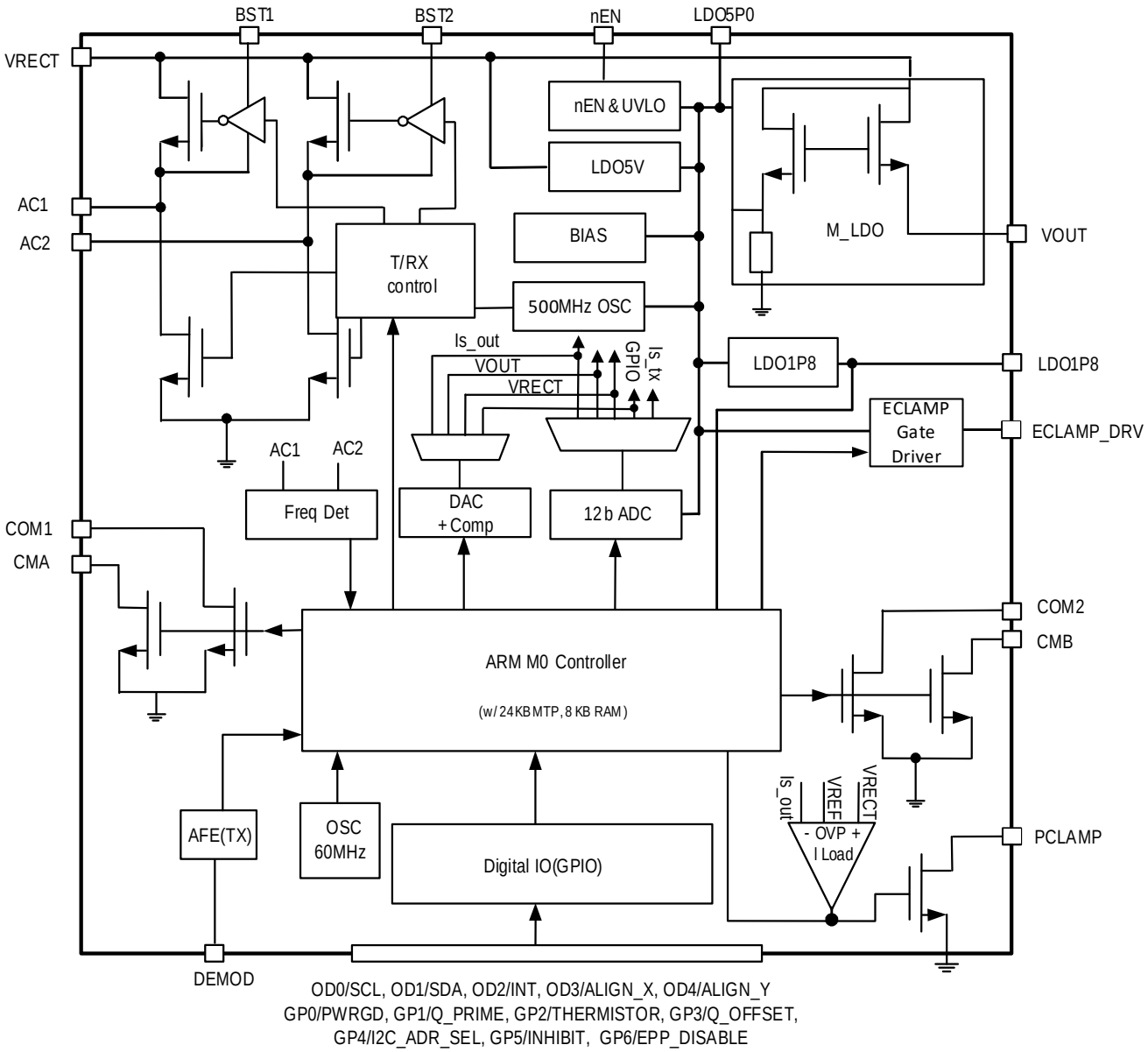
Figure 14. X-Y Alignment



8. Theory of Operation

The P9415-R is a highly integrated wireless power receiver IC for mobile devices. The device can receive up to 15W wirelessly using near-field magnetic induction. The P9415-R Rx will operate in WPC mode when the digital ping frequency is below 190 kHz from the transmitter.

Figure 15. Internal Block Diagram



8.1 Overview

The simplified internal block diagram of the P9415-R is shown in Figure 15. External Rx coil(s) and CS capacitor(s) as shown in Figure 1 transfer energy wirelessly using the P9415-R AC1 and AC2 pins to be full-wave-rectified (AC-to-DC).

The wireless power is stored on a capacitor(s) connected to VRECT. Until the voltage across the VRECT capacitor exceeds the UVLO threshold, the rectification is performed by the body diodes of the Synchronous Full Bridge Rectifier FETs. After the internal biasing circuit is enabled, the Driver and Control block operate the MOSFET switches of the rectifier in various modes to maintain reliable connections at optimal efficiency. An internal ADC monitors the voltage at VRECT and the load current, the P9415-R sends instructions to the wireless power transmitter to increase or decrease the amount of power transferred or to terminate power transmission based on these readings. The voltage at the output of the P9415-R Main Low-Drop-Out (LDO) regulator is programmed up to 20V using I2C commands. The internal temperature is continuously monitored to ensure proper operation.

The voltage at VRECT and the current through the rectifier are sampled periodically and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the internal control logic, which decides whether the loading conditions on VRECT indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at VRECT below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO's load current increases.

8.2 WPC Mode Characteristics

8.2.1 Startup

When a mobile device containing the P9415-R is placed on a WPC "Qi" charging pad, it responds to the transmitter's "ping" signal by rectifying the AC power from the transmitter and storing it on a capacitor connected to VRECT. During the "Ping" phase, once the rectifier voltage at the VRECT pin goes above the UVLO threshold, the digital section of the P9415-R enables communication. The control loop of the P9415-R adjusts the rectifier voltage by sending error packets to the transmitter before and after it enables the VOUT LDO.

The VOUT LDO is enabled when the power transfer mode is initiated and the voltage at VRECT, the output of the full-wave synchronous rectifier reaches the target voltage that includes headroom in addition to the LDO VOUT target voltage. For example, if the VOUT voltage target is 12V, the target VRECT voltage is VOUT + headroom, where the headroom is a function of the output current.

8.2.2 Power Transfer

Once the "identification and configuration" phase is completed and successful "negotiation and calibration" is made, then the transmitter initiates power transfer mode. The P9415-R control circuit measures the rectifier voltage and sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the main LDO linear regulator and to notify the Tx of the current Rectified Power Packet for Foreign Object Detection (FOD) to guarantee safe efficient power transfer. The P9415-R is compatible with the WPC 1.2.4 Specification, and can use compatible Rx coils. Each receiver coil type has a unique inductance value. As such, a unique resonant capacitor (C_S) is used for a given type of receiver coil.

8.2.3 Advanced Foreign Object Detection (FOD) WPC MODE

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of parasitic metal objects are coins, keys, paperclips, etc. The amount of heating depends on the amplitude and frequency of the magnetic field coupled, as well as on the characteristics of the object such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduced power transfer efficiency. Moreover, if no appropriate measures are taken, the heating could lead to unsafe situations if the objects reach high temperatures.

WPC power transmitters and receivers also need to compensate for the power loss due to parasitic metals intentionally designed into the final product: i.e., metals that are neither part of the power transmitter, nor of the power receiver, but which absorb power from magnetic field coupling during power transfer, such as Li-ion batteries, metallic cases, etc.

The P9415-R uses advanced FOD techniques to detect foreign objects placed on or near the transmitter base station. The FOD algorithm includes values that are programmable through either the I²C interface or MTP (Multi-Time Programmable) bits. Programmability is necessary so that the FOD settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the Tx and Rx coils, battery, shielding, and case materials under no load to full load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

The P9415-R FOD values need to be tuned before production for WPC compliance using final production hardware and coils.

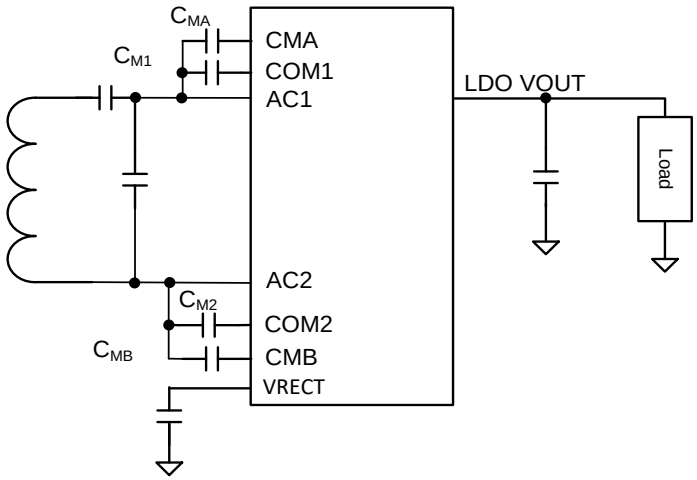
8.2.4 Status/Interrupt Output

When the power transfer connection is established and stable, the VOUT LDO is enabled. GPOD and GPIO pins can be connected to the AP to perform status and interrupt commands.

8.2.5 WPC Modulation/Communication

The P9415-R operates in WPC using a single LC tank Rx coil and requires AC modulation capacitor connections for WPC communication. The LC tank also should be tuned to achieve maximum efficiency (C_{MA}, C_{MB}, C_{M1}, C_{M2} connected to pins CMA, CMB COM1, COM2) in order to accomplish WPC modulation.

Figure 16. Rx Modulation Components



Receiver-to-transmitter communication is completed by modulating the load applied to the receiver's inductor. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. Modulation is done with AC Modulation, using internal switches to connect external capacitors from AC1 and AC2 to ground.

The P9415-R communicates with the base via communication packets or decodes messages sent by WPC Rx's. Each communication packet has the following structure:

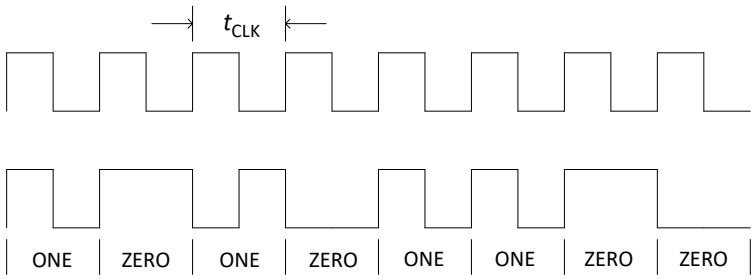
Figure 17. Communication Packet Structure

According to the WPC specification, the power receiver communicates with the power transmitter using backscatter modulation. The load seen by the power transmitter's inductor is modulated on the receiver side to send packets. The power transmitter demodulates these signals as a modulation of coil current/voltage to decode and receive packets.

8.2.6 Bit Encoding Scheme

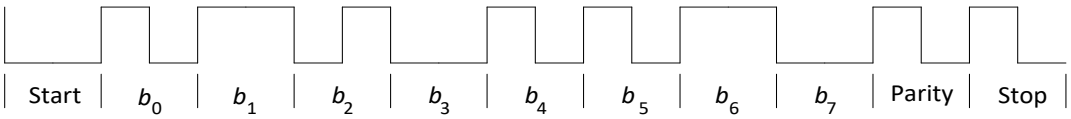
As required by the WPC, the P9415-R uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using two wider transitions as shown below:

Figure 18. Bit Encoding Scheme



Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown below:

Figure 19. Byte Encoding Scheme

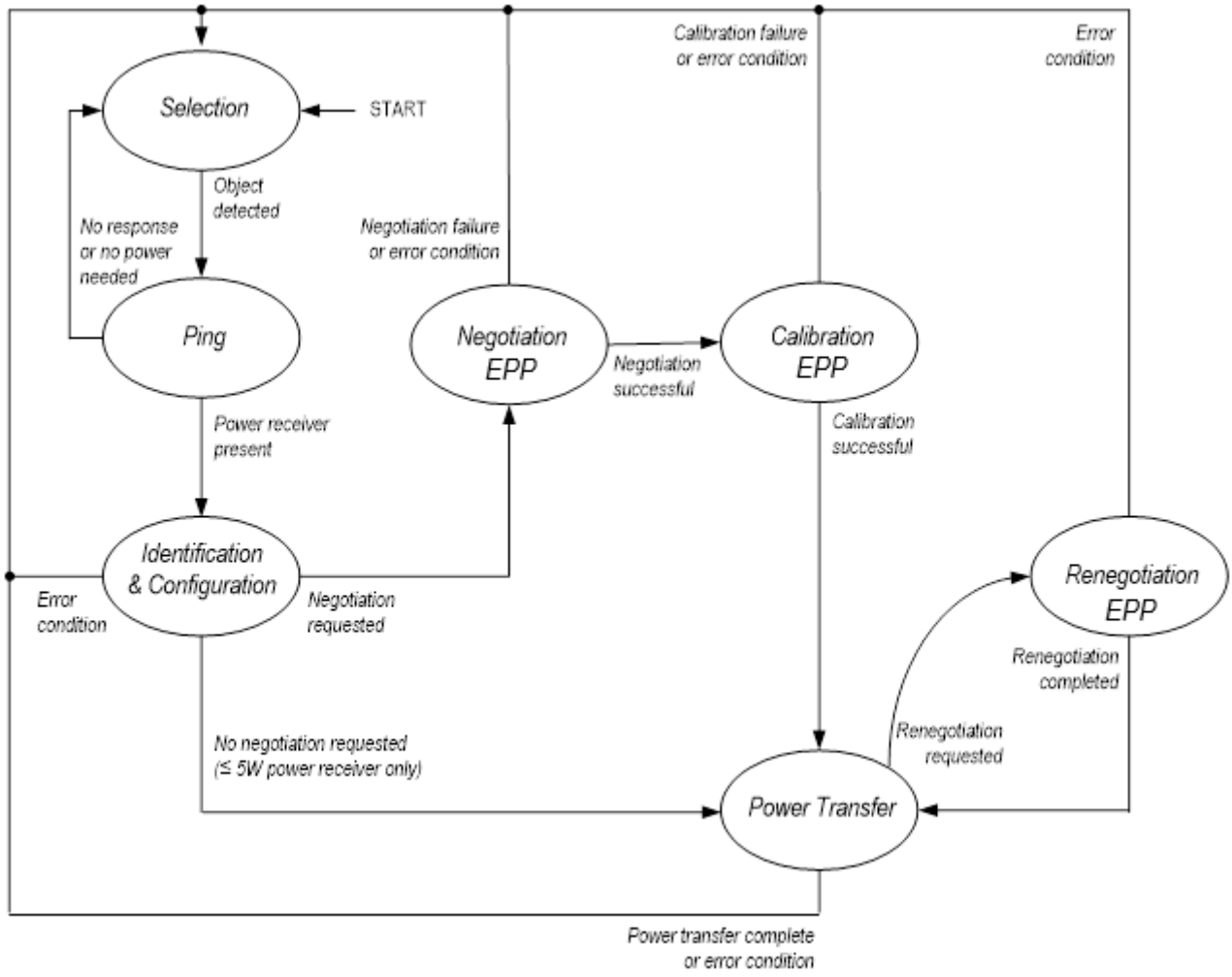


Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

8.2.7 System Feedback Control

The P9415-R is fully compatible with WPC (latest specification) and has all necessary circuitry to communicate with the base station or with a receiver via WPC communication packets. The overall WPC system behavior between the transmitter and the receiver follows the state machine in Figure 20.

Figure 20. WPC System Feedback Control



The P9415-R goes through six phases: Selection, Ping, Identification & Configuration, Negotiation, Calibration, and Power Transfer.

8.2.8 Selection

In this phase, the P9415-R senses or delivers the wireless power and proceeds to the Ping state. It monitors the rectified voltage or DEMOD signal, and when the voltage is above the V_{UVLO_rising} threshold, the P9415-R prepares to communicate with the base station or enter power Ping mode.

8.2.9 Ping

In this phase, the P9415-R transmits a Signal Strength Packet as the first communication packet to instruct the base to keep the power signal ON (or the P9415-R detects a Signal Strength Packet). After sending/receiving the Signal Strength Packet, the P9415-R proceeds to the Identification and Configuration phase. If, instead, an End of Power Packet is sent or an invalid response is sent, then it remains in the Ping phase.

In this phase, the P9415-R sends/expects the following packets:

- Signal Strength Packet
- End of Power Packet

8.2.10 Identification and Configuration (ID and Config)

In this phase, the P9415-R sends or expects the following packets:

- Identification Packet
- Configuration Packet

After the transmission of the Configuration Packet, the P9415-R proceeds to the Negotiation phase.

8.2.11 Negotiation

The Power Receiver negotiates with the Power Transmitter to fine-tune the Power Transfer Contract. For this purpose, the Power Receiver sends negotiation requests to the Power Transmitter, where the Power Transmitter can grant or deny.

8.2.12 Calibration

The Power Receiver provides its Received Power back to the Power Transmitter.

8.2.13 Power Transfer

In this phase, the P9415-R controls the power transfer by means of the following Control Data Packets:

- Control Error Packets
- Rectified Power Packet
- End Power Transfer Packet

8.2.14 Renegotiation

In this phase, the Power Receiver can make adjustments to the Power Transfer Contract, if required. If necessary, this phase can be aborted prematurely without changing the Power Transfer Contract.

8.2.15 End of Power Transfer (EPT)

In the event of EPT, the device turns off the LDO only after the AP instructs the P9415-R to continuously send End of Power (EPT) packets until the transmitter removes the power and the rectifier voltage on the receiver side drops below the UVLO threshold.

8.3 Rx Mode Functions

8.3.1 Synchronous Rectifier

The efficiency of the full-bridge rectifier in the P9415-R is increased by implementing it as a synchronous rectifier. The rectifier comprises four internally-driven switches that work in a full synchronous mode of operation when the load applied to VOUT is higher than the programmed threshold value. Below that threshold, the rectifier works in half-synchronous rectification mode. In half-synchronous rectification mode, only the low-side N-MOSFETs are driven and the high-side N-MOSFETs are forced into diode mode. At power-up, when the voltage is below the UVLO threshold, the rectifier works by using the body diodes associated with the NMOS transistors. The BST capacitors are used to provide power to drive the gates of high-side NMOS switches.

8.3.2 Rectifier and VRECT Level

Once VRECT powers up to greater than UVLO, the full-bridge rectifier switches to half synchronous or full synchronous mode (depending on the loading conditions) to efficiently transfer energy from the transmitter to the load applied to VOUT. The control loop of the P9415-R maintains the rectifier voltage between 5V and 23.5V, depending on the output current (I_{OUT}) and the programmed output voltage. VRECT must not be directly loaded.

8.3.3 Over-Voltage Protection

If VRECT voltage increases above 90% of the OVP voltage set point, the P9415-R turns on the internal clamp to bring the rectifier voltage back to a safe operating level. If the Vrect voltage increases above the OVP voltage set point, the P9415-R sends an interrupt to the AP to notify Over-voltage condition. The internal clamp is released when the VRECT voltage falls below 90% of the OVP voltage set point. The default OVP voltage setpoint is 18.04V for EPP and 14.66V for BPP mode and both are programmable.

8.3.4 Over-Current Protection, Over-Temperature Protection, and Thermal Shutdown

The P9415-R uses over-current (OC) protection and over-temperature (OT) protection by sending an interrupt to the AP if the output current or die temperature exceeds the operating limits.

If an over-current condition exists, over-current Warning interrupt is sent early to the AP before Iout reaches the over-current limit threshold (1.5A default) with the expectation that the AP will respond by reducing the output consumption being drawn from P9415-R. If the output current reaches the over-current limit threshold, Vout starts to drop without increasing current.

If the die temperature exceeds over-temperature threshold1 (default 105°C), the P9415-R first sends an interrupt (OTP) to the AP to alarm over-temperature condition and starts OTP timer (180sec default). If the temperature falls below over-temperature threshold1 – hysteresis, OTP timer resets. If the die temperature keeps increasing and exceeds over-temperature threshold2 (default 120°C) or OTP timer expires, the P9415-R sends an End Power Transfer Packet to the transmitter to terminate a power transfer. If the temperature keeps increasing and exceeds the thermal shutdown threshold (typical 140°C), the P9415-R turns off output LDO.

8.3.5 Enable Input

The P9415-R offers an active LOW enable the function that allows the host AP to control when wireless power will be enabled. When /EN pin is pulled high, the P9415-R is suspended and placed in low current mode. If pulled low, P9415-R is active. /EN pin should never be left floating. In addition, the P9415-R should not be disabled with /EN when the device is in the power transfer phase. Wireless power transfer should be terminated via an EPT command and then once power is removed, /EN high can be asserted.

8.3.6 LDO Regulators

The P9415-R has three LDOs. The Main LDO (VOUT pin) is programmable from 5V to 20V and LDO5P0 is powered by VRECT. LDO1P8 is powered by LDO5P0. Both LDO5P0 and LDO1P8 are used for supplying power to internal low voltage blocks. The LDOs must have local ceramic bypass capacitors placed near the P9415-R.

8.3.7 MLDO Output Enable Conditions

In the BPP mode after entering the power transfer phase, the P9415-R starts sending control error packets with high value to raise the VRECT voltage close to its target value and starts a 2-second timer. The P9415-R enables the MLDO when the VRECT voltage reaches the target voltage or the 2-second timer expires.

In the EPP mode, the P9415-R starts a 5-second timer while exiting the Negotiation phase and waits for the Tx acknowledgment (ACK) in the Calibration Mode1 phase. The P9415-R enables the MLDO when it receives ACK from Tx in Calibration Mode1 phase or the 5-second timer expires.

8.4 WattShare™ (TRx) Mode Functions

The P9415-R can be configured as a wireless power transmitter. The device uses an on-chip full/half-bridge inverter, a PWM generator, a modulator/demodulator for communication, and a microcontroller to produce an AC power signal to drive external L-C tank to operate as a wireless power transmitter (TRx). The P9415-R uses the same L-C tank in both Rx mode and TRx mode.

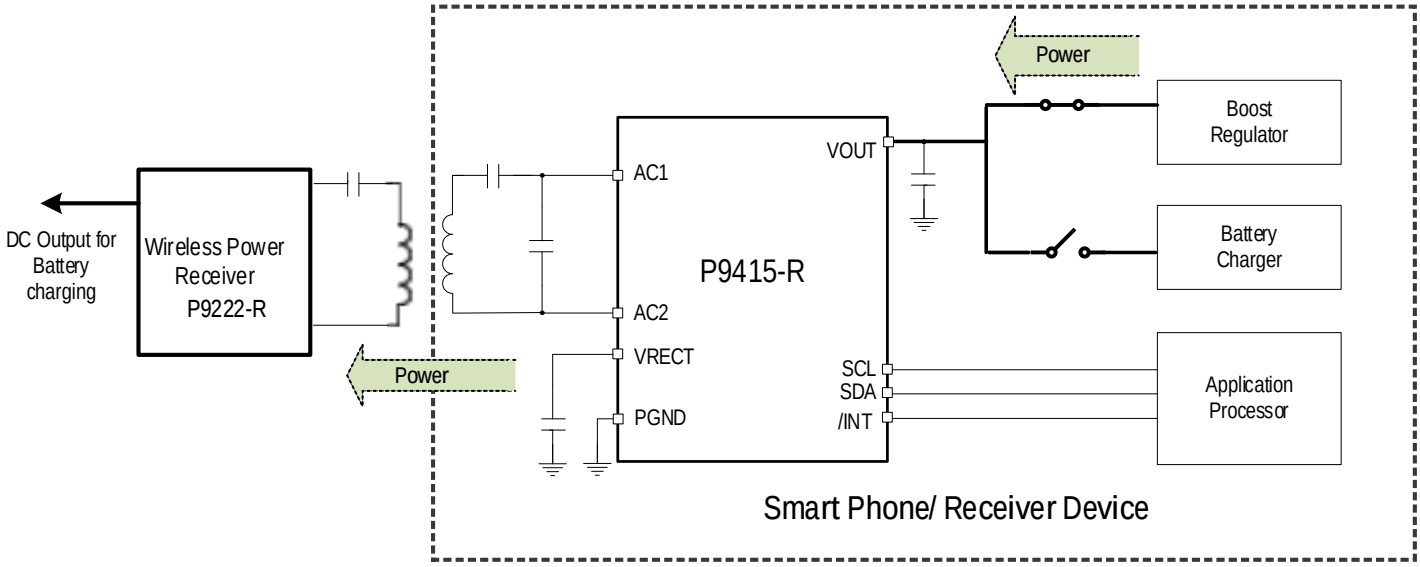
8.4.1 Enabling WattShare™ (TRx) Mode

In TRx mode, the power needs to be applied on the VOUT pin which is the same node as the power receiver output when the device operates in Rx Mode. The Application processor (AP) must adhere to the following procedure to enable TRx mode.

1. AP must ensure that the VOUT pin is not connected to the battery charger. It must enable the power supply on VOUT.
2. AP waits for the interrupt register 0x30 bit 7 (TX_INIT_INT) that indicates TRx mode initialization is finished
3. AP writes 0x0001 to 0x0076 (2 bytes) to enable TRx mode.

The P9415-R starts sending digital pings after enabling TRx mode. The digital ping frequency is 145kHz and the normal operating frequency range is from 130kHz to 145kHz in the default configuration. It can be changed to 110 – 148kHz using the *P9415-R Wireless Power Pro GUI*.

Figure 21. Enabling WattShare™ (TRx) Mode



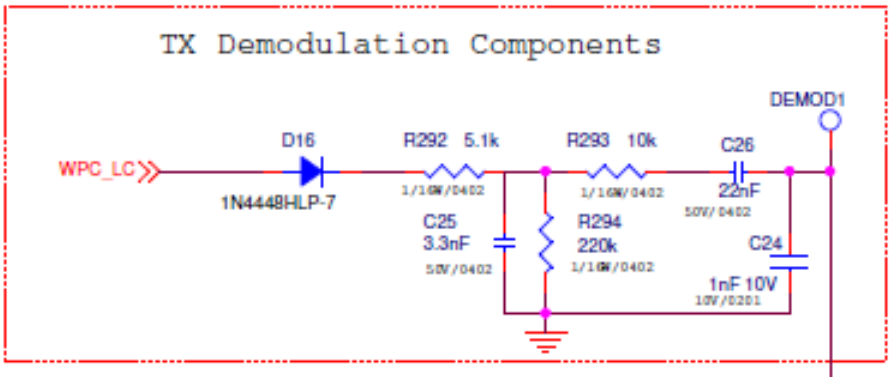
8.4.2 WattShare™ Mode Input Voltage

The P9415-R can transfer up to 5W of power in TRx mode. It follows the WPC 1.2.4 BPP protocol to transfer the power to other Qi-certified receivers such as Mobile devices and Earbud charging cases. The maximum power delivered in TRx mode is dependent on the input voltage on VOUT pin, coil characteristics such as AC resistance, and the friendly metal around the coil. Because the coil used for power transfer in TRx mode has high AC resistance compared to transmitter coil used in a charging pad, the input voltage on the VOUT pin in TRx mode must be around 7 to 9V to deliver 5W of power to the receiver.

8.4.3 Demodulator

In TRx Mode, the Rx sends WPC protocol packets to the P9415-R. Using the demodulation (DEMOD) filter shown in Figure 22 and the internal demodulator circuitry, the P9415-R decodes the ASK modulation packets Rx sent. Based on the packet information, the P9415-R modulates the transmitted power by adjusting the operating frequency or duty cycle and detects a foreign object between Tx and Rx.

Figure 22. WattShare™ Mode Demodulation Filter



8.4.4 WattShare™ Mode Input Under Voltage, Over Voltage, and Current Limit

There are several Over-current Protection thresholds in the WattShare mode that are applied differently depending on the operation phase.

In the ping phase, if the input current exceeds the ping OCP threshold (default 1.1A), the P9415-R sets flag EPT_POCP in TRx End Power Transfer Reason Register (0x0074 2byte), sends an interrupt (EPT_TYPE_INT) to the AP and disables TRX function. TRx will not resume until the AP recycles the power on the VOUT pin and enables the TRx mode again.

In the power transfer phase, if the input current exceeds the IgnoreCepThd (default 1.3A) but less than OCPThd (default 1.5A), the P9415-R enters in CEP Ignore mode. In this mode, bit3 of TRx System Flag Register (0x007B, 1byte) is set and the P9415-R will not respond to the positive CEP from the receiver with the expectation that the receiver detects its Vout drops and decreases the output load. If the input current falls below IgnoreCepThd – IgnoreCepHysteresis (default 0.2A), bit3 of TRx System Flag Register (0x007B, 1byte) is cleared, and the P9415-R operates in normal TRx mode and responds to positive CEP normally.

If the average input current exceeds OCPThd or instant input current exceeds OCPThdFast (default 1.8A), the P9415-R sets flag EPT_OCP in TRx End Power Transfer Reason Register (0x0074, 2byte), sends an interrupt (EPT_TYPE_INT) to the AP and disables TRx function. TRx will not resume until the AP recycles the power on the VOUT pin and enables the TRx mode again.

If the voltage on the VRECT pin is higher than the over-voltage protection (OVP) threshold (default 11V), the P9415-R sends interrupt (EPT_TYPE_INT) to AP, sets the EPT_OVP bit of TRx End Power Transfer Reason Register 0x0074(2 bytes), and disables the TRx function. If the voltage on the VRECT pin is lower than (OVP threshold – OVP hysteresis (1.5V), the P9415 clears the EPT_OVP bit. If the EPT_OVP bit is set, the TRx function cannot be enabled.

If the voltage on the VOUT pin is lower than the low voltage protection (LVP) threshold (Default 4V), the P9415-R sends interrupt (EPT_TYPE_INT) to AP, sets EPT_LVP bit of TRx End Power Transfer Reason Register 0x0074(2 bytes), and disables the TRx function. There is an internal digital filter to avoid false triggering of LVP for small voltage dips. TRx will not resume until AP recycles the power on the VOUT pin and enables the TRx mode again.

8.4.5 Transmitter Conflict in WattShare™ Mode

When the P9415-R is in WattShare™ mode, users might accidentally place the P9415-R on another WPC transmitter. The pings from the WPC transmitter will generate an AC voltage in the resonant tank connected to the P9415-R. The P9415-R detects this voltage, sends an interrupt (GET_DPING_INT in 0x30[6]) to the AP, and exits TRx mode. The AP must disable the external power supply connected to the VOUT pin of the P9415-R.

9. Applications Information

9.1 External Components

The P9415-R requires a minimum number of external components for proper operation. For more information, see Figure 26 and Table 6 and *AN-998 Determining critical component values for Wireless Power Receivers*.

9.2 Rx Wireless Power Coil

The Rx coil is dependent on customer requirements and most are custom designs. Renesas recommends the following measured values for Rx-only coils:

- Ls = 8 to 10µH
- DCR = < 0.3Ω
- ACR = < 0.4Ω

Table 5. Recommended Coil Manufacturer

Output Power	Vendor	Part Number	Inductance at 100kHz	Resonant Caps (Cs)	DC Resistance at 20℃
15W	Luxshare	ICTR-QS5858031L-MW034	9.0±0.2µH	400nF	195mΩ+/-10%

9.3 Resonance Capacitors

The series resonance capacitors (C32, C33, C34, C36, and C37) are critical components and must be chosen carefully. All current that flows to the load flows through these components plus any current loss in the rectifier AC to DC conversion. The recommended capacitor is the 100nF Murata (GRM155C71H104KE19, X7S, 50V, or GRM155R61H104KE19, X5R, 50V), which have an ESR < 0.1ohms at 100kHz. The GRM155C71H104KE19 capacitor is the best choice based on ESR value and DC bias effects. If another capacitor is chosen, inspecting the ESR vs. Frequency curve of the manufacturer's capacitor datasheet is necessary to compare ESR characteristics as well as the DC bias effects on the capacitor value. Adding non-populated (NP) component placement (C37) is advised if the additional capacitance is needed for a particular Rx coil.

9.4 Input Capacitor (VRECT Capacitors)

The LDO input capacitors (VRECT capacitors) should be located as close as possible to the VRECT pins and ground (PGND). Ceramic capacitors are recommended for their low ESR and small profile.

9.5 Output Capacitor (VOUT Capacitors)

The output capacitor connection to the ground pins (PGND) should be made as short as practical for maximum device performance. Because the LDO is designed to function with very low ESR capacitors, a ceramic capacitor is recommended for the best performance. For better transient response, the total amount of output capacitance should be increased to meet the output voltage variation target of the application (VRECT capacitance might need to be increased as well).

9.6 LDO1P8 Capacitor

The P9415-R has an internal LDO regulator that must have at least a 1µF to 2.2µF capacitor connected from the LDO1P8 pin to PGND. This capacitor should be as close as possible to the LDO1P8 pin with a close GND connection. A 0.1µF capacitor in a 0201 or 0402 size package can be added for improved high-frequency decoupling of the LDO1P8 power rail because this voltage powers the internal ARM Cortex-M0 processor.

9.7 LDO5P0 Capacitor

The P9415-R has an internal LDO regulator that must have at least a 1µF to 2.2µF capacitor connected from the LDO5P0 pin to PGND. This capacitor should be as close as possible to the LDO5P0 pin with a close PGND connection. A 0.1µF capacitor in a 0201 or 0402 size package can be added for improved high-frequency decoupling of the LDO5P0 power rail because of this voltage powers the internal ADC and UVLO circuits.

For additional power savings at higher input voltages, an external 5V supply should be connected to supply power to the P9415-R via the LDO5P0 pin. The applied voltage to this pin must be > LDO5P0 regular output voltage to power the low-voltage circuitry from the external 5V supply, while the external 5V supply should be between 5.2V to 5.5V.

9.8 PCLAMP Connection

The P9415-R has an internal automatic DC clamping feature to protect the device from events that cause high voltages to occur on the AC or DC side of the rectifier. The clamping engages by the VRECT connection to the PCLAMP pin. The VRECT node must be connected to the PCLAMP pin at all times during Rx mode operation. For greater than 5W operation, the VRECT node is connected to the PCLAMP pin using a 50Ω to 100Ω resistor with greater than 1/4W rating with 2.5x or greater over-power surge capability. For space-constrained designs, the PCLAMP pin can be directly connected to the VRECT node for 5W or lower power operation.

Also, there is an option for external FET and resistor clamping by the use of the ECLAMP_DRV pin which can output 5V to drive the gate of external MOSFET. This output is synchronized with the internal PCLAMP signal. ECLAMP_DRV can provide additional clamping capability as needed and there is no thermal increase in the IC side because clamping energy is consumed in external components.

9.9 Transient Voltage Suppressors

The Transient Voltage Suppressor (TVS) is an active device that will direct high voltages from the input to ground, thus protecting the wireless power device or other downstream ICs from being exposed to high voltages.

Transient Voltage Suppressor diodes should be added to the design from the AC1 and AC2 nodes to GND or from AC1 to AC2. These components are useful to rapidly limit incoming ESD surges or situations when the TX incoming power exceeds the expected power and VRECT voltage rises above target and Over-voltage protection threshold in less than 10µs to aid in voltage limiting the incoming AC waveforms in conjunction with the PCLAMP power limiting circuitry.

A balance in Reverse Standoff Voltage (VRWM), Clamping Voltage (VCL), Break-down Voltage (VBR) relative to the expected Vrect operating voltage Vrect (be sure minimum VBR is less than maximum operating Vrect value and that VCL is less than Vrect Absolute maximum voltage) should be reached.

Table 6. Transient Voltage Suppressors (TVS) Recommendations

V_{MLDO} = 12V D24V0L1B2LP
VRWM = 24V maximum
VBR = 26V minimum at 1mA
VCL = 42V maximum at 1A pp

9.10 GPIO Pins

The P9415-R has general-purpose input-output (GPIO) pins. The OD0-OD4 and GP0-GP6 pins are all multi-functional.OD0-OD4 pins have an open-drained structure and GP0-GP6 pins have a push-pull structure.

9.10.1 OD0/SCL Pin

The OD0 pin has a digital function open-drain structure. It is assigned to SCL of the I2C function for the serial interface between the AP and the P9415-R. An external pull-up register on the SCL line is required for I2C communication. OD0 can operate up to 5V.

9.10.2 OD1/SDA Pin

The OD1 pin is set as a digital function open-drain structure. It is assigned to the SDA function of the I2C serial interface bus between the AP and the P9415-R. An external pull-up resistor on the SDA line is required for I2C communication. OD1 can operate up to 5V.

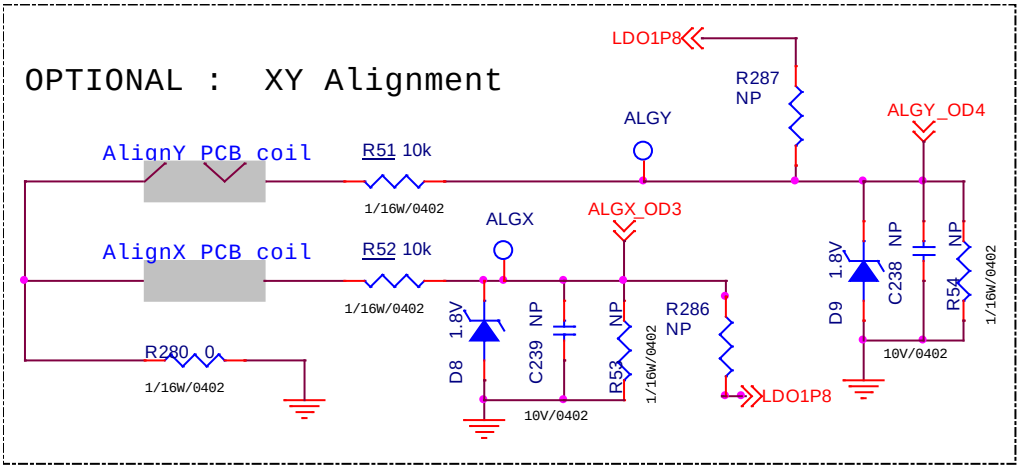
9.10.3 OD2/INT Pin

The OD2 pin is set as a digital function open-drain structure. It is assigned as the /INT signal for interrupt notification to the AP. /INT pin indicates a major change of states or error modes such as over-current, over-voltage, or over-temperature event. Connect this pin to the AP I/O voltage rail using an external pull-up resistor. The P9415-R drives this pin LOW to notify the AP of status changes.

9.10.4 OD3/ALIGN_X Pin and OD4/ALIGN_Y Pin

The XY alignment feature allows the P9415-R to sense its relative position to the Tx coil magnetic field center. When used, the XY alignment coils should be connected to pins OD3(X-alignment coil input) and 0D4 (Y-alignment coil input). These signals are internally rectified, filtered, and sensed through the ADC. The ADC values that represent Align X coil signal strength and Align Y coil signal strength can be read in 0x38 and 0x39 registers respectively.

Figure 23. Typical XY Align Coil Schematic Level Connection Guide



9.10.5 GP0/PWRGD Pin

The GP0 pin is a digital output referenced to LDO1P8. The AP can use the power good signal to turn on the charging connection indicator or other system functions. Power good (PWRGD) pin is pulled low by default. In BPP mode, the power good pin is pulled high when MLDO is enabled. In EPP mode, the power good pin is pulled high at the end of the negotiation phase by default. It can be configured to be pulled high when MLDO Vout is enabled.

9.10.6 GP1/Q Main Pin and GP3/Q Offset Pin

If both GP1 and GP3 are low (< 0.2V), the P9415-R reports the default value programmed in the firmware. Q is 30 in the default configuration and can be changed with a P9415-R Wireless Power Pro GUI; otherwise, the default Q factor value is decided by the following tables.

Table 7. Q Factor Main – GP1

GP1 ≥ Vmin	GP1 < Vmax	Q_Main	Pup(R)	Pdown(R)
0.2	0.55V	30	100K	27K
0.55V	0.90V	40	100K	68K
0.90V	1.25V	50	100K	150K
1.25V	1.60V	60	47K	180K
1.60V	1.98V	70	47K	NP

Table 8. Q Factor Offset – GP3

GP3 ≥ Vmin	GP3 < Vmax	Q_Offset	Pup(R)	Pdown(R)
0V	0.2V	+0	NP	47K
0.2	0.55V	+1	100K	27K
0.55V	0.90V	+2	100K	68K
0.90V	1.25V	+4	100K	150K
1.25V	1.60V	+6	47K	180K
1.60V	1.98V	+8	47K	NP

For example, if both GP1 and GP3 are pulled up, the reported Q factor value is 78(70+8). The AP can also change the reported Q factor by writing to register 0x55 before the negotiation phase.

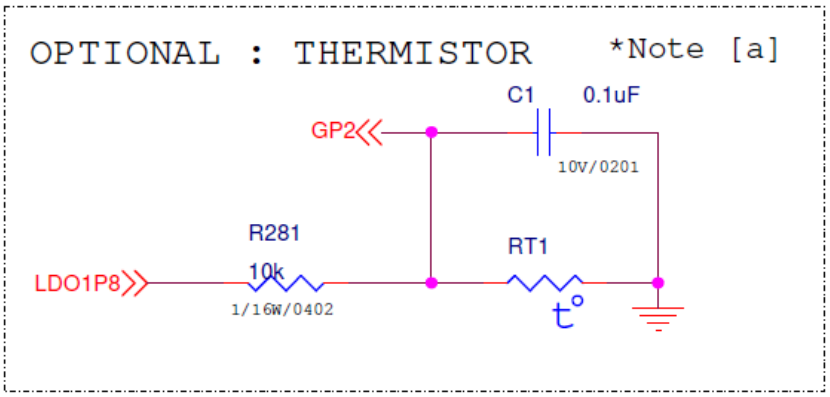
9.10.7 GP2/Thermistor Pin

The GP2 pin is connected to the internal ADC and can measure the voltage of the thermistor connected to measure the external temperature on either the receiver coil or the PCB. The P9415-R sends interrupts to the AP if the voltage reaches below the threshold level (0.6V default, configurable) to allow the AP an opportunity to reduce the temperature and prevent power transfer interruptions. The AP must convert the ADC value into a pin voltage using the below equation. Voltage can be converted into temperature information based on the thermistor manufacturer datasheet information.

Equation 1

Voltage on GP2 Pin in mV = (Register 0x42 [11:0] Data / 4095) * 10 * 2.1

Figure 24. GP2 Pin External Connection to Thermistor Configuration



9.10.8 GP4/I2C Address Select Pin

The pin is used to select the P9415-R device I2C slave address. When this pin is pulled high to LDO1P8, I2C Address is 0x3F and when this pin pulled low to GND, I2C Address is 0x3B (default). The slave address is a 7-bit I2C address.

9.10.9 GP5/INHIBIT Pin

The GP5 / INHIBIT pin is a digital input referenced to LDO1P8 and gets polled during the startup. When the INHIBIT pin is low, the Rx mode is enabled. Pulling the INHIBIT pin high will prevent the P9415-R from connecting to the transmitter. The AP can use this pin to safely enable and disable wireless power transfer function with proper VRECT node protections. If this pin is driven high in the power transfer phase, the P9415-R will send an End Power Transfer packet to the transmitter and wireless power transfer will be disabled while Vrect protection is alive.

9.10.10 GP6/EPP_DISABLE Pin

The GP6 is assigned as a digital input referenced to LDO1P8. When the EPP_DISABLE pin is high, the Rx EPP mode is disabled and the P9415-R operates in BPP mode. When it is low, the Rx mode is determined by the internal mode configuration setting value in the firmware. If not used, connect this pin to ground.

9.11 Foreign Object Detection

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign object could become heated to an unsafe temperature.

In the Extended Power Profile, there are two methods of foreign object detection (FOD). One is by measuring the system quality factor before entering the power transfer phase, and the other is to measure the power loss difference between the received power and the transmitted power during the power transfer phase. Before entering the power transfer phase, the P9415-R sends a reference Q-factor (default 30) in the negotiation phase. The transmitter measures the Q-factor on its coil and compares it with the reference Q-factor provided by the P9415-R. If the difference is large, the transmitter presumes that there is a foreign object (FO) between the Tx and Rx and shuts down. The power loss foreign object detection method is used in both the Extended Power Profile (EPP) and the Basic Power Profile (BPP) modes power transfer phase. During the power transfer phase, the P9415-R continuously sends to the transmitter the amount of power received using the Received Power Packet (RPP). The transmitter will compare the RPP packet information received from the receiver with its measured transmitted power. If there is a significant difference the transmitter presumes that there is a foreign object (FO) between Tx and Rx that is absorbing the transmitted power and will stop the power transfer to avoid heating of FO.

9.11.1 FOD Parameters in Receiver Mode

For a WPC power loss foreign object detection to function effectively, the receiver must account and compensate for all of their known losses. Such losses, for example, could be due to resistive losses or nearby metals that are part of the receiver. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (PPR) in an RPP. The maximum value of the received power accuracy $P\Delta$ depends on the maximum power of the power receiver as defined in Table 9.

The power receiver must determine its PPR with an accuracy of $\pm P\Delta$, and report its received power as PRECEIVED = PPR + $P\Delta$. This means that the reported received power is always greater than or equal to the transmitted power (PPT) if there is no foreign object (FO) present on the interface surface.

Table 9. Recommended Maximum Estimated Power Loss

Maximum Power (W)	Maximum $\boldsymbol{P\Delta}$ (mW)
5	350
10	500
15	750

The compensation algorithm includes parameter values that are programmable either internal register or customer configuration table in MTP. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

FOD parameters consist of eight sections. Each section is divided by output current and consists of gain and offset to compensate for Rx internal power loss; each section is also adjusted for Reported Rx power. The following comprises the Rx load current ranges for the FOD sections.

- FOD section [0] is from 0mA to section 0 current mA
- FOD section [1] is reserved for test
- FOD section [2] is from section 0 current mA to 351mA
- FOD section [3] is from 352mA or section 0 671mA
- FOD section [4] is from 672mA to 863mA
- FOD section [5] is more than 864mA

Section 0 current is the point where the internal rectifier changes bridge configuration from half-bridge to full-bridge. In the default configuration, If VOUT is set to less than 7V, section0 current is 288mA. If Voutset is higher than 7V, section0 current is 384mA, section2 is not used and section3 starts from 384mA. There is around ±30mA load current hysteresis for changing the FOD sections. These settings can be changed using the *P9415-R Wireless Power Pro GUI.*

The formula of Rx Reported Power is:

$$Rx\ Reported\ Power[0..5] = Power(Rx\ delivered\ power) * FOD\ Gain[0 \ldots 5] + Offset[0..5]$$

Place the receiver with the P9415-R on the Nok9 FOD transmitter. Ramp the current on the output of the P9415-R in steps of 50mA to 100mA and monitor power difference between the Nok9 transmitted power and the receiver reported power value. The difference should be within maximum Power loss delta in Table 9. If the difference exceeds the maximum power loss delta, adjust the FOD gain or FOD offset of that particular output current section to bring the difference back to within range. The AP can modify the FOD gain and FOD offset by writing to the Foreign Object Detection Customer Registers (0x68-0x77). In the final product, the AP can use the VRECTON interrupt or battery charger interrupt as a trigger to update the FOD registers.

9.11.2 FOD Parameters in Transmitter Mode

For a WPC power loss foreign object detection to function effectively, the transmitter must set the FOD threshold at a reasonable value by accounting all its known losses such as Coil resistance loss and losses because of metal around the coil integrated into the product. In the power transfer phase, the P9415-R will continuously calculate the difference between its measured transmitted power and RPP packet information received from the receiver. If the difference is higher than the FOD threshold, the P9415-R presumes that there is a foreign object (FO) between Tx and Rx that is absorbing the transmitted power and will stop the power transfer to avoid heating of FO.

FOD threshold value changes based on the Received Power Packet value (RPP) from the receiver. In the default configuration, If RPP is larger than 3700mW (FodSegThd), the FOD threshold is -100mW (FodThdH) and if RPP is less than 3700mW, the FOD threshold is 800mW (FodThdL)

The FodSegThd, FodThdH, and FodThdL are configurable by config table in MTP using the *P9415-R Wireless Power Pro GUI*.

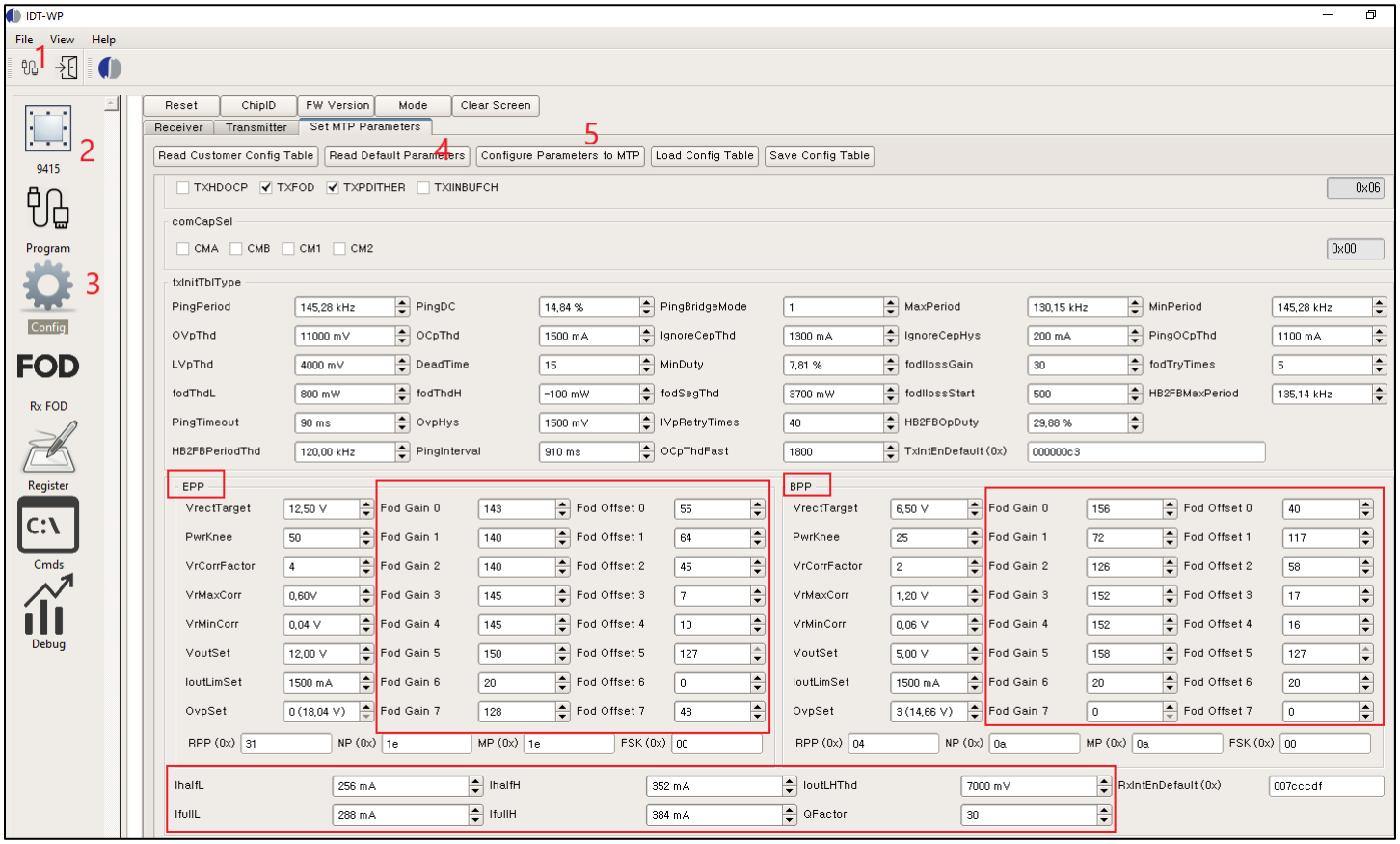
FOD criteria: FOD threshold > Transmitted Power (PPT) – Received Power (RPP)

9.11.3 FOD Parameters Configuration with P9415-R GUI

The default values of the FOD parameters in MTP can be configured by the following procedure.

1. Provide external power supply (+5V) on the P9415-R VOUT pin.
2. Launch the *P9415-R Wireless Power Pro GUI* after connecting WPD–USB-DONGLE to the computer.
3. Click #1 to connect the GUI with the P9415-R device and the P9415 device name in should be displayed at #2 on the successful connection.
4. Click the Config Icon in #3 and the Read Default Parameters in #4.
5. Enter new FOD parameter values and click Configure Parameters to MTP
6. Remove the external power supply and place the receiver with P9415-R on the Nok9 transmitter or a target transmitter and verify if new parameters.

Figure 25. P9415-R Wireless Power Pro GUI



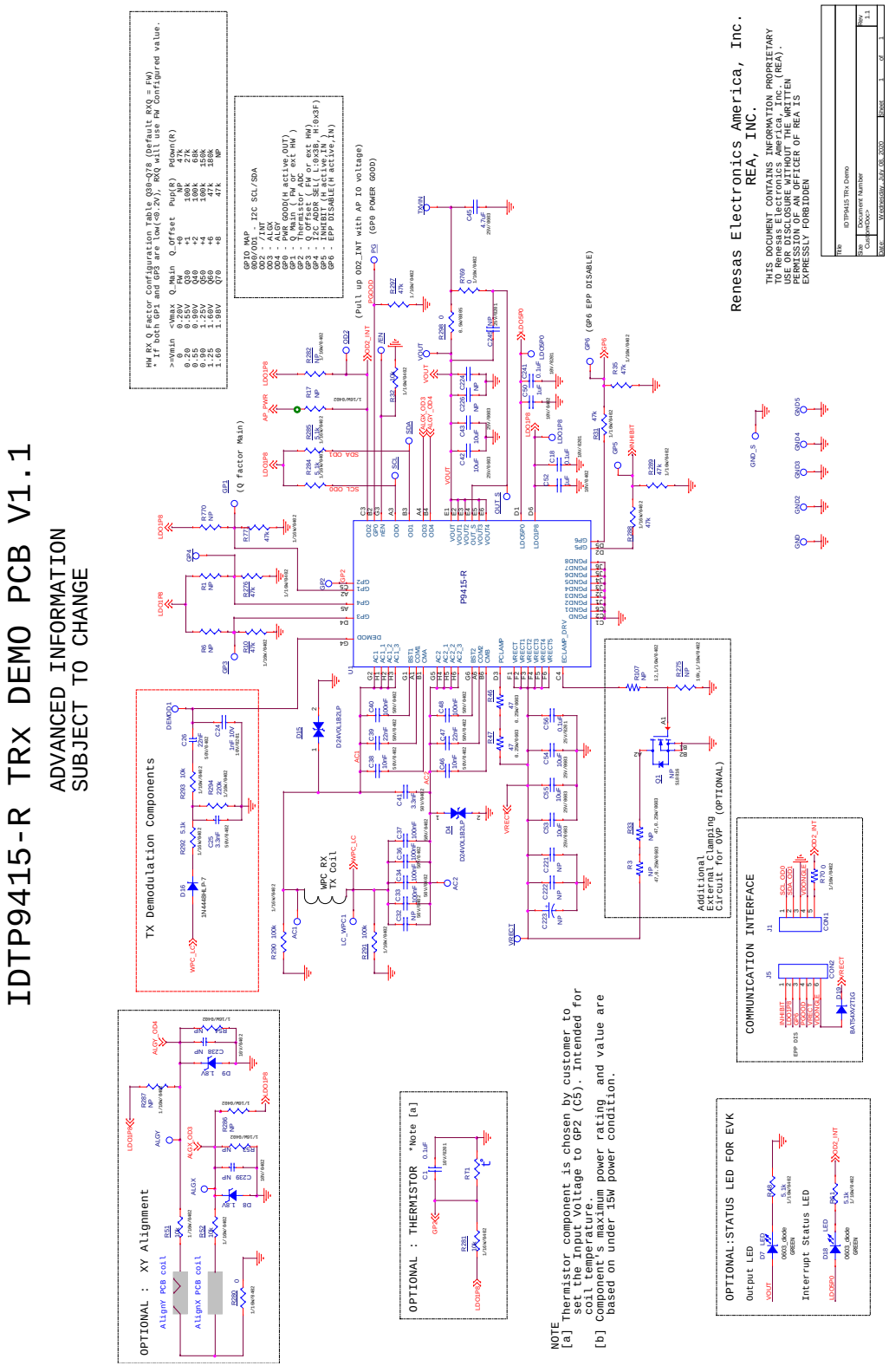
9.12 Multiple-Time Programming Memory

The P9415-R includes MTP or “pseudo-flash” capability with re-programming up to 1000 times. This offers the advantage of re-programming during the pre-production phase to optimize performance and/or re-programming for field upgrades when required. The device contains 24 KB of MTP memory. The MTP programming voltage range is based on the “On-the-Go” (OTG) specification of 5V power (±10%) applied to VRECT via the VOUT pin.

P9415-R Wireless Power Pro GUI software can be used to create a custom design configuration in which users can change the default values of the design parameters such as Rx output voltage value, FOD threshold values.

9.13 Applications Schematics

Figure 26. Typical TRx Applications Schematic



9.14 PCB Layout Considerations

For optimum device performance and lowest output noise, the following guidelines should be observed. Please contact Renesas for Gerber files that contain the recommended board layout.

An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Signal traces not related to the P9415-R should be routed away from the IC as much as possible to avoid blocking thermal dissipation paths from the IC to the PCB. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs because the surface-mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques should be used to remove the heat due to device power dissipation.

The following general guidelines are helpful with designing a board layout for lowest thermal resistance:

1. PC board traces with large cross-sectional areas remove more heat. For optimum results, use large-area PCB patterns with wide copper traces, placed on the P9415-R side of the PCB.
2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
3. Thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

9.15 Special Notes

Package assembly:

- Unopened dry packaged parts have a one-year shelf life.
- The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

10. I2C Function

The P9415-R uses standard I²C slave implementation protocol to communicate with a host Application Processor (AP) or other I2C peripherals. The I2C slave address is decided by GP4 voltage. During the P9451-R power-up, if the GP4 pin is pulled down, the I2C address is 0x3B. During the P9451-R power-up, if the GP4 pin is pulled high, the I2C address is 0x3F.

The AP can write to only the registers that are marked as Read/Write (RW). Registers marked as Read Only (R) should never be sent a Write command. Likewise, register locations marked Reserved should not receive a Write command. When writing to a RW register that contains a combination of RW fields and reserved fields, a read-modify-write should be performed to the intended bit/field only. All other bits, including reserved bits should NOT be modified.

11. List of Registers

Table 10. Chip ID (0x00, 0x01)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x00 [7:0]	Chip_ID_L	R	0x15	Chip ID low byte
0x01 [7:0]	Chip_ID_H	R	0x94	Chip ID high byte

Table 11. HW Revision Register, HW_Rev (0x02)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x02 [7:0]	HW_Rev	R	0x06	Hardware Revision 0x00 (default).

Table 12. Customer Code Register, Customer Code (0x03)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x03 [7:0]	CustomerCode	R	0x00	Customer code. 0x00 (default).

Table 13. Customer ID Register (0x04)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x04 [15:0]	CustomerID	R	0x0000	CustomerID

Table 14. ProjectID Register (0x06)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x06 [15:0]	ProjectID	R	0x0005	Project ID

Table 15. Firmware Revision Major (0x08)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x08 [7:0]	Major	R	0x02	Firmware major revision

Table 16. Firmware Revision Minor (0x09)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x09 [7:0]	Minor	R	0x01	Firmware minor revision

Table 17. Firmware Revision Beta (0x0A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x0a [7:0]	beta	R	0x00	Firmware revision beta

Table 18. Date Register (0x0C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x0c [96:0]	Date	R	-	12-byte string initialized with FW compile data code. The format of the string is: “Mmm DD YYYY”, where Mmm is a three letter Month code, followed by the date in the month and the year. The string is terminated with 0x00.

Table 19. Time Register, (0x18)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x18 [64:0]	Time	R	-	8-byte string initialized with FW compile time code. The format of the string is: “HH:MM:SS”. The string is not zero terminated.

Table 20. Part Number Register (0x20)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x20 [32:0]	Part Number	R	0x52000000	Part number.

Note: The bit definition in Rx mode and Tx mode is different.

Table 21. System Interrupt Clear Register (0x28, 0x29, 0x2A, 0x2B) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2B [7:0]	Reserved	R/W	0	Reserved
0x2A [7]	OVERCURRWARN	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [6]	ADTERROR	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [5]	ADTRCVD	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [4]	ADTSENT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [3]	NTCOVERTEMP	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [2]	VRECTON	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [1:0]	Reserved	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [7]	VSWITCHFAILED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [6]	SLEEPMODE	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [5]	IDAUTHSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [4]	IDAUTHFAILED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [3]	BCSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [2]	BCTIMEOUT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [1]	TXAUTHSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [0]	TXAUTHFAILED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [7]	LDODISABLE	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [6]	LDOENABLE	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [5]	MODECHHGED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [4]	TXDATARCVD	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x28 [3]	VSWITCHSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [2]	OVERTEMP	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [1]	OVERVOLT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [0]	OVERCURR	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.

Note: The bit definition in Rx mode and Tx mode is different.

Table 22. System Interrupt Clear Register (0x28, 0x29, 0x2A, 0x2B) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2B [7:0]	Reserved	R/W	0	Reserved
0x2A [7:0]	Reserved	R/W	0	Reserved
0x29 [7:1]	Reserved	R/W	0	Reserved
0x29 [0]	CSP_RECEIVE_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [7]	TX_INIT_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [6]	GET_DPING_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [5]	MODECHNGED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [4]	GET_CFG_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [3]	GET_ID_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [2]	GET_SS_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [1]	START_DPING_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [0]	EPT_TYPE_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.

Note: The bit definition in Rx mode and Tx mode is different.

Table 23. System Status Register (0x2C, 0x2D, 0x2E, 0x2F) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2F [7:0]	Reserved	R	0	Reserved
0x2E [7]	OVERCURRWARN	R	0	1 = Indicates the Iout is closed to Ilim value
0x2E [6]	ADTERROR	R	0	1 = Indicates error condition happens in the communication channel. Cleared together with the corresponding interrupt flag.
0x2E [5]	ADTRCVD	R	0	1 = Indicates data was received from the Com channel and is pending to be read. Cleared together with the corresponding interrupt flag.
0x2E [4]	ADTSENT	R	0	1 = Indicates data message was processed (sent) in the Com Channel and the WriteBuffer is available to accept new data. Cleared together with the corresponding interrupt flag.
0x2E [3]	NTCOVERTEMP	R	0	1 = Indicates the NTC value exceeds the threshold
0x2E [2]	VRECTON	R	0	Indicates AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. An interrupt event is generated on SET event.
0x2E [1:0]	Reserved	R	0	Reserved
0x2D [7]	VSWITCHFAILED	R	0	1 = Indicates the voltage switch command is failed.
0x2D [6]	SLEEPMODE	R	0	1 = Indicates the Rx is in sleep mode
0x2D [5]	IDAUTHSUCCESS	R	0	1 = Indicates the ID authentication is passed
0x2D [4]	IDAUTHFAILED	R	0	1 = Indicates the ID authentication is failed
0x2D [3]	BCSUCCESS	R	0	1 = Indicates the backchannel packet is received by Tx
0x2D [2]	BCTIMEOUT	R	0	1 = Indicates the backchannel packet is sending failed.
0x2D [1]	TXAUTHSUCCESS	R	0	1 = Indicates the Device authentication is passed.
0x2D [0]	TXAUTHFAILED	R	0	1 = Indicates the Device authentication is failed.
0x2C [7]	LDODISABLE	R	0	1 = Indicates the LDO is disabled
0x2C [6]	LDOENABLE	R	0	1 = Indicates the LDO is enabled
0x2C [5]	MODECHHGED	R	0	1 = Indicates the work mode of P9415 is changed
0x2C [4]	TXDATARCVD	R	0	1 = Indicates the proprietary packet from Tx is received.
0x2C [3]	VSWITCHSUCCESS	R	0	1 = Indicates the voltage switch command is successful.
0x2C [2]	OVERTEMP	R	0	1 = Indicates the die temperature exceeds the OTP threshold.
0x2C [1]	OVERVOLT	R	0	1 = Indicates the voltage on Vrect exceeds the OVP threshold
0x2C [0]	OVERCURR	R	0	1 = Indicates the current exceeds the OCP threshold.

Note: The bit definition in Rx mode and Tx mode is different.

Table 24. System Status Register (0x2C, 0x2D, 0x2E, 0x2F) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2F [7:0]	Reserved	R	0	Reserved
0x2E [7:0]	Reserved	R	0	Reserved
0x2D [7:1]	Reserved	R	0	Reserved
0x2D [0]	CSP_RECEIVE_INT	R	0	1 = Indicates the CSP packet is received. Cleared together with the corresponding interrupt flag
0x2C [7]	TX_INIT_INT	R	0	1 = Indicates the Tx initialization is finished
0x2C [6]	GET_DPING_INT	R	0	1 = Indicates the P9415 works in Tx mode, but is put on another working Tx device.
0x2C [5]	MODECHNGED	R	0	1 = Indicates the work mode of P9415 is changed.
0x2C [4]	GET_CFG_INT	R	0	1 = Indicates the configuration packet is received.
0x2C [3]	GET_ID_INT	R	0	1 = Indicates the Identification packet is received.
0x2C [2]	GET_SS_INT	R	0	1 = Indicates the Signal Strength packet is received.
0x2C [1]	START_DPING_INT	R	0	1 = Indicates the digital ping starts
0x2C [0]	EPT_TYPE_INT	R	0	1 = Indicates the error is met and recommend AP to remove power in this case. AP could read the error type from TRx End Power Transfer Reason Register

Note: The bit definition in Rx mode and Tx mode is different.

Table 25. System Interrupt Register (0x30, 0x31, 0x32, 0x33) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x33 [7:0]	Reserved	R	0	Reserved
0x32 [7]	OVERCURRWARN	R	0	1 = Indicates the Iout is closed to Ilim value 0 = No such condition
0x32 [6]	ADTERROR	R	0	1 = Indicates error condition happens in the communication channel. 0 = No such condition
0x32 [5]	ADTRCVD	R	0	1 = Indicates data was received from the Com channel and is pending to be read. 0 = No such condition
0x32 [4]	ADTSENT	R	0	1 = Indicates data message was processed (sent) in the Com Channel and the WriteBuffer is available to accept new data. 0 = No such condition
0x32 [3]	NTCOVERTEMP	R	0	1 = Indicates the NTC value exceeds the threshold 0 = No such condition
0x32 [2]	VRECTON	R	0	1 = Indicates AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. An interrupt event is generated on SET event. 0 = No such condition

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x32 [1:0]	Reserved	R	0	Reserved
0x31 [7]	VSWITCHFAILED	R	0	1 = Indicates the voltage switch command is failed. 0 = No such condition
0x31 [6]	SLEEPMODE	R	0	1 = Indicates the Rx is in sleep mode 0 = No such condition
0x31 [5]	IDAUTHSUCCESS	R	0	1 = Indicates the ID authentication is passed 0 = No such condition
0x31 [4]	IDAUTHFAILED	R	0	1 = Indicates the ID authentication is failed 0 = No such condition
0x31 [3]	BCSUCCESS	R	0	1 = Indicates the backchannel packet is received by Tx 0 = No such condition
0x31 [2]	BCTIMEOUT	R	0	1 = Indicates the backchannel packet is sending failed. 0 = No such condition
0x31 [1]	TXAUTHSUCCESS	R	0	1 = Indicates the Device authentication is passed. 0 = No such condition
0x31 [0]	TXAUTHFAILED	R	0	1 = Indicates the Device authentication is failed. 0 = No such condition
0x30 [7]	LDODISABLE	R	0	1 = Indicates the LDO is disabled 0 = No such condition
0x30 [6]	LDOENABLE	R	0	1 = Indicates the LDO is enabled 0 = No such condition
0x30 [5]	MODECHHGED	R	0	1 = Indicates the work mode of P9415 is changed 0 = No such condition
0x30 [4]	TXDATARCVD	R	0	1 = Indicates the proprietary packet from Tx is received. 0 = No such condition
0x30 [3]	VSWITCHSUCCESS	R	0	1 = Indicates the voltage switch command is successful. 0 = No such condition
0x30 [2]	OVERTEMP	R	0	1 = Indicates the die temperature exceeds the OTP threshold. 0 = No such condition
0x30 [1]	OVERVOLT	R	0	1 = Indicates the voltage on Vrect exceeds the OVP threshold 0 = No such condition
0x30 [0]	OVERCURR	R	0	1 = Indicates the current exceeds the OCP threshold. 0 = No such condition

Note: The bit definition in Rx mode and Tx mode is different.

Table 26. System Interrupt Register (0x30, 0x31, 0x32, 0x33) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x33 [7:0]	Reserved	R	0	Reserved
0x32 [7:0]	Reserved	R	0	Reserved
0x31 [7:1]	Reserved	R	0	Reserved
0x31 [0]	CSP_RECEIVE_INT	R	0	1 = Indicates the CSP packet is received. 0 = No such condition
0x30 [7]	TX_INIT_INT	R	0	1 = Indicates the Tx initialization is finished 0 = No such condition
0x30 [6]	GET_DPING_INT	R	0	1 = Indicates the P9415 works in Tx mode, but is put on another working Tx device. 0 = No such condition
0x30 [5]	MODECHNGED	R	0	1 = Indicates the work mode of P9415 is changed. 0 = No such condition
0x30 [4]	GET_CFG_INT	R	0	1 = Indicates the configuration packet is received. 0 = No such condition
0x30 [3]	GET_ID_INT	R	0	1 = Indicates the Identification packet is received. 0 = No such condition
0x30 [2]	GET_SS_INT	R	0	1 = Indicates the Signal Strength packet is received. 0 = No such condition
0x30 [1]	START_DPING_INT	R	0	1 = Indicates the digital ping starts 0 = No such condition
0x30 [0]	EPT_TYPE_INT	R	0	1 = Indicates error is met and recommend AP to remove power in this case. 0 = No such condition

Note: The bit definition in Rx mode and Tx mode is different.

Table 27. System Interrupt Enable Register (0x34, 0x35, 0x36, 0x37) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x37 [7:0]	Reserved	R/W	0	Reserved
0x36 [7]	OVERCURRWARN	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [6]	ADTERROR	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [5]	ADTRCVD	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [4]	ADTSENT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [3]	NTCOVERTEMP	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [2]	VRECTON	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [1:0]	Reserved	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [7]	VSWITCHFAILED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [6]	SLEEPMODE	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [5]	IDAUTHSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [4]	IDAUTHFAILED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [3]	BCSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [2]	BCTIMEOUT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [1]	TXAUTHSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [0]	TXAUTHFAILED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [7]	LDODISABLE	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [6]	LDOENABLE	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x34 [5]	MODECHHGED	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [4]	TXDATARCVD	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [3]	VSWITCHSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [2]	OVERTEMP	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [1]	OVERVOLT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [0]	OVERCURR	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Note: The bit definition in Rx mode and Tx mode is different.

Table 28. System Interrupt Enable Register (0x34, 0x35, 0x36, 0x37) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x36 [7:0]	Reserved	R/W	0	Reserved
0x36 [7:0]	Reserved	R/W	0	Reserved
0x35 [7:1]	Reserved	R/W	0	Reserved
0x35 [0]	CSP_RECEIVE_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [7]	TX_INIT_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [6]	GET_DPING_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [5]	MODECHNGED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [4]	GET_CFG_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [3]	GET_ID_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [2]	GET_SS_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [1]	START_DPING_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x34 [0]	EPT_TYPE_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Note: The bit definition in Rx mode and Tx mode is different.

The alignment registers provide information about the positioning of the RX coil relative the TX coil. The AP may use this information to inform the user of possible reduced power transfer level due to receiver misalignment and suggest repositioning of the RX to improve coupling. The magnitude of the alignment information depends on the coil sizes and shall not be used for absolute distance measurement.

Table 29. Alignment X-Axis Register (0x38)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x38 [7:0]	Align[0]	R	-	8-bit signed integer representing X-axis alignment.

Table 30. Alignment Y-Axis Register (0x39)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x39 [7:0]	Align[1]	R	-	8-bit signed integer representing Y-axis alignment.

Table 31. Charge Status Register (0x3A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3a [7:0]	SSChargeStau	RW	0x00	In RX mode the AP writes this register with the value intended to be sent as payload to the Charge Status Packet. The FW does not verify or modify the value in any way. The value should be filled based on the following: 0x0 = Reserved 0x1 = Charge status packet sent with parameter = 1 (1%) 0x2 = Charge status packet send with parameter = 2 (2%) … 0x64 = Charge status packet send with parameter = 100 (100%) 0x65-0xFE = Reserved 0xFF = No battery charge device or not providing charge status packet

Note: After writing to this register, Send Charge Status bit of Command Register (0x4E) needs to be set for transmission to begin.

Table 32. End of Power Transfer Code Register (0x3B)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3b [7:0]	EPTCode	R/W	0x00	In RX mode the AP writes this register with the value intended to be sent as payload to the Charge Status Packet. The FW does not verify or modify the value in any way. A WPC End of Power Transfer packet/message will be sent based on the following: 0 = WPC mode, unknown EPT should be sent. 1 = WPC mode, End of Charge EPT packet should be sent. 2 = WPC mode, Internal Fault EPT packet should be sent. 3 = WPC mode, Over Temperature EPT packet should be sent. 4 = WPC mode, Over Voltage EPT packet should be sent. 5 = WPC mode, Over Current EPT packet should be sent. 6 = WPC mode, Battery Failure EPT packet should be sent. 7 = WPC mode, Reconfiguration EPT packet should be sent. 8 = WPC mode, No Response EPT packet should be sent. 9-254 = Reserved

Table 33. Vout ADC Register (0x3C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3c [15:0]	Vout ADC	R	-	12-bit of current main LDO Vout ADC value. Vout = ADC_Vout Value/4095*10*2.1(V)

Table 34. Vout Set Register (0x3E)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3e [15:0]	Vout_Set	R/W	-	Set the output voltage of the main LDO. VoutSet = (Vout_mV - 2800)*10/84 AP through this register, target Vrect will be automatically set for best efficiency.

Table 35. Vrect ADC (0x40)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x40 [15:0]	Vrect ADC	R	-	12 LSB of current Vrect ADC value. Vrect = ADC_Vrect Value/4095*10*2.1 (V).

Table 36. External Temperature Register ADC (0x42)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x42 [15:12]	Reserved	R	0	Reserved
0x42 [11:0]	NtcTemp	R	-	12-bit raw data of the thermistor ADC reading on GP2 pin. Vol_gp2 = NtcTemp / 4095 * 10 * 2.1(V)

Table 37. IOut Register (0x44)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x44 [15:0]	IOut	R	-	In RX mode the AP may read this register to get current Iout level in mA. In TX mode the register holds the Power Supply current Iin in mA.

Table 38. Die Temperature Register (0x46)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x46 [15:0]	DieTemp	R	-	12bit of current Die Temperature ADC value. Formula converting ADC value to Die Temperature in Celsius Degree is t_die [degC] = (ADC code * 0.075) - 174.

Table 39. AC Period Register (0x48)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x48 [15:0]	ACPeriod	R	-	Read back the AC Period. The value is presented by number of 6MHz clocks per 64 AC cycles. The AC frequency can be calculated as: F(kHz) = 64 * 6000 / ACPeriod;

Table 40. Iout Limit Set Register (0x4A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4a [7:0]	ILim	R	0x0E	Set main LDO current limit in 0.1A steps. The limit level is set to the value plus 0.1A.

Table 41. Signal Strength Packet (0x4B)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4b [7:0]	SignalStrength	R	-	Signal Strength Packet sent by 9415 at beginning of power transfer

Table 42. System Mode Register (0x4D)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4d [7]	BACKPOWERED	R	-	Indication P9415 is powered by Vrect or Vout, but Tx function is not enabled.
0x4d [6:4]	Reserved	R	-	Reserved
0x4d [3]	EXTENDED	R	-	Indicates WPC EPP mode.
0x4d [2]	TXMODE	R	-	Indication of WP Transmitter mode.
0x4d [1]	Reserved	R	-	Reserved
0x4d [0]	WPCMODE	R	-	Indicates the FW is in WP Receiver mode.

Table 43. System Command Register (0x4E)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4F [7]	MPRENEGOTIATE	W	0	AP sets 1 to launch re-negotiation. P9415 clears the bit after processing the command
0x4F [6]	SETIDAUTNOK	W	0	AP sets 1 to set ID authentication pass flag. P9415 clears the bit after processing the command
0x4F [5:2]	Reserved	W	0	Reserved
0x4F [1]	CCACTIVATE	W	0	AP sets 1 to enabled WPC 1.3 communication. P9415 clears the bit after processing the command
0x4F [0]	SOFTRESTART	W	0	AP sets 1 to restart P9415. P9415 clears the bit after processing the command
0x4E [7]	VSWITCH	W	0	AP sets 1 to send Voltage Switch command. P9415 clears the bit after processing the command
0x4E [6]	Reserved	W	0	Reserved
0x4E [5]	CLRINT	W	0	AP sets 1 to clear the interrupt. P9415 clears the bit after processing the command
0x4E [4]	SENDCSP	W	0	AP sets 1 to send Charge Status Packet in Rx mode. P9415 clears the bit after processing the command
0x4E [3]	SENDEOP	W	0	AP sets 1 to send End of Power Transfer Packet in Rx mode. P9415 clears the bit after processing the command
0x4E [2]	SHA1AUTH	W	0	AP sets 1 to enable device authentication. P9415 clears the bit after processing the command
0x4E [1]	LDOTGL	W	0	AP sets 1 to toggle LDO ON/OFF. P9415 clears the bit after processing the command
0x4E [0]	SENDPROPP	W	0	AP sets 1 to enable send the proprietary packet. P9415 clears the bit after processing the command

Note: It takes time to implement the command. AP could write new command to System Command Register 3~5ms after the previous command.

Table 44. Foreign Object Detection Registers (FOD) (0x68-0x77)

The FOD registers are divided into eight pairs. Each pair has one byte for gain setting and one byte for offset setting. The first six pairs control the Received Power calculation for six power sectors during the Power Transfer phase. The seventh pair calibrates the internal DC Load. The set values of the FOD registers are found with the help of a Renesas developed calibration procedure using the nok9 tester.

The firmware initializes the FOD registers for BPP mode. The correct set is loaded at the completion of the ID and Configuration Phase. The AP can modify the registers at any time if needed to update the values.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x68 [7:0]	GAIN_0	R/W	-	FOD coefficients for Power Region 0: Gain (slope settings).
0x69 [7:0]	OFFSET_0	R/W	-	FOD coefficients for Power Region 0: Offset settings.
0x6A [7:0]	GAIN_1	R/W	-	FOD coefficients for Power Region 1: Gain (slope settings).
0x6B [7:0]	OFFSET_1	R/W	-	FOD coefficients for Power Region 1: Offset settings.
0x6C [7:0]	GAIN_2	R/W	-	FOD coefficients for Power Region 2: Gain (slope settings).
0x6D [7:0]	OFFSET_2	R/W	-	FOD coefficients for Power Region 2: Offset settings.
0x6E [7:0]	GAIN_3	R/W	-	FOD coefficients for Power Region 3: Gain (slope settings).
0x6F [7:0]	OFFSET_3	R/W	-	FOD coefficients for Power Region 3: Offset settings.
0x70 [7:0]	GAIN_4	R/W	-	FOD coefficients for Power Region 4: Gain (slope settings).
0x71 [7:0]	OFFSET_4	R/W	-	FOD coefficients for Power Region 4: Offset settings.
0x72 [7:0]	GAIN_5	R/W	-	FOD coefficients for Power Region 5: Gain (slope settings).
0x73 [7:0]	OFFSET_5	R/W	-	FOD coefficients for Power Region 5: Offset settings.
0x74 [7:0]	GAIN_6	R/W	-	FOD coefficients for Power Region 6: Gain (slope settings).
0x75 [7:0]	OFFSET_6	R/W	-	FOD coefficients for Power Region 6: Offset settings.
0x76 [7:0]	GAIN_7	R/W	-	FOD coefficients for Power Region 7: Gain (slope settings).
0x77[7:0]	OFFSET_7	R/W	-	FOD coefficients for Power Region 7: Offset settings.

Table 45. Vin Register in Tx Mode (0x70)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x70 [15:0]	TxVin	R	-	Input voltage, value in mV.

Table 46. Vrect Register in Tx Mode (0x72)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x72 [15:0]	TxVrect	R	-	Vrect voltage in Tx mode, value in mV.

Table 47. End Power Transfer Reason Register (0x74)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x75 [7]	EPT_POCP	R	0	1 = Indicates over current protect during digital ping 0 = No such error
0x75 [6]	EPT_OTP	R	0	1 = Over current error 0 = No such error
0x75 [5]	EPT_FOD	R	0	1 = FOD error 0 = No such error
0x75 [4]	EPT_LVP	R	0	1 = Vrect is less than low voltage protection threshold 0 = No such error
0x75 [3]	EPT_OVP	R	0	1 = Over voltage error 0 = No such error
0x75 [2]	EPT_OCP	R	0	1 = Over current error 0 = No such error
0x75 [1]	Reserved	R	0	Reserved
0x75 [0]	EPT_CEP_TIMEOUT	R	0	1 = CEP timeout 0 = No such error
0x74 [7]	EPT_TIMEOUT	R	0	1 = Watch dog timeout 0 = No such error
0x74 [6:1]	Reserved	R	0	Reserved
0x74 [0]	EPT_CMD	R	0	1 = End power transfer packet has been received 0 = No such error

Table 48. System Command Register (0x76)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x77 [7:0]	Reserved	W	0	Reserved.
0x76 [7]	Reserved	W	0	Reserved.
0x76 [6]	CTCMND	W	0	AP sets 1 to set CT command. The P9415 will read CT command from CT Command register and implement. P9415 clears the bit after processing the command.
0x76 [5]	TX_CLRINT	W	0	AP sets 1 to clear interrupt. P9415 clears the bit after processing the command.
0x76 [4]	Reserved	W	0	Reserved
0x76 [3]	TX_BC	W	0	AP sets 1 to send a proprietary packet to Rx. P9415 clears the bit after processing the command
0x76 [2]	TX_DIS	W	0	AP sets 1 to disable Tx mode. P9415 clears the bit after processing the command.
0x76 [1]	Reserved	W	0	Reserved
0x76 [0]	TX_EN	W	0	AP sets 1 to enable Tx mode. P9415 clears the bit after processing the command

Note: It costs time to implement the command. AP could write new command to System Command Register 3~5ms after the previous command.

Table 49. Over Voltage Threshold Register in Tx Mode (0x98)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x98 [15:0]	OVpThd	R/W	0x2AF8	Over-voltage threshold in Tx mode, value in mV.

Table 50. Over Current Threshold Register in Tx Mode (0x9A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x9A [15:0]	OCpThd	R/W	0x05DC	Over-current threshold in Tx mode, value in mA.

Table 51. FOD Low Segment Threshold Register in Tx Mode (0xA8)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xA8 [15:0]	FodThdL	R/W	0x0320	FOD threshold for low level segment in Tx mode, value in mW.

Table 52. FOD High Segment Threshold Register in Tx Mode (0xAA)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xAA [15:0]	fodThdH	R/W	0xFF9C	FOD threshold for high level segment in Tx mode, value in mW.

Table 53. FOD Segment Threshold Register in Tx Mode (0xAC)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xAC [15:0]	fodSegThd	R/W	0x0E74	Threshold for two segment FOD threshold. Value in mW. If Rx Power is higher than FOD Segment Threshold, the High Level FOD Threshold is used, otherwise, the Low Level FOD Threshold is used as FOD threshold.

Table 54. Ping Interval Register in Tx Mode (0xBA)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xBA [15:0]	PingInterval	R/W	0x038E	The interval between each digital ping, value in ms.

11.1 Bi-di Communication Registers

Table 55. Write Data Type and Length Register for WPC 1.3 (0x1A0)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x1A1[7]	WrLsSize	R/W	0	7 LSB of packet size
0x1A0[7:5]	WrMsSize	R/W	0	3 MSB of packet size
0x1A0 [4:0]	WrType	R/W	0	Type of packet

Table 56. Write Data Register for WPC 1.3 (0x1A4~0x39F)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x1A4[508]	WrData	R/W	0	Raw data which is intended to send to Tx

Table 57. Read Data Register for WPC 1.3 (0x3A4~0x59F)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3A4[508]	RdData	R	0	Raw data which is received from Tx

Table 58. Read Data Register for WPC 1.3 (0x196)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x196[15:0]	ccRdSize	R	0	Length of the raw data received from Tx

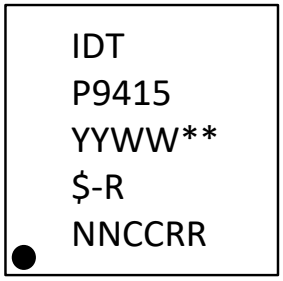
Procedure of WPC1.3 bi-di communication

1. Clear interrupt.
2. AP writes raw data to Write Data Register (0x1A4).
3. AP writes type and data length to Write Data Type and Length Register (0x1A0, 2 bytes).
4. AP writes command 0x02 to system command register (0x4F, 1 byte) to send the data out.
5. AP waits for interrupt (ADTRCVD).
6. AP reads received data length from Read Data Register (0x196, 2 bytes).
7. AP reads received data from Read Data Register (0x3A4).

12. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

13. Marking Diagram



Line 1. is the manufacturer.
Line 2. is the truncated part number.
Line 3. "YYWW" is the last 2 digits of the year and week that the part was assembled.
"**" denotes sequential lot number.
Line 4. "$" denotes assembly mark code. " "R" is part of the device part number.
Line 5. "NN" is the wafer number; "CC" is the column or X- coordinate of the wafer; "RR" is the row or Y-coordinate of the wafer.

14. Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Ambient Temperature	Firmware[a]
P9415-RAWQI8	AWQ53 WLCSP-53 2.82 × 4.22 × 0.50 mm with 0.4mm pitch	MSL 1	Tape and Reel	-40° to +85°C	Blank

15. Revision History

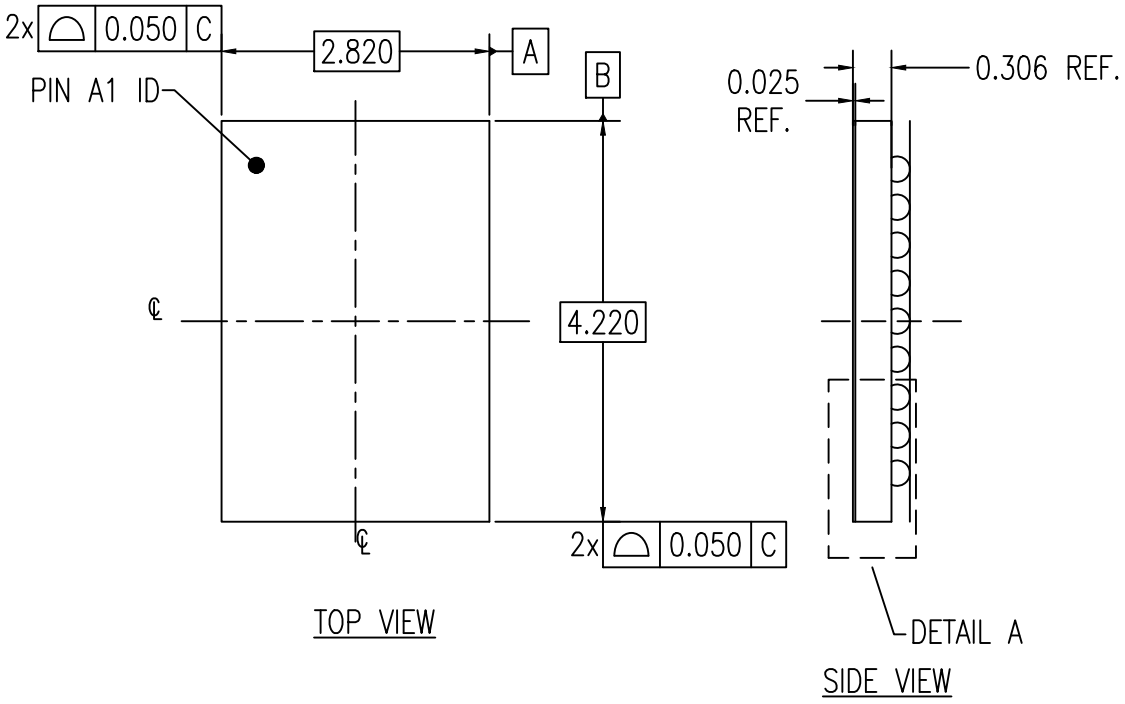
Revision Date	Description of Change
May 4, 2021	Updated "GP1/Q Main Pin and GP3/Q Offset Pin"
September 4, 2020	Updated the V_{MLDO} specifications in Table 4 Updated the address and bit field in Table 30
September 1, 2020	Initial release.

53-DSBGA, Package Outline Drawing

2.820 x 4.220 x 0.500 mm Body, 0.40mm Pitch

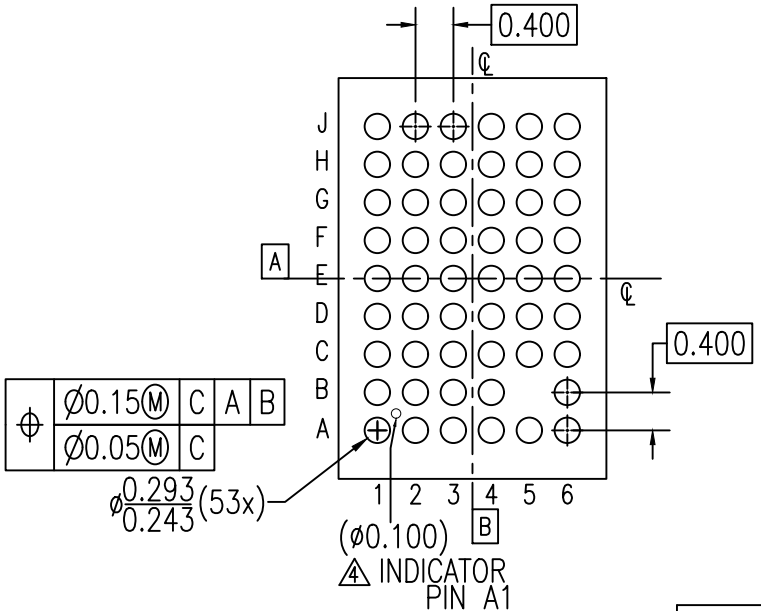
AWQ53D1, PSC-4798-01, Rev 01, Page 1

NOTES:
1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SEATING PLANE AND PRIMARY DATUM –C– ARE DEFINED BY THE CONTACT POINTS OF THREE OR MORE SOLDER BALLS THAT SUPPORT THE DEVICE WHEN PLACED ON A TOP OF A PLANAR SURFACE.
4. BOTTOM PIN#1 INDICATOR OPTIONAL.
5. BALL SIZE BEFORE REFLOW IS 0.25MM.
6. WAFER SCRIBE LINE WIDTH 90UM; KERF WIDTH 40UM.

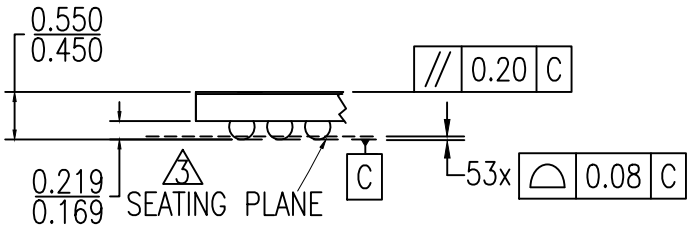


TOP VIEW

SIDE VIEW

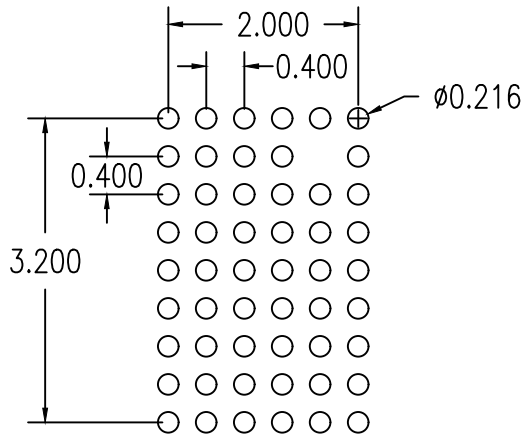


BOTTOM VIEW



DETAIL A
(ROTATED 90 DEG CW)

Package Revision History		
Date Created	Rev No.	Description
April 1, 2019	Rev 00	Initial Release



RECOMMENDED LAND PATTERN DIMENSION

NOTE:
1. ALL DIMENSIONS ARE IN MM, ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEW ON PCB.
3. NSMD LAND PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION AS PER IDT DSBGA APPLICATION NOTE.

	Package Revision History	
Date Created	Rev No.	Description
May 6, 2019	Rev 01.	Change Package Code from AZQ53 To AWQ53
April 1, 2019	Rev 00	Initial Release

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