OPAx863A High-Precision, 105-MHz, Rail-to-Rail Input/Output Amplifiers

1 Features

- Gain-bandwidth product: 50-MHz
- High precision
  - Input offset voltage: 95-µV (maximum)
  - Offset drift: 1.2-µV/°C (maximum)
- Low power
  - Quiescent current: 800-µA/ch (typical)
  - Supply voltage: 2.7-V to 12.6-V
- Input voltage noise: 6.3-nV/√Hz
- Slew rate: 100-V/µs
- Rail-to-rail input and output
- HD_2/HD_3: –129 dBc/–138 dBc at 20 kHz (2-V_{PP})
- Operating temperature range: –40°C to +125°C
- Additional features:
  - Overload power limit
  - Output short-circuit protection

2 Applications

- Low-power SAR and ΔΣ ADC driver
- ADC reference buffer
- Low-side current sensing
- Photodiode TIA interface
- Inductive sensing
- Battery-powered instrumentation
- Gain and active filter stages

3 Description

The OPA863A and OPA2863A devices (OPAx863A) are low-power, unity-gain stable, rail-to-rail input and output, voltage-feedback operational amplifiers. These devices are trimmed in package to offer high-precision performance with a maximum input offset voltage of 95 µV and offset drift of 1.2 µV/°C for high accuracy measurements over temperature.

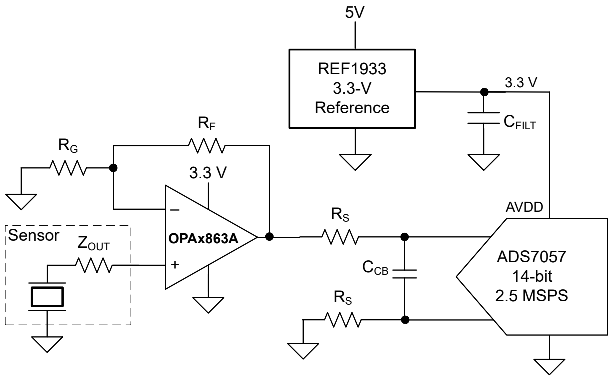
Consuming only 800 µA per channel, the OPAx863A offer a gain-bandwidth product of 50 MHz, slew rate of 100 V/µs, and a voltage noise density of 6.3 nV/√Hz. The rail-to-rail input stage with 2.7-V supply operation is useful in portable, battery-powered applications. The rail-to-rail input stage is well matched for gain-bandwidth product and noise across the full input common-mode voltage range, enabling excellent performance with wide-input dynamic range.

The OPAx863A include overload power limiting to limit the increase in I_Q with saturated outputs, thereby preventing excessive power dissipation in power-conscious, battery-operated systems. The output stage is short-circuit protected, making these devices conducive to ruggedized environments.

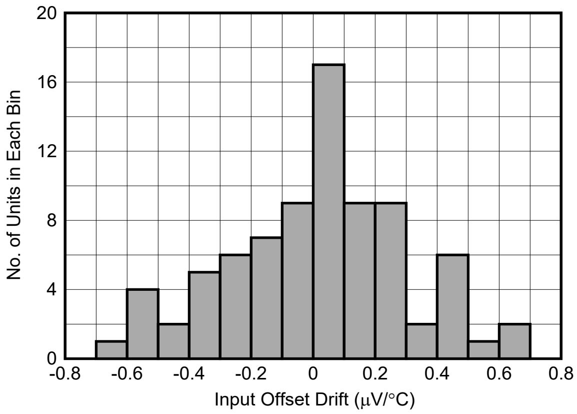
Package Information[(1)(2)]

PART NUMBER	CHANNEL COUNT	PACKAGE
OPA863A	Single	DBV (SOT-23, 5)[(3)]
OPA2863A	Dual	DSN (USON, 10)

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) For related products, see the *Device Comparison Table*.
(3) Preview information (not Production Data).



OPAx863A as a Precision SAR ADC Input Driver



Precision Performance With Low Input-Offset-Voltage Drift

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2022) to Revision C (August 2023) — Page

- Changed OPA863A DBV (SOT-23, 5) package status from preview to advanced information (preview with samples)...... 1
- Added correct Y-axis label to Figure 7-2, *Small-Signal Frequency Response vs Output Load* 11

Changes from Revision A (December 2022) to Revision B (December 2022) — Page

- Changed the description for the $\overline{\text{PD1}}$ and $\overline{\text{PD2}}$ pins from: *high/floating = enabled* to: *high = enabled* 3

Changes from Revision * (May 2022) to Revision A (December 2022) — Page

- Changed the status of the data sheet from: *Advanced Information* to: *Production Data* 1

5 Device Comparison Table

DEVICE	±V_S (V)	I_Q/CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPAx863A	±6.3	0.80	50	100	6.3	Unity-gain stable RRIO bipolar amplifier
LMH6643	±6.4	2.7	65	130	17	Unity-gain stable NRI/RRO bipolar amplifier
OPA810	±13.5	3.6	70	200	6.3	Unity-gain stable RRIO FET-input amplifier
OPA837	±2.7	0.6	50	105	4.7	Unity-gain stable NRI/RRO bipolar amplifier
OPA607	±2.75	0.9	50	24	3.8	Decompensated gain of 6 V/V stable CMOS amplifier

6 Pin Configuration and Functions

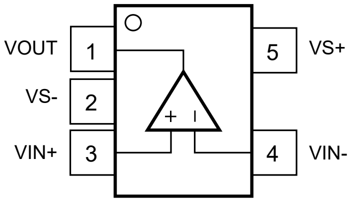


Figure 6-1. OPA863A DBV Package (Preview), 5-Pin SOT-23 (Top View)

Table 6-1. Pin Functions: OPA863A

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{PD}$	—	I	Power down. Low = disabled, high = enabled
VIN+	3	I	Noninverting input pin
VIN–	4	I	Inverting input pin
VOUT	1	O	Output pin
VS–	2	P	Negative power-supply pin
VS+	5	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

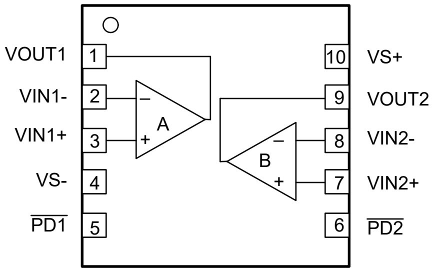


Figure 6-2. OPA2863A DSN Package, 10-Pin USON With Exposed Thermal Pad (Top View)

Table 6-2. Pin Functions: OPA2863A

PIN		TYPE[1]	DESCRIPTION
NAME	**NO.**		
$\overline{\text{PD1}}$	5	I	Amplifier 1 power down. Low = disabled, high = enabled
$\overline{\text{PD2}}$	6	I	Amplifier 2 power down. Low = disabled, high = enabled
VIN1–	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VIN2–	8	I	Amplifier 2 inverting input pin
VIN2+	7	I	Amplifier 2 noninverting input pin
VOUT1	1	O	Amplifier 1 output pin
VOUT2	9	O	Amplifier 2 output pin
VS–	4	P	Negative power-supply pin
VS+	10	P	Positive power-supply pin
Thermal Pad		—	Thermal pad. Electrically isolated from the device. Recommended connection to a heat spreading plane, typically GND.

(1) I = input, O = output, and P = power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		13	V
	Supply turn-on/off maximum dV/dt		1	V/µs
V_I	Input voltage	V_{S-} – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Continuous input current limit for both the ESD diodes to the supply pins and amplifier differential input clamp diode. The differential input clamp diodes limit the voltage between the two inputs to 1 V with this continuous input current flowing through these diodes.

(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S-} to V_{S+}	Total supply voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information: OPA863A

THERMAL METRIC[1]		OPA863A DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2863A

THERMAL METRIC[1]		OPA2863A DSN (USON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	25.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics: V_S = ±5 V

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		105		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		14		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		15		MHz
SR	Slew rate	V_{OUT} = 2-V step		100		V/µs
	Rise, fall time	V_{OUT} = 200-mV step		9		ns
	Settling time	To 0.1%, V_{OUT} = 2-V step		50		ns
		To 0.01%, V_{OUT} = 2-V step		70		
	Overshoot/undershoot	V_{OUT} = 2-V step		1		%
	Overdrive recovery time	G = –1, 0.5-V overdrive beyond supplies		70		ns
		G = 1, 0.5-V overdrive beyond supplies		90		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–129		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–138		dBc
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–107		dBc
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–125		dBc
e_N	Input voltage noise			6.3		nV/√Hz
i_N	Input current noise			0.5		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 2 V_{PP}		–120		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±2.5 V	110	128		dB
V_{OS}	Input-referred offset voltage		–95	±10	95	µV
	Input offset voltage drift	T_A = –40°C to +125°C	–1.2	±0.3	1.2	µV/°C
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3		nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage		V_{S-}–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = V_{S-} – 0.2 V to V_{S+} – 1.6 V	95	120		dB
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		V_{S-}+0.14	V_{S-}+0.2	V
		T_A = –40°C to +125°C		V_{S-}+0.15	V_{S-}+0.22	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.2	V_{S+}–0.14		V
		T_A = –40°C to +125°C	V_{S+}–0.2	V_{S+}–0.15		
	Linear output drive (sourcing/sinking)	V_{OUT} = ±2.5 V, ΔV_{OS} < 1 mV(1)	23	30		mA
	Short-circuit current			45		mA

7.6 Electrical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≈ 25°C		800	925	µA
		T_A = –40°C to +125°C			1040	
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V[2]	100	120		dB
POWER DOWN						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			4.5	V
	Disable voltage threshold	Specified *off* below V_{S+}–1.5 V	3.5			V
	Power-down quiescent current per channel	$V_{\overline{PD}} \le V_{S+}$ – 1.5 V		11	28	µA
		$V_{\overline{PD}} \le V_{S+}$ – 1.5 V, T_A = –40°C to +125°C			35	
	Power-down pin bias current			1	2.5	µA
	Turn-on time delay			8		µs
	Turn-off time delay			3.5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise			6.3		nV/√Hz
	Input current noise			0.5		pA/√Hz
	Input-referred offset voltage		–95	±10	95	µV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.2	1.3	
	Common-mode rejection ratio	V_{CM} = 4.1 V to 5.2 V		120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V		120		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

7.7 Electrical Characteristics: V_S = 3 V

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		85		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		23		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		10		MHz
SR	Slew rate	V_{OUT} = 1-V step		53		V/µs
	Rise, fall time	V_{OUT} = 200-mV step		10		ns
	Settling time	To 0.1%, V_{OUT} = 1-V step		58		ns
		To 0.01%, V_{OUT} = 1-V step		90		
	Overshoot	V_{OUT} = 1-V step		2		%
	Undershoot	V_{OUT} = 1-V step		16		%
	Overdrive recovery time	G = –1, 0.5-V overdrive beyond supplies		85		ns
		G = 1, 0.5-V overdrive beyond supplies		130		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–123		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–132		dBc
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–109		dBc
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–129		dBc
e_N	Input voltage noise			6.3		nV/√Hz
i_N	Input current noise			0.5		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 1 V_{PP}		–120		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = 1 V to 2 V	104	123		dB
V_{OS}	Input-referred offset voltage		–95	±10	95	µV
	Input offset voltage drift	T_A = –40°C to +125°C	–1.2	±0.3	1.2	µV/°C
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.56	
	Input bias current drift	T_A = –40°C to +125°C		±3		nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	92	115		dB
	Input impedance common-mode			360 || 0.9		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		$V_{S–}$ + 0.13	$V_{S–}$ + 0.15	V
		T_A = –40°C to +125°C		$V_{S–}$ + 0.13	$V_{S–}$ + 0.16	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.15	V_{S+}–0.13		V
		T_A = –40°C to +125°C	V_{S+}–0.15	V_{S+}–0.13		
	Linear output drive (sourcing and sinking)	V_{OUT} = ±0.7 V, ΔV_{OS} < 1 mV(1)	23	33		mA
	Short-circuit current			45		mA

7.7 Electrical Characteristics: V_S = 3 V (continued)

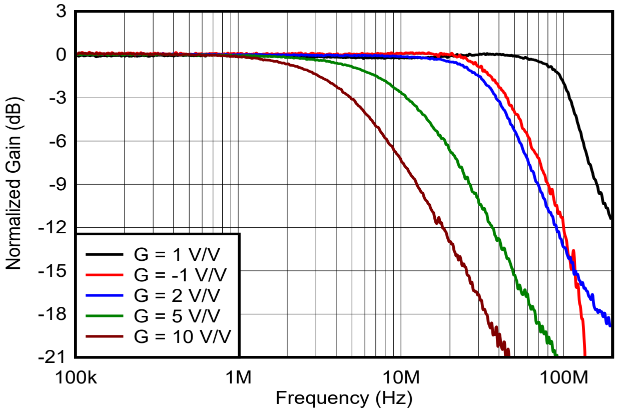
at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≈ 25°C		770	890	µA
		T_A = –40°C to +125°C			995	
PSRR	Power-supply rejection ratio	ΔV_S = ±1 V(2)	100	120		dB
POWER DOWN						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			2.5	V
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	1.5			V
	Power-down quiescent current per channel	$V_{\overline{PD}} \leq V_{S+}$ – 1.5 V		8.5	20	µA
		$V_{\overline{PD}} \leq V_{S+}$ – 1.5 V, T_A = –40°C to +125°C			30	
	Power-down pin bias current			1	2.5	µA
	Turn-on time delay			8		µs
	Turn-off time delay			3.5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise			6.3		nV/√Hz
	Input current noise			0.5		pA/√Hz
	Input-referred offset voltage		–95	±10	95	µV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.4	1.2	
	Common-mode rejection ratio	V_{CM} = 2.1 V to 3.2 V		115		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V		115		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

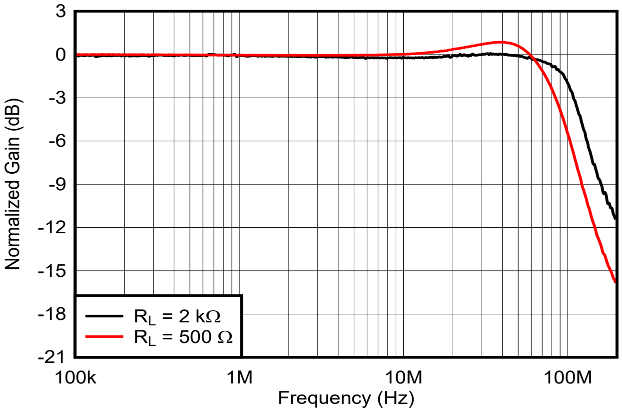
7.8 Typical Characteristics: $V_S = \pm5$ V

at $V_{S+} = 5$ V, $V_{S-} = -5$ V, $R_F = 0\ \Omega$ for G = 1 V/V; otherwise, $R_F = 1\ k\Omega$ for other gains, $C_L = 1$ pF, $R_L = 2\ k\Omega$ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and $T_A \cong 25°C$ (unless otherwise noted)



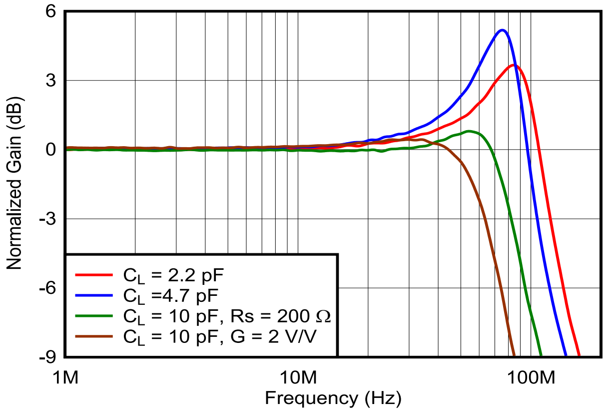
$V_{OUT} = 20\ mV_{PP}$

Figure 7-1. Small-Signal Frequency Response vs Gain



$V_{OUT} = 20\ mV_{PP}$

Figure 7-2. Small-Signal Frequency Response vs Output Load



$V_{OUT} = 20\ mV_{PP}$

Figure 7-3. Frequency Response vs Load Capacitance

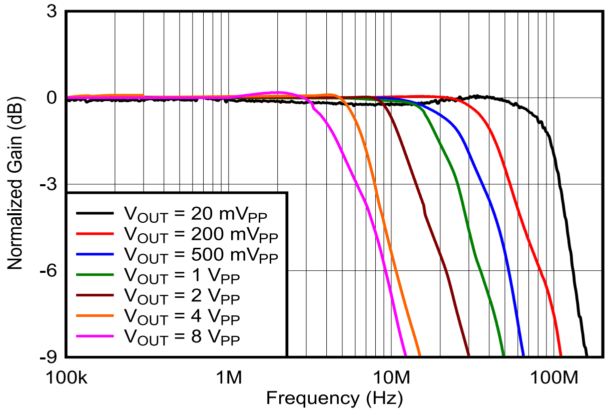
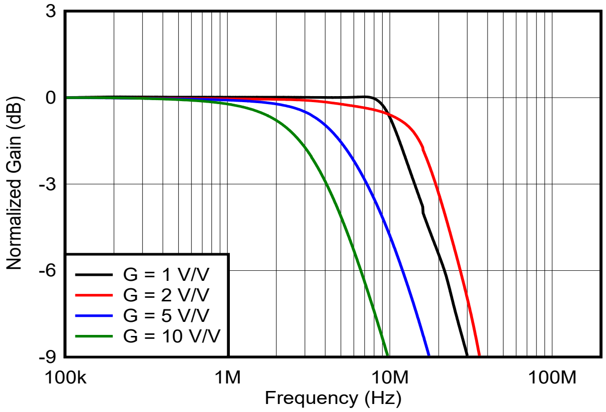
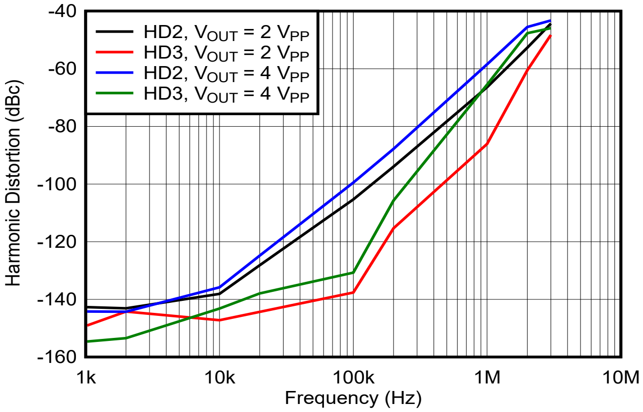


Figure 7-4. Frequency Response vs Output Voltage



$V_{OUT} = 2\ V_{PP}$

Figure 7-5. Large-Signal Frequency Response vs Gain

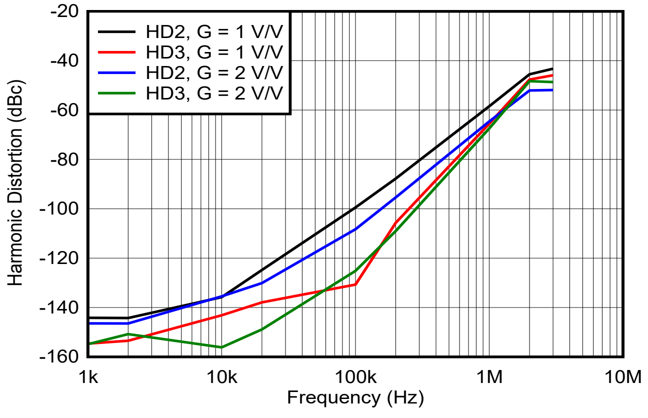


G = 1 V/V

Figure 7-6. Harmonic Distortion vs Frequency

7.8 Typical Characteristics: V_S = ±5 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for G = 1 V/V; otherwise, R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 4 V_{PP}

Figure 7-7. Harmonic Distortion vs Gain

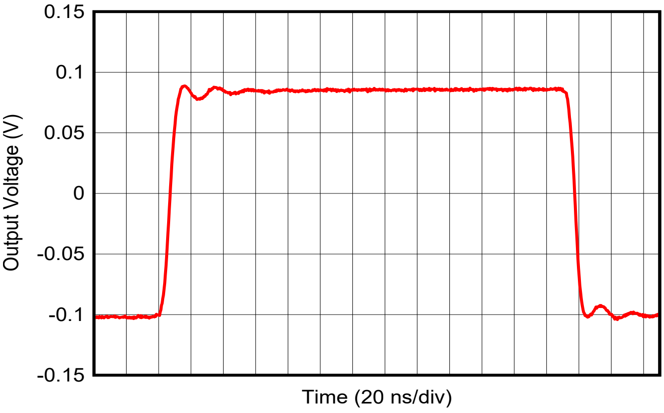


Figure 7-8. Small-Signal Transient Response

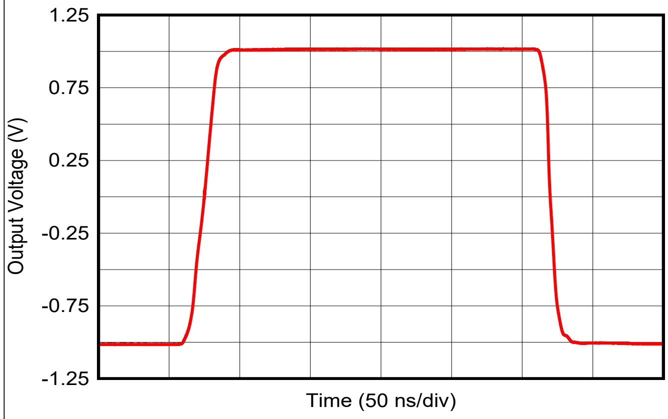
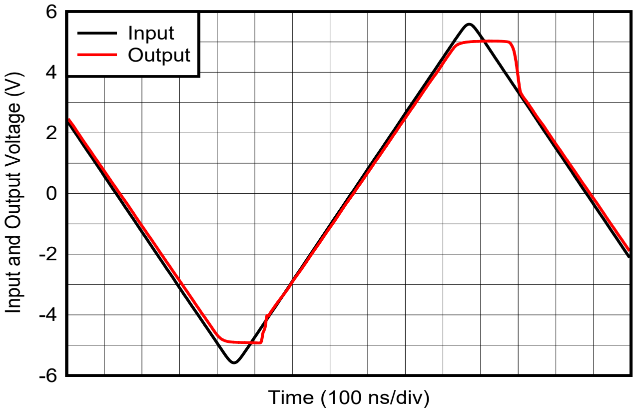
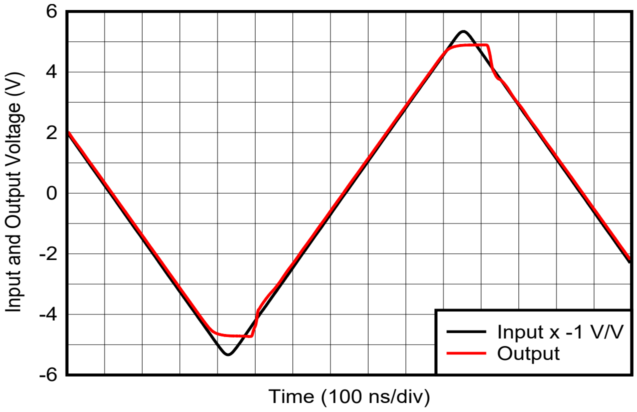


Figure 7-9. Large-Signal Transient Response



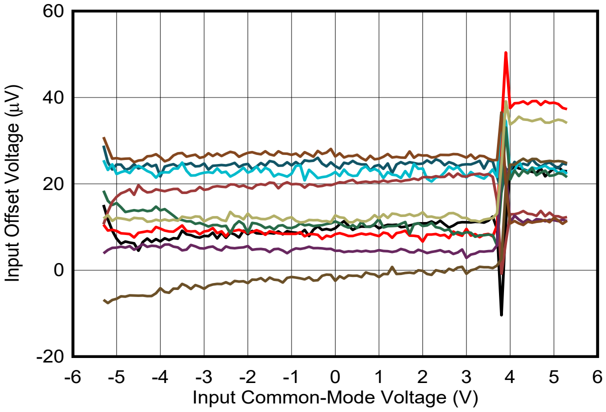
G = 1 V/V

Figure 7-10. Input Overdrive Recovery



G = –1 V/V

Figure 7-11. Output Overdrive Recovery



Measured for 10 units

Figure 7-12. Input Offset Voltage vs Input Common-Mode Voltage

7.8 Typical Characteristics: V_S = ±5 V (continued)

at V_{S+} = 5 V, V_{S-} = –5 V, R_F = 0 Ω for G = 1 V/V; otherwise, R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

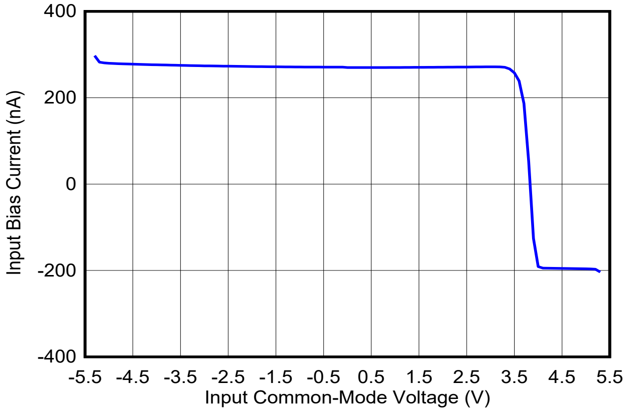


Figure 7-13. Input Bias Current vs Input Common-Mode Voltage

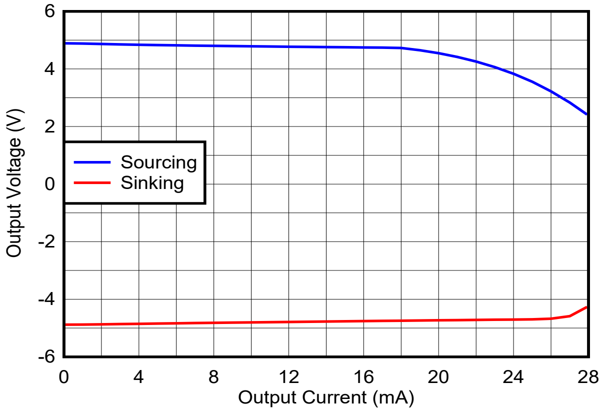
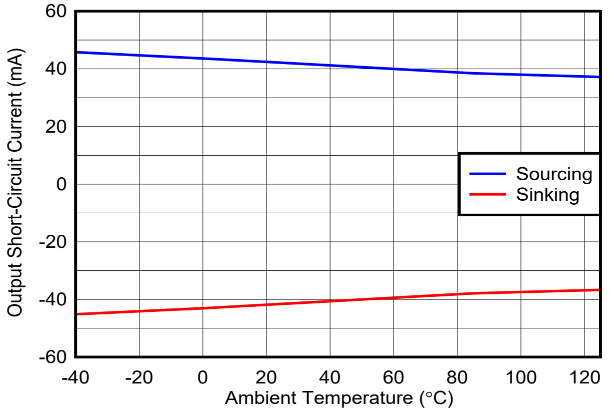
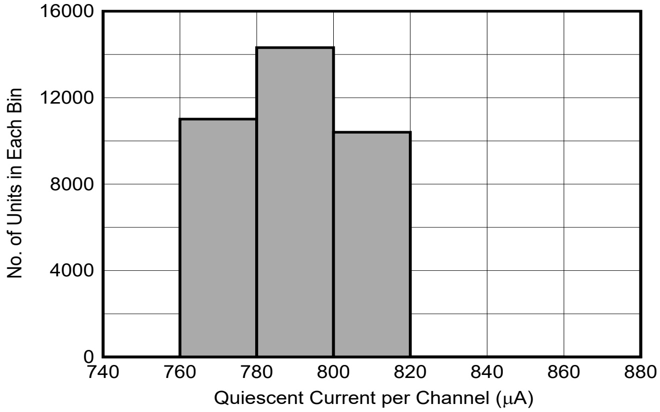


Figure 7-14. Output Voltage vs Load Current



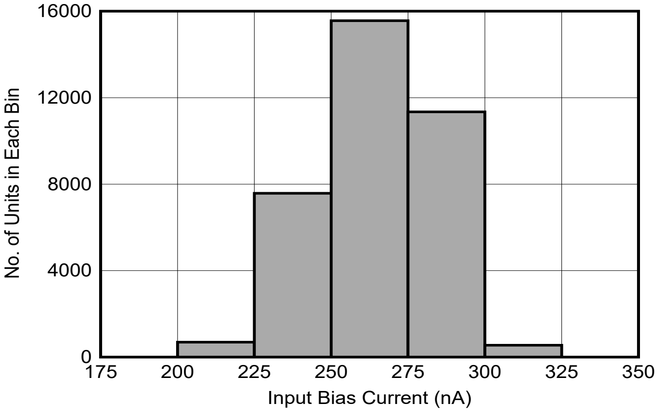
Output saturated and then short-circuited to opposite supply

Figure 7-15. Output Short-Circuit Current vs Ambient Temperature



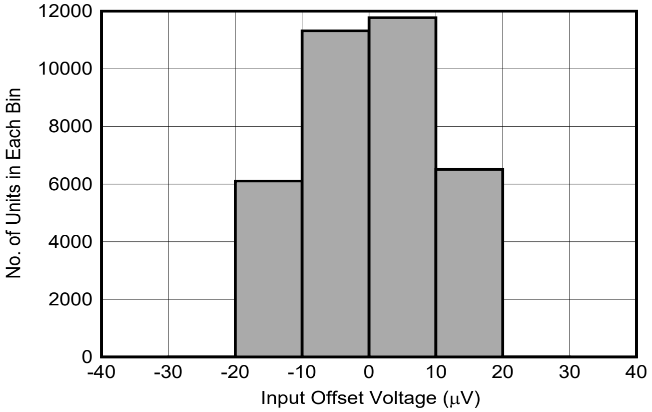
μ = 790 μA, σ = 13.8 μA

Figure 7-16. Quiescent Current Distribution



μ = 265 nA, σ = 18.6 nA

Figure 7-17. Input Bias Current Distribution

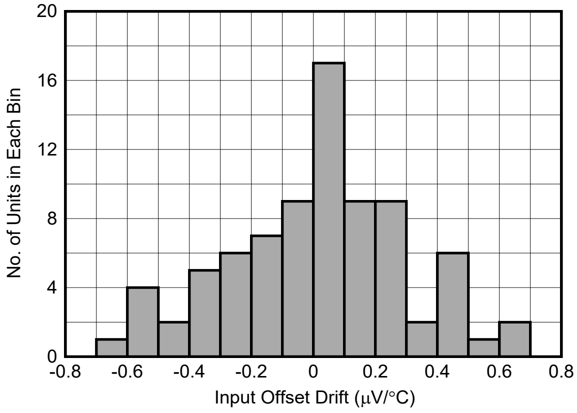


μ = 0.1 μV, σ = 9.1 μV

Figure 7-18. Input Offset Voltage Distribution

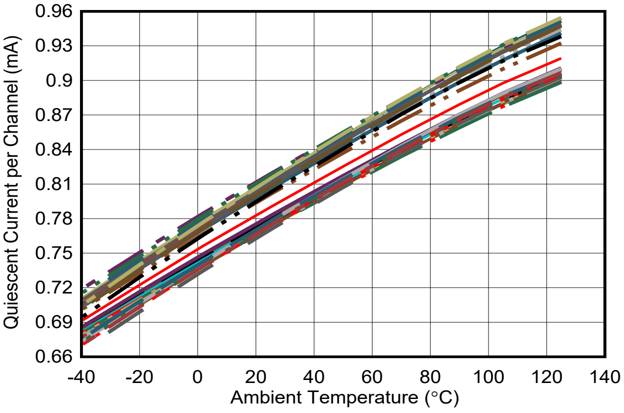
7.8 Typical Characteristics: V_S = ±5 V (continued)

at V_{S+} = 5 V, V_{S-} = –5 V, R_F = 0 Ω for G = 1 V/V; otherwise, R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



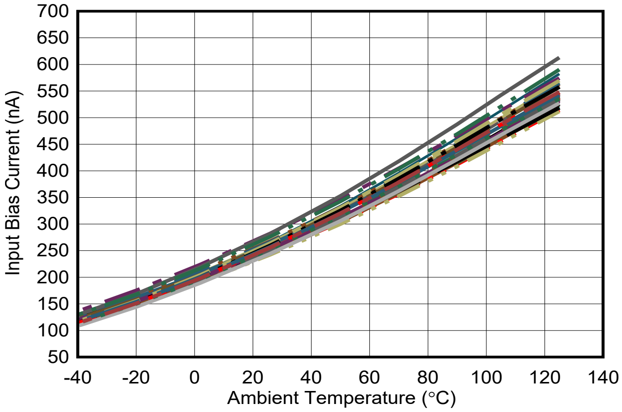
80 units, µ = 0.01 µV/°C, σ = 0.29 µV/°C, DSN package

Figure 7-19. Input Offset Voltage Drift Distribution



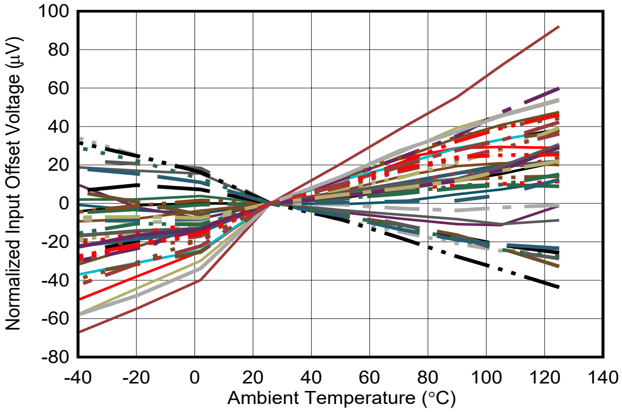
35 units

Figure 7-20. Quiescent Current vs Ambient Temperature



35 units

Figure 7-21. Input Bias Current vs Ambient Temperature



Normalized to 25°C values, 35 units, DSN package

Figure 7-22. Input Offset Voltage vs Ambient Temperature

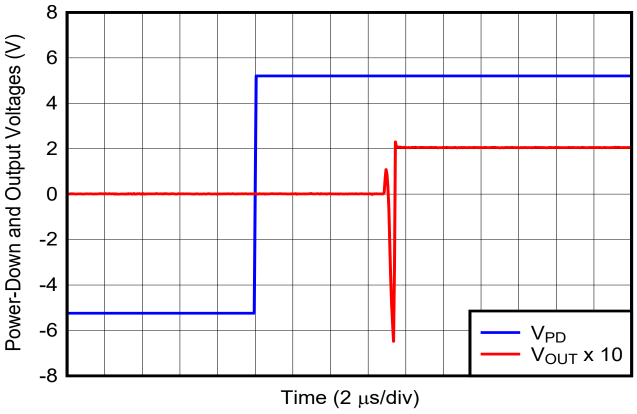


Figure 7-23. Turn-On Time to DC Input

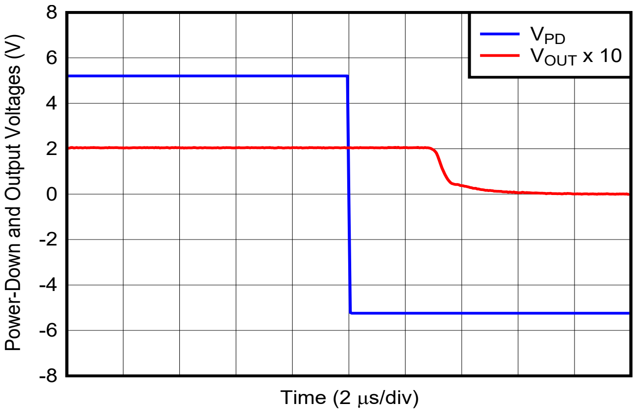
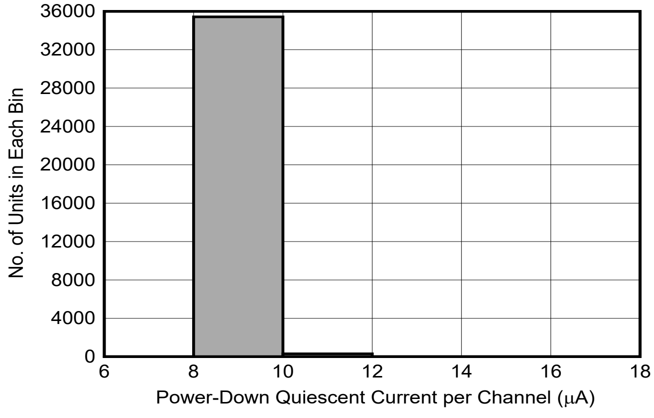


Figure 7-24. Turn-Off Time to DC Input

7.8 Typical Characteristics: V_S = ±5 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for G = 1 V/V; otherwise, R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



μ = 9.3 μA, σ = 0.32 μA

Figure 7-25. Power-Down Quiescent Current Distribution

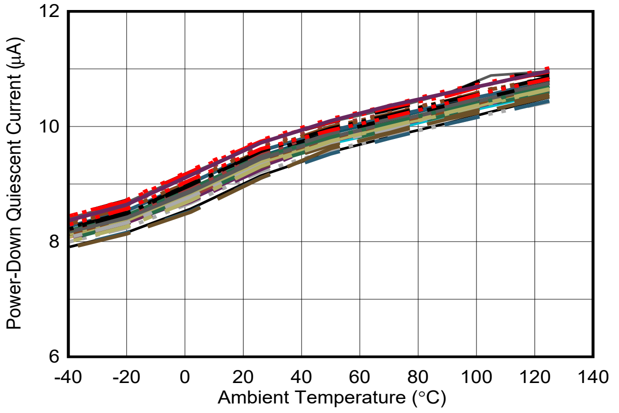
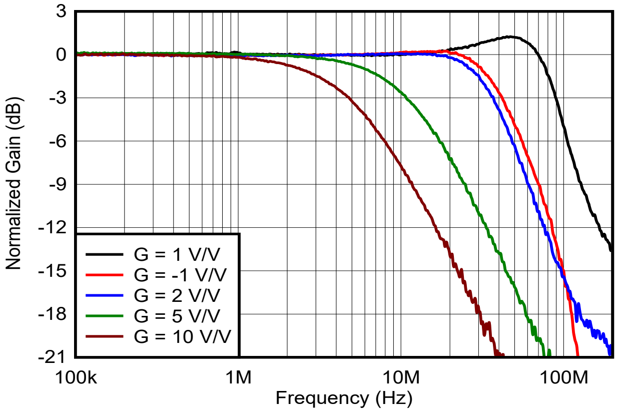


Figure 7-26. Power-Down I_Q vs Ambient Temperature

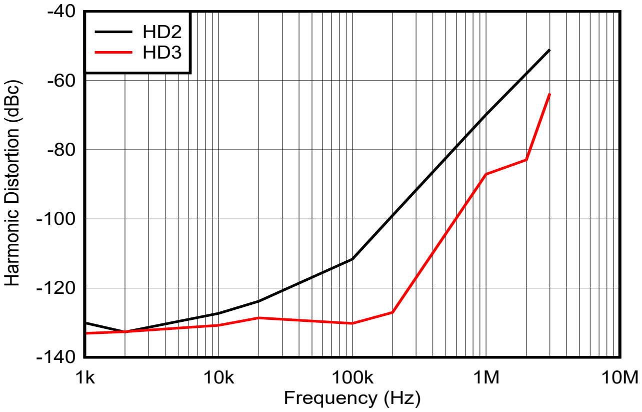
7.9 Typical Characteristics: V_S = 3 V

at V_{S+} = 3 V, V_{S-} = 0 V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-27. Small-Signal Frequency Response vs Gain



V_{OUT} = 1 V_{PP}

Figure 7-28. Harmonic Distortion vs Frequency

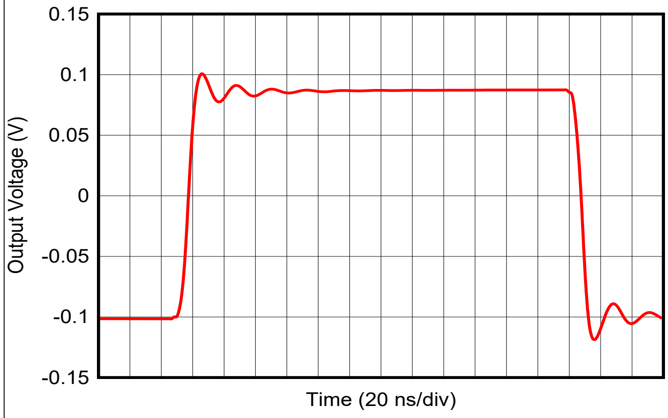


Figure 7-29. Small-Signal Transient Response

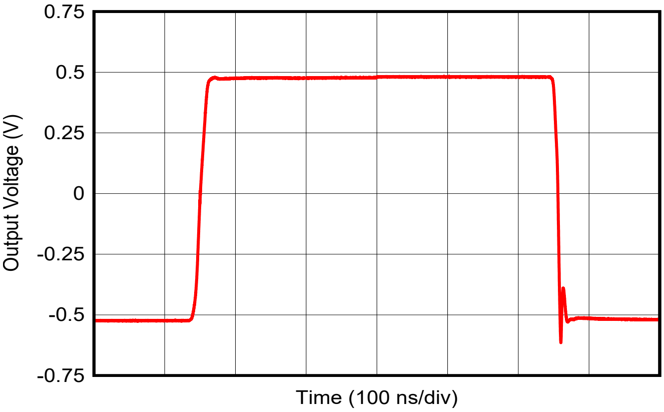
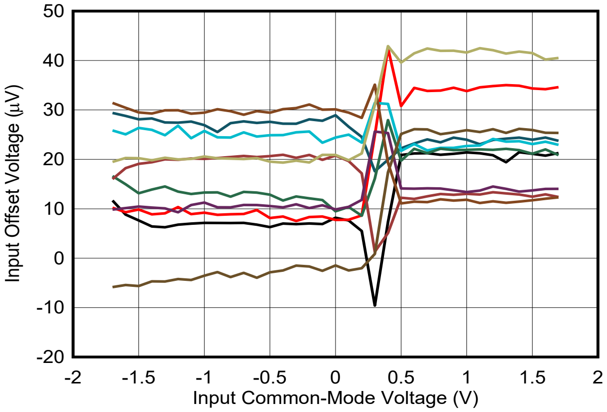
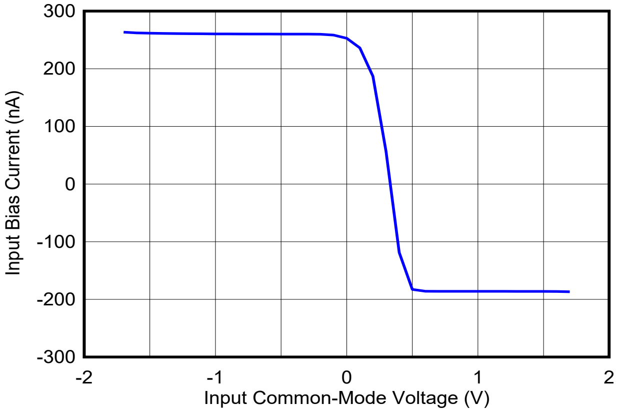


Figure 7-30. Large-Signal Transient Response



V_S = ±1.5 V, measured for 10 units

Figure 7-31. Input Offset Voltage vs Input Common-Mode Voltage



V_S = ±1.5 V

Figure 7-32. Input Bias Current vs Input Common-Mode Voltage

7.9 Typical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, V_{S-} = 0 V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

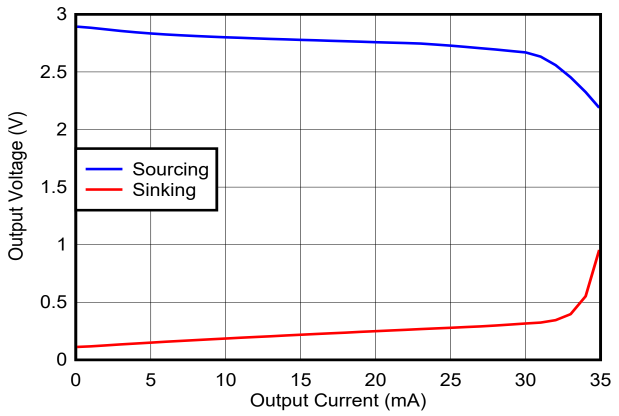
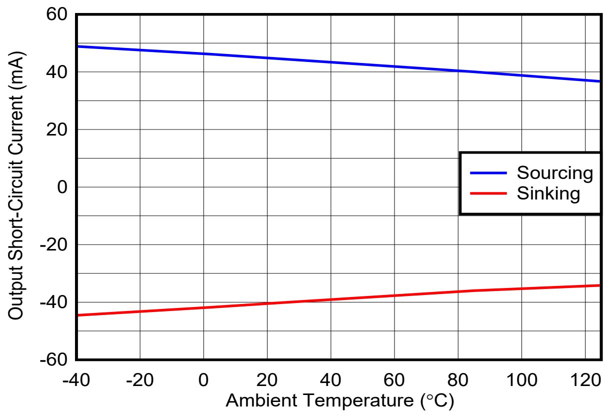


Figure 7-33. Output Voltage vs Load Current



Output saturated and then short-circuited to other supply

Figure 7-34. Output Short-Circuit Current vs Ambient Temperature

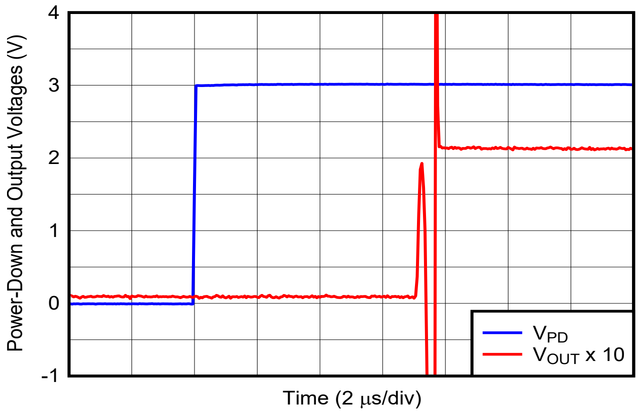


Figure 7-35. Turn-On Time to DC Input

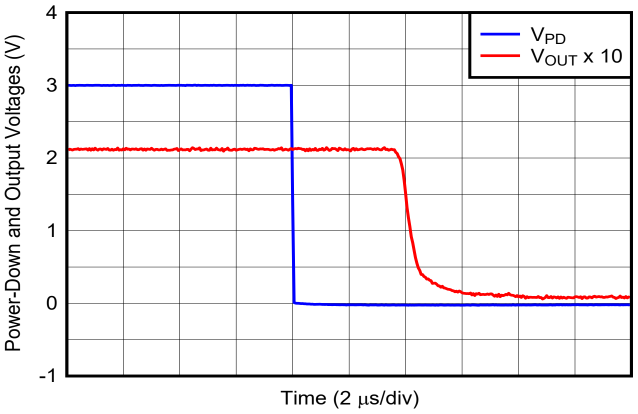
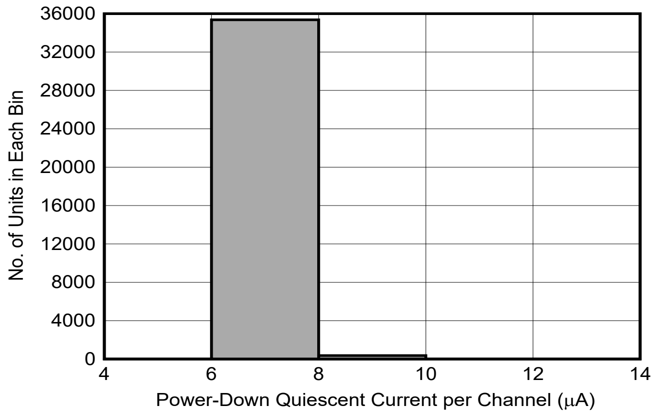


Figure 7-36. Turn-Off Time to DC Input



μ = 7.36 μA, σ = 0.29 μA

Figure 7-37. Power-Down Quiescent Current Distribution

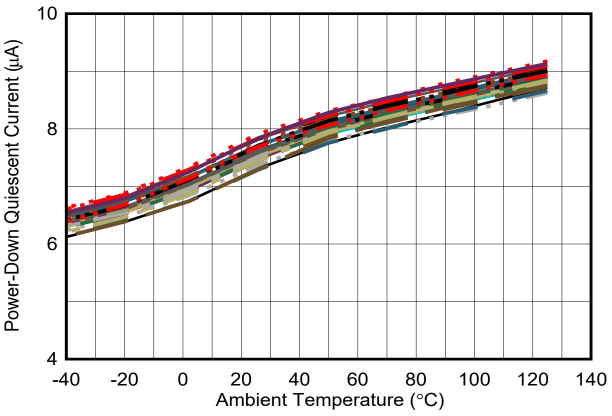
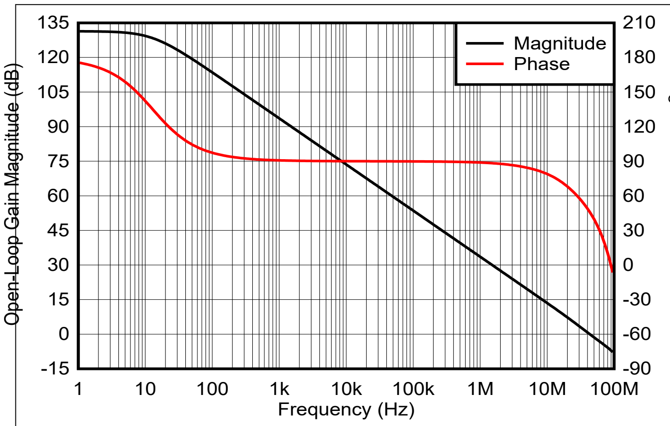


Figure 7-38. Power-Down I_Q vs. Ambient Temperature

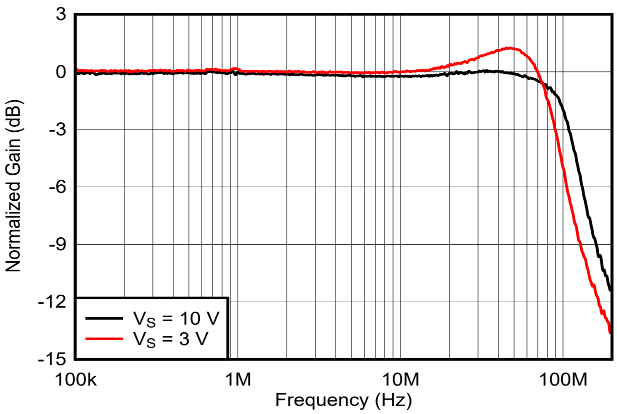
7.10 Typical Characteristics: V_S = 3 V to 10 V

at V_{OUT} = 2 V_{PP}, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



Small-signal response

Figure 7-39. Open-Loop Gain and Phase vs Frequency



V_{OUT} = 20 mV_{PP}

Figure 7-40. Frequency Response vs Supply Voltage

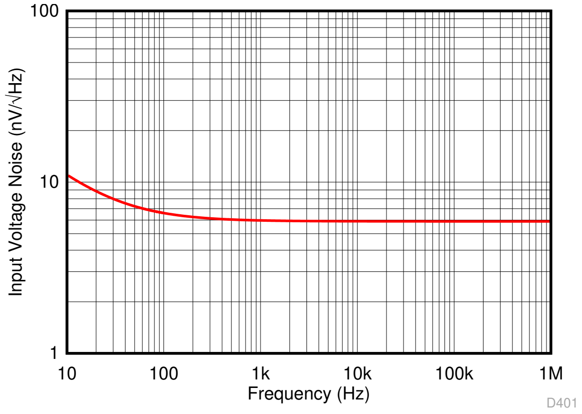


Figure 7-41. Input Voltage Noise Density vs Frequency

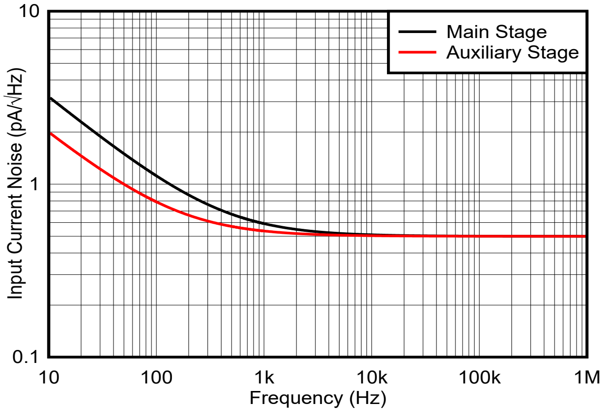


Figure 7-42. Input Current Noise Density vs Frequency

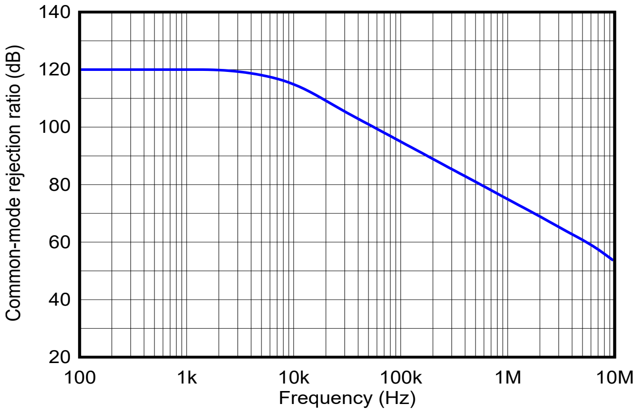


Figure 7-43. Common-Mode Rejection Ratio vs Frequency

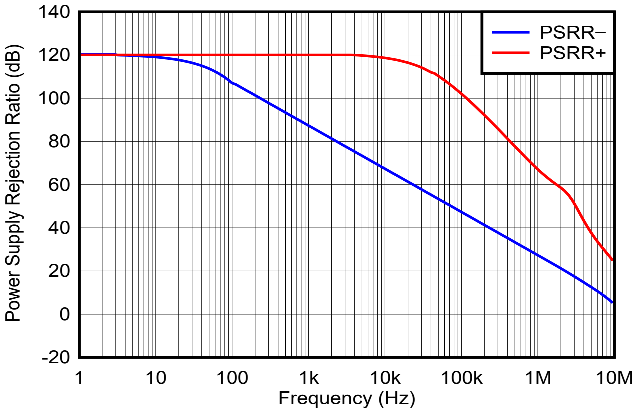


Figure 7-44. Power Supply Rejection Ratio vs Frequency

7.10 Typical Characteristics: V_S = 3 V to 10 V (continued)

at V_{OUT} = 2 V_{PP}, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

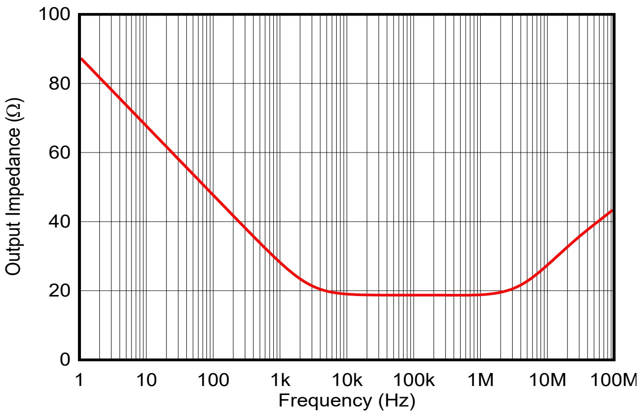
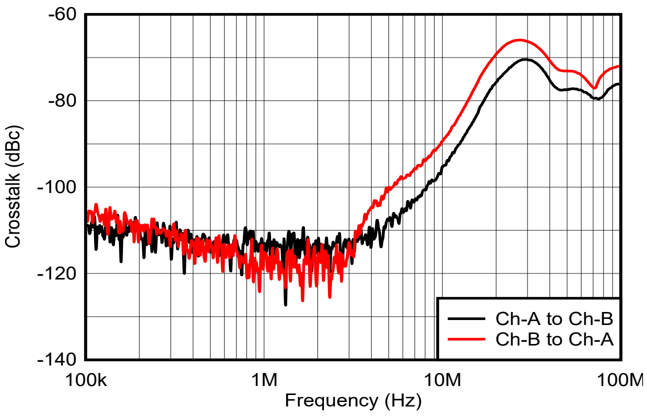


Figure 7-45. Open-Loop Output Impedance vs Frequency



DSN package

Figure 7-46. Crosstalk vs Frequency

8 Detailed Description

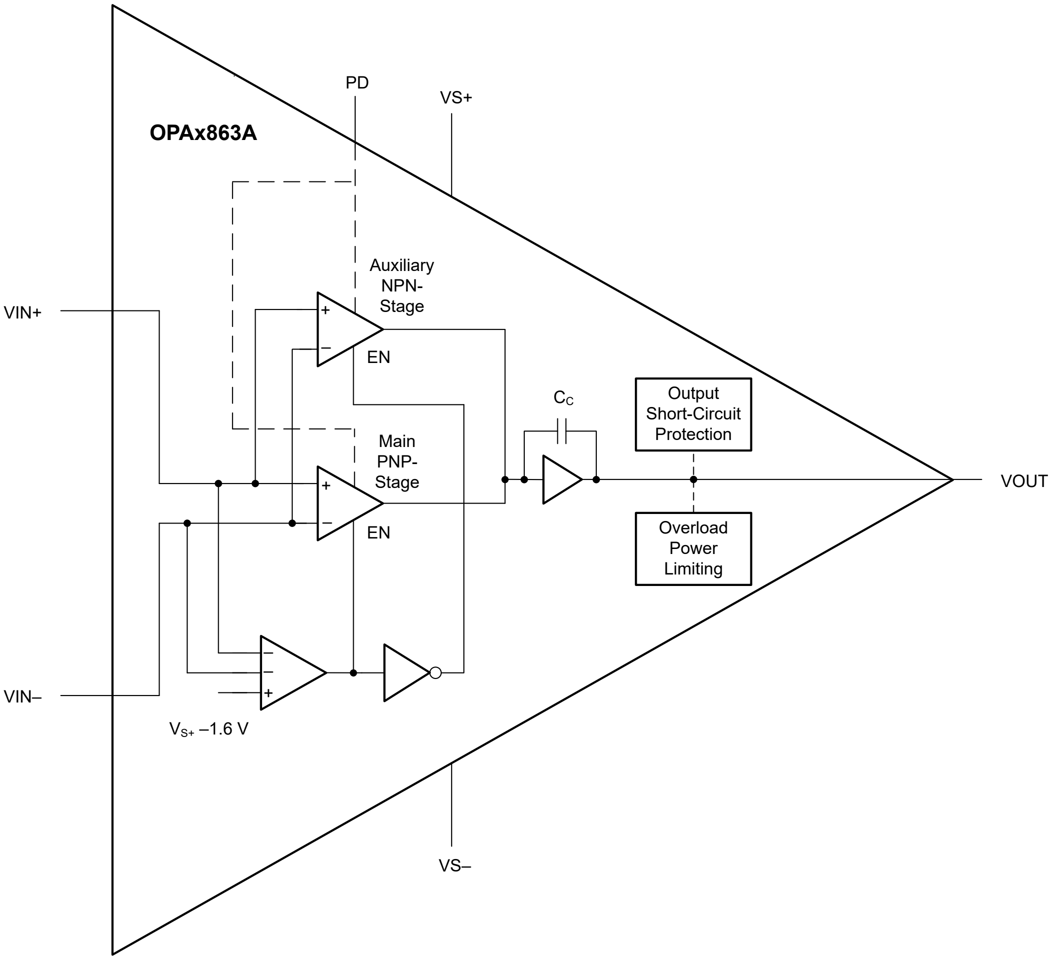
8.1 Overview

The OPAx863A bipolar voltage-feedback amplifiers offer 50 MHz gain-bandwidth product with a proprietary in-package trim technology for high-precision performance with maximum 95 µV input offset voltage and 1.2 µV/°C offset drift. The OPAx863A are low-power, rail-to-rail input and output (RRIO) operational amplifiers with a voltage noise density of 6.3 nV/√Hz and 1/f noise corner at 25 Hz. The OPAx863A work with a wide-supply voltage range from 2.7 V to 12.6 V and consume only 800 µA quiescent current. The OPAx863A operate with 2.7 V supply, are RRIO capable, consume low-power, and offer a power-down mode, which makes them an excellent choice of amplifiers for 3.3-V or lower voltage applications that need excellent ac performance. The main and auxiliary input stages of the amplifier are matched for gain bandwidth product (GBW), noise and offset voltage and designed for applications which require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. For more details of this overload power limit feature, see Section 8.3.2.1. The amplifier's output is protected against short-circuit fault conditions.

The OPAx863A feature a power-down mode (PD) with a PD quiescent current of 20 µA (maximum) with a 3-V supply, with turn-on and turn-off time within less than 8 µs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The OPAx863A include a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from V_{S-} – 0.2 V to V_{S+} – 1.6 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.6 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 6.3 nV/√Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The auxiliary NPN input stage does not use the slew-boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages causes a crossover distortion that must be considered in high-frequency applications requiring excellent linearity. Limit the common-mode input voltage to V_{S+} – 1.6 V (maximum) for main-stage operation across process and ambient temperature.

The OPAx863A are bipolar amplifiers; therefore, the two inputs are protected with antiparallel back-to-back diodes between the inputs, which limits the maximum input differential voltage to 1 V. The amplifier is slew limited, and the two inputs are pulled apart up to 1 V when the antiparallel diodes begin to conduct in very fast input or output transient conditions. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPAx863A feature a rail-to-rail output stage with possible signal swing from V_{S-} + 0.2 V to V_{S+} – 0.2 V. Violating the output headroom of either supply causes output signal clipping and introduces distortion.

The OPAx863A integrate an output short-circuit protection circuit that makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

During overload or fault conditions, bipolar rail-to-rail output (RRO) amplifiers consume excessive quiescent current (five to seven times) with saturated outputs. With saturated outputs, the output signal is clipped with much higher base current from output predriver stage which results in increase in device quiescent current. During this condition, the negative feedback control is disabled and an input differential voltage appears thereby resulting in an input overdrive. During input overdrive, the slew boost circuit engages causing increase in the tail current and hence the device quiescent current. This overall increase in quiescent current can cause excessive battery discharge in portable products shortening operating lifetime or disturb the thermal equilibrium causing irreversible damage due to increased system power dissipation in a multichannel design.

The OPAx863A includes an intelligent overload detection circuit that monitors for output saturation and limits the base drive from output predriver circuit and disables the slew boost circuit in this condition. Table 8-1 compares the increase in quiescent current with 500-mV input overdrive for OPAx863A devices and other voltage-feedback amplifiers without overload power limit.

Table 8-1. Quiescent Current with Saturated Outputs

DEVICE	INPUT DIFFERENTIAL VOLTAGE	QUIESCENT CURRENT DURING OVERLOAD	INCREASE IN I_Q FROM STEADY-STATE CONDITION
OPAx863A with overload power limit	500 mV	1.4 mA	1.8 ×
Competitor amplifier without overload power limit	500 mV	4.05 mA	7.1 ×

8.3.3 ESD Protection

As Figure 8-1 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which makes sure that the current through the ESD diodes remains within the rated value. OPAx863A is a bipolar amplifier; therefore, the two inputs are protected with antiparallel, back-to-back diodes between the inputs that limits the maximum input differential voltage to approximately 1 V. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in fast slewing conditions.

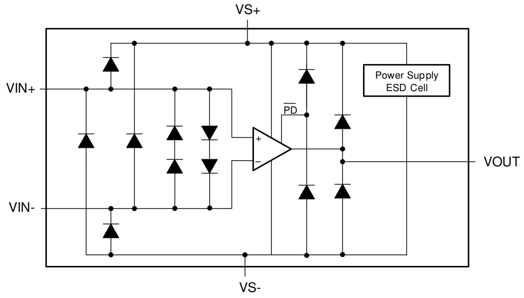


Figure 8-1. Internal ESD Protection

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The OPAx863A includes a power-down mode for low-power standby operation with a quiescent current of 8.5 µA (typical) and high output impedance. Many low-power systems are active for only a small time interval when the parameters of interest are measured and remain in low-power standby mode for a majority of the time, for an overall small average power consumption. The OPAx863A enables such low-power operation with quick turn-on within less than 8 µs. See the *Electrical Characteristics* tables for power-down pin control thresholds.

The OPAx863A is enabled with the $\overline{\text{PD}}$ pin driven to V_{S+} – 0.5 V or greater. The device powers down if the $\overline{\text{PD}}$ pin is driven to V_{S+} – 1.5 V or less with a driver device capable of sinking approximately 1 µA (typical) current from the $\overline{\text{PD}}$ pin. If level translation is needed to realize the $\overline{\text{PD}}$ pin thresholds for enable or power-down modes of operation, use an external pullup resistor from $\overline{\text{PD}}$ pin to V_{S+} driven with an open-collector output.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx863A are classic voltage-feedback amplifiers, where each channel has two high-impedance inputs and a low-impedance output. Theses devices feature a GBW of 50 MHz, 6.3- nV/√Hz noise, RRIO capability, and high-precision performance consuming only 800 µA of quiescent current. These features make the OPAx863A an excellent choice for use in precision data acquisition, reference buffering with fast settling, high gain and filter circuits. The overload power limit feature makes the OPAx863A truly low power in high-gain multichannel systems, and limits any increase in quiescent current during output overload conditions.

9.2 Typical Applications

9.2.1 Active Filters

Active filter circuits are used to amplify signals in the pass band, attenuate signals in the stop band, and also limit the integrated noise at the amplifier output. The OPAx863A, with a wide bandwidth and high-precision performance, is an excellent device for designing multifeedback (MFB) low-pass filter circuits.

9.2.1.1 Design Requirements

This section discusses the design of a MFB low-pass active filter with a cut-off frequency at 2 MHz and the impact of amplifier's gain-bandwidth (GBW) on filter performance.

9.2.1.2 Detailed Design Procedure

Figure 9-1 shows the use of OPAx863A in a second-order multifeedback (MFB) low-pass filter with a cut-off frequency of 2 MHz. The frequency response of the circuit in Figure 9-1 is compared for various amplifiers with different gain-bandwidth products and shown in Figure 9-2:

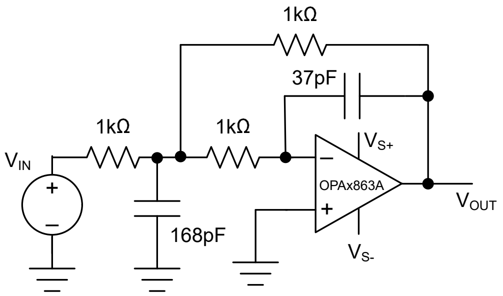


Figure 9-1. MFB Low-Pass Filter Circuit Using the OPAx863A

Table 9-1. Impact of Amplifier GBW on Cutoff Frequency

DEVICE	GBW (MHz)	CUTOFF FREQUENCY (MHz)
TLV9051	5	1.59
LMV641	10	1.78
OPA2834	20	1.87
OPAx863A	50	1.95
OPA836	110	1.98

Table 9-1 provides the following benefits of using OPAx863A in an MFB low-pass filter circuit:

- High-precision measurements with low offset voltage across the operating temperature range for low-frequency signals in pass band
- High linearity due to the larger GBW and loop gain for low-frequency signals in pass band
- Higher accuracy of cutoff frequency and smaller variations over process and temperature
- Small integrated output noise due to low-pass filtering

Based on Figure 9-2, and as with the OPAx863A, use an amplifier with a gain bandwidth product at least 20 × greater than the filter cutoff frequency. This configuration results in a high-precision and high-linearity, low-pass-filter design.

9.2.1.3 Application Curves

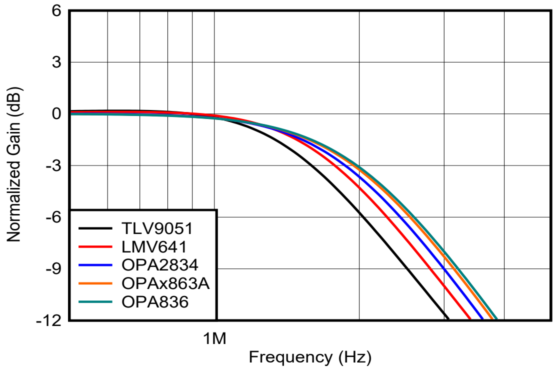


Figure 9-2. MFB Low-Pass Filter Frequency Response vs GBW

9.2.2 Low-Power SAR ADC Driver and Reference Buffer

Figure 9-3 shows the use of the OPAx863A as a SAR ADC input driver driving the .ADS7057 sensors, which are used for interface with the physical environment, exhibit high output impedance, and cannot drive SAR ADC inputs directly. A wide-GBW amplifier, such as the OPAx863A, is needed to charge the switching capacitors at the SAR ADC input, and quickly settle to the required accuracy within the given acquisition time. The OPAx863A wide-GBW, high precision performance enables fast settling, high accuracy sensor measurements, and reference buffering for precision ADCs.

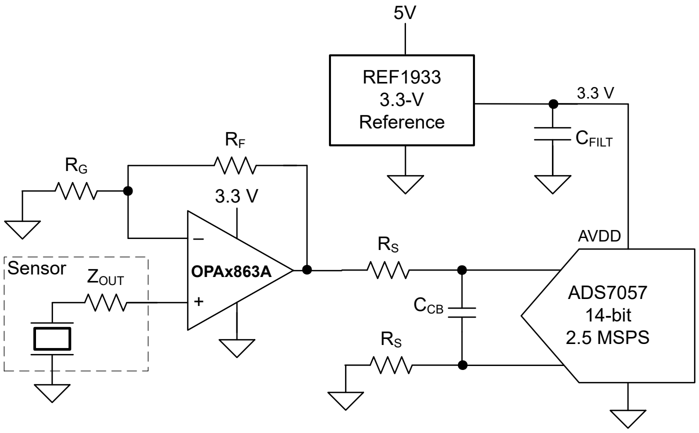


Figure 9-3. OPAx863A as a Precision SAR ADC Driver

9.3 Power Supply Recommendations

The OPAx863A is intended to operate on supplies ranging from 2.7 V to 12.6 V. The OPAx863A devices operate on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply has numerous advantages. The dc errors, due to the –PSRR term, can be minimized with the negative supply at ground. Typically, ac performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. Only the positive supply has these capacitors for single-supply operation. Use these capacitors from each supply to ground when a split-supply is used. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier (like the OPAx863A) requires careful attention to board layout parasitics and external component types. The *High Speed Amplifiers Generic DSN Evaluation Module* user's guide can be used as a reference when designing the circuit board. Recommendations that optimize performance includes the following:

1. **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability on the noninverting input and can react with the source impedance to cause unintentional band-limiting. Open a window around the signal I/O pins in all of the ground and power planes around those pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections these capacitors. Use larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, on the supply pins. These capacitors can be placed somewhat farther from the device and shared among several devices in the same area of the PCB.
3. **Carefully select and place external components to preserve the high-frequency performance of the OPAx863A.** Use low-reactance-type resistors. Surface-mount resistors work best and allow a tighter overall layout. Place other network components, such as noninverting input termination resistors, close to the package. Keep resistor values as low as possible and consistent with load-driving considerations. Lower the resistor values to keep the resistor noise terms low and minimize the effect of the parasitic capacitance. Lower resistor values, however, increase the dynamic power consumption because R_F and R_G become part of the amplifier output load network.

9.4.2 Layout Example

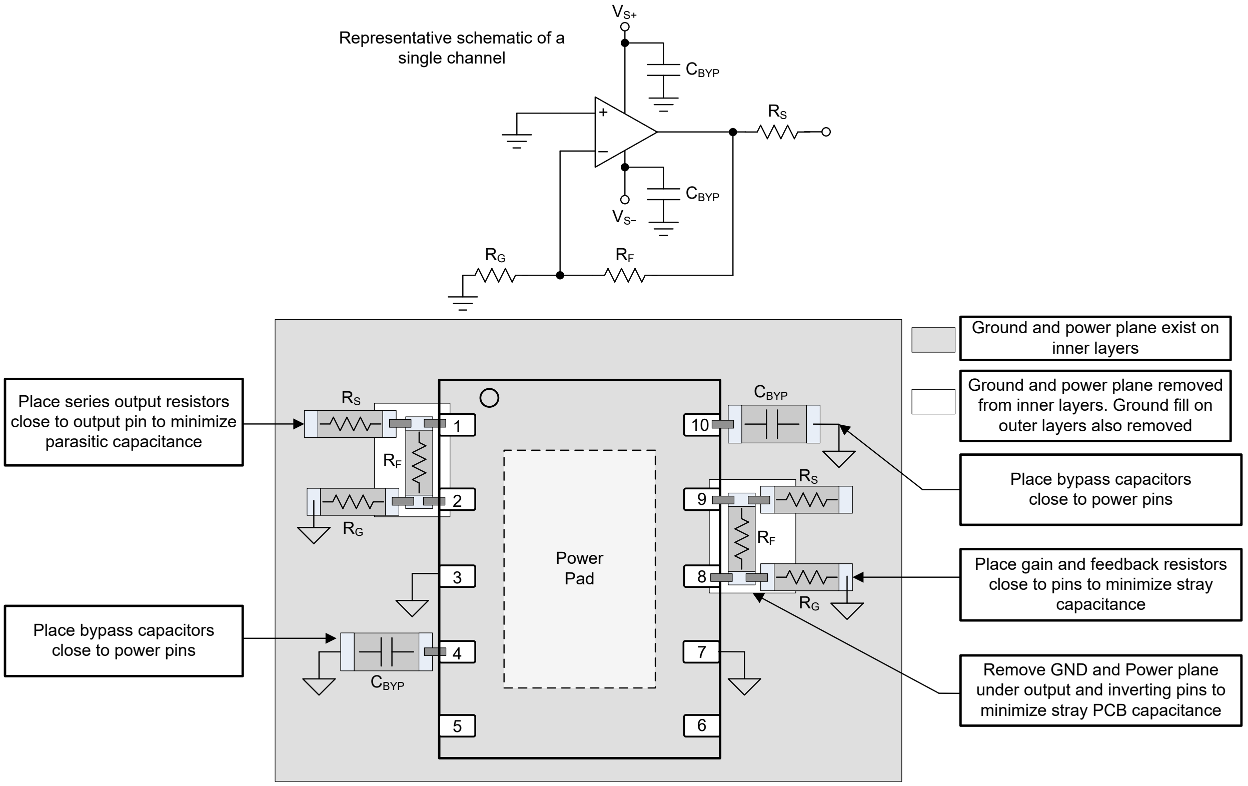


Figure 9-4. Layout Recommendation for Dual-Channel DSN Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High Speed Amplifiers Generic DSN Evaluation Module* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

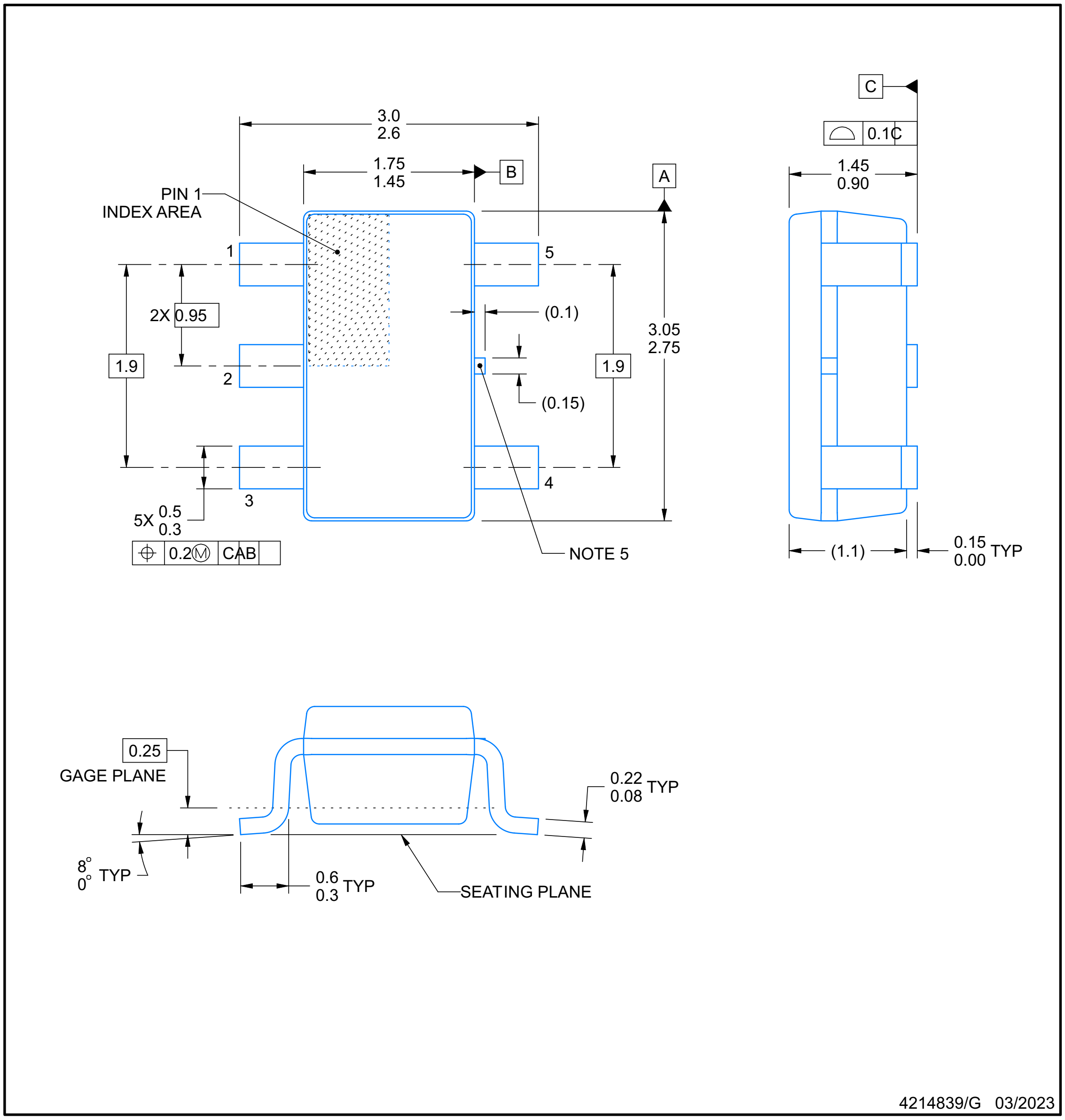
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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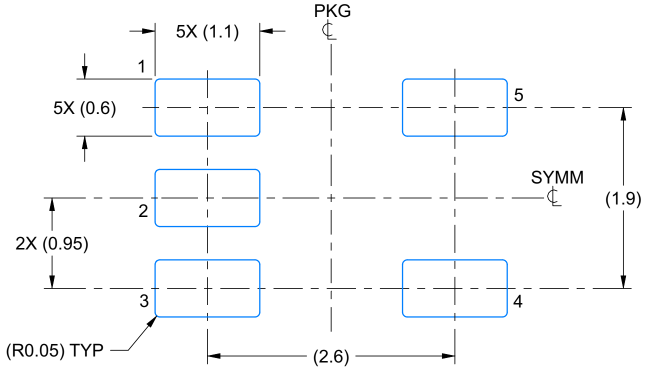
EXAMPLE BOARD LAYOUT

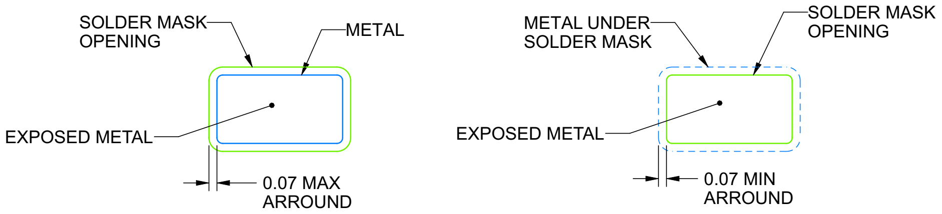
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/G 03/2023

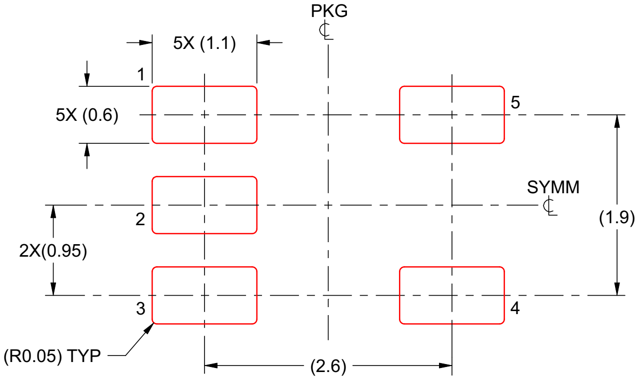
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2863AIDSNR	ACTIVE	SON	DSN	10	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2863A	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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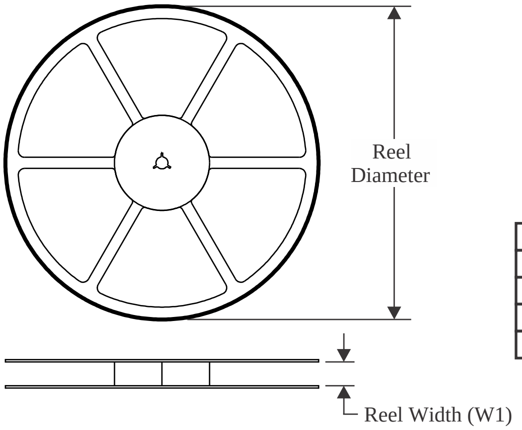
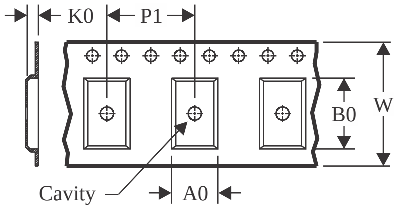
TAPE AND REEL INFORMATION

REEL DIMENSIONS

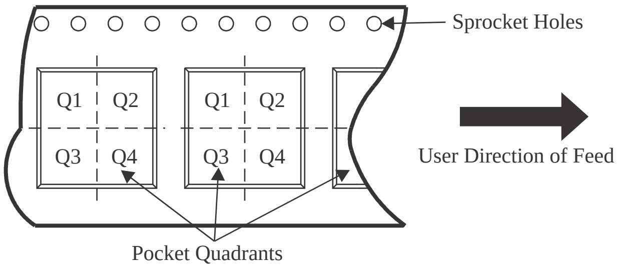


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

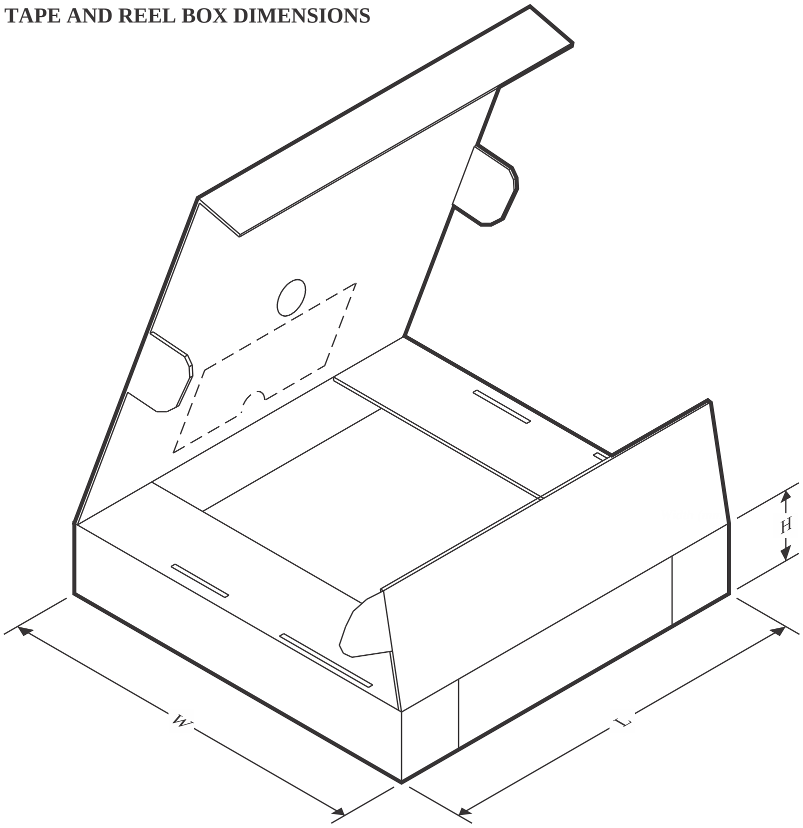
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2863AIDSNR	SON	DSN	10	5000	330.0	12.4	3.15	3.15	0.75	8.0	12.0	Q2

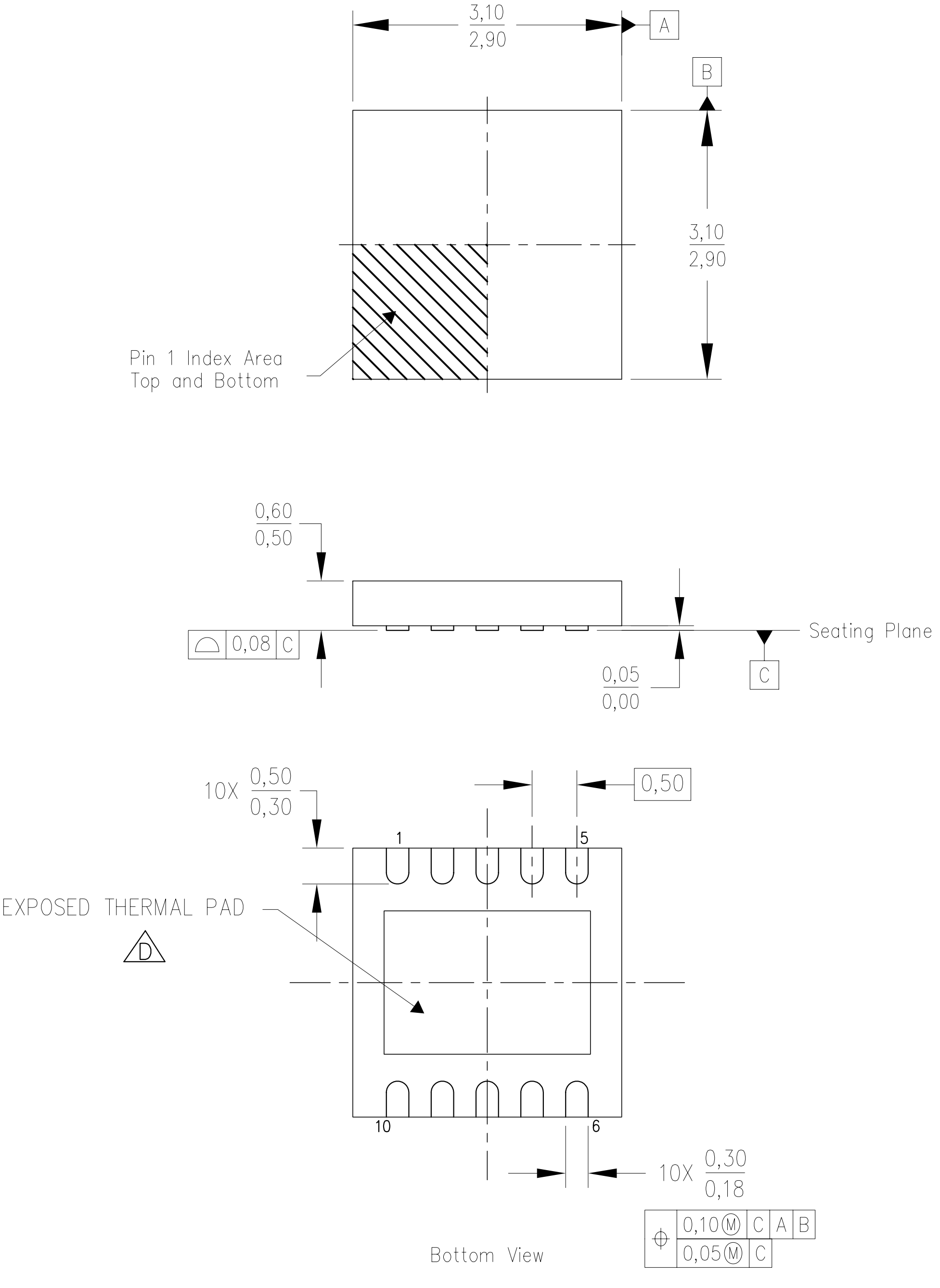
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2863AIDSNR	SON	DSN	10	5000	364.0	357.0	31.0

DSN (S–PUSON–N10) PLASTIC QUAD FLATPACK NO–LEAD



4209052/B 11/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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