MOSFET - Power, Single N-Channel, μ8FL

30 V, 2.25 mΩ, 162 A

NVTFS4C02N

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	2.25 mΩ @ 10 V	162 A
	3.1 mΩ @ 4.5 V	

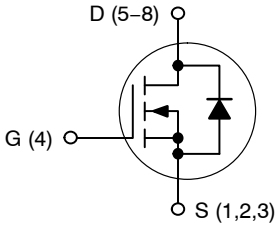
Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C02NWF − Wettable Flanks Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

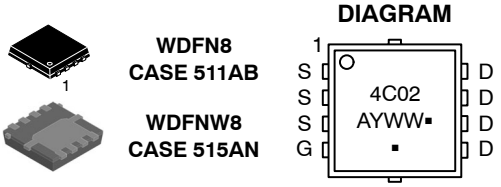
Applications

- Reverse Battery Protection
- DC−DC Converter Output Driver

N−Channel MOSFET



MARKING DIAGRAM



4C02 = Specific Device Code
02WF = Specific Device Code of NVTFS4C02NWF
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	28.3	A
		T_A = 100°C		20	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	3.2	W
		T_A = 100°C		1.6	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	162	A
		T_C = 100°C		115	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	107	W
		T_C = 100°C		53.5	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	500	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	100	A
Drain to Source dV/dt			dV/dt	6.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (I_L = 37 A_{pk}) (Note 3)			E_{AS}	162	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.
3. This is the absolute maximum ratings. Parts are 100% tested at T_J = 25°C, V_{GS} = 10 V, I_L = 36 A, E_{AS} = 65 mJ.

ORDERING INFORMATION

Device	Package	Shipping†
NVTFS4C02NTAG	WDFN8	1500 / Tape & Reel
NVTFS4C02NWFTAG	WDFNW8	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.4	°C/W
Junction−to−Ambient − Steady State	$R_{\theta JA}$	46	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				13.8		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V	T_J = 25°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.3	1.6	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A		1.9	2.25	mΩ
		V_{GS} = 4.5 V	I_D = 20 A		2.7	3.1	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 50 A			140		S
Gate Resistance	R_G				0.9		Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			2980		pF
Output Capacitance	C_{OSS}				1200		
Reverse Transfer Capacitance	C_{RSS}				55		
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DD} = 15 V			25		nC
Capacitance Ratio	C_{RSS}/C_{ISS}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz			0.018		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 50 A			20		nC
Threshold Gate Charge	$Q_{G(TH)}$				4.7		
Gate−to−Source Charge	Q_{GS}				8.5		
Gate−to−Drain Charge	Q_{GD}				4		
Gate Plateau Voltage	V_{GP}				2.8		V
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 50 A			45		nC
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 50 A, R_G = 3.0 Ω			12		ns
Rise Time	t_r				116		
Turn−Off Delay Time	$t_{d(OFF)}$				25		
Fall Time	t_f				10		

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 50 A, R_G = 3.0 Ω			9		ns
Rise Time	t_r				102		
Turn−Off Delay Time	$t_{d(OFF)}$				33		
Fall Time	t_f				6		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.8	1.1	V
			T_J = 125°C		0.6		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 50 A			42		ns
Charge Time	t_a				21		
Discharge Time	t_b				21		
Reverse Recovery Charge	Q_{RR}				28		nC

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

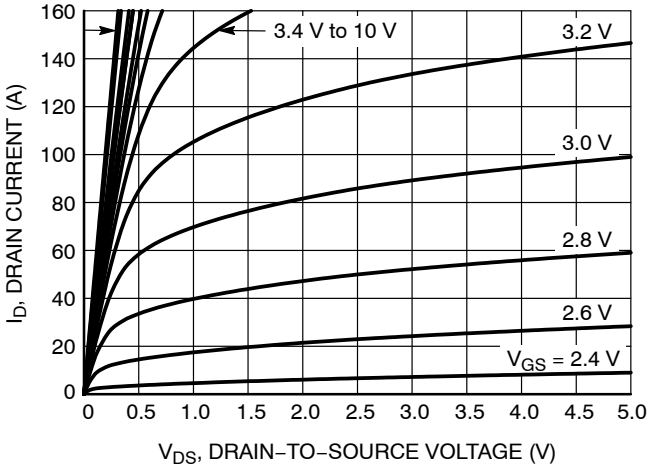


Figure 1. On−Region Characteristics

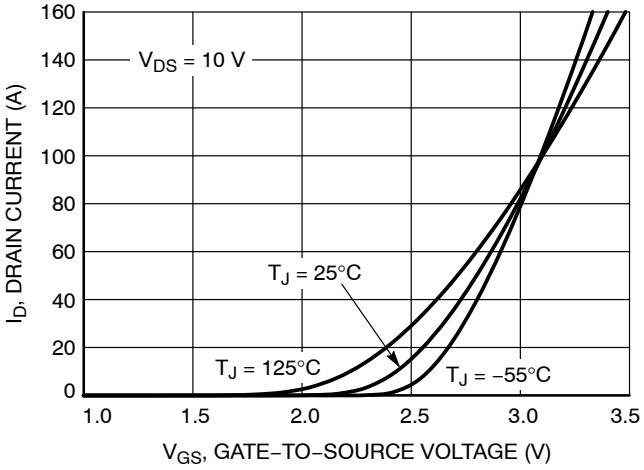


Figure 2. Transfer Characteristics

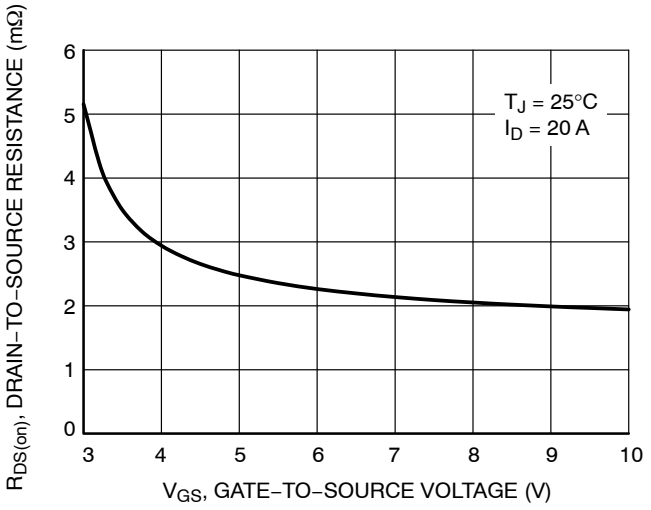


Figure 3. On−Resistance vs. Gate−to−Source Voltage

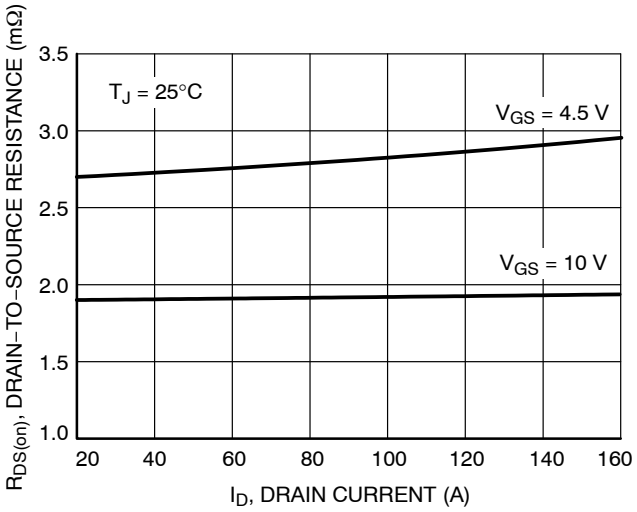


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

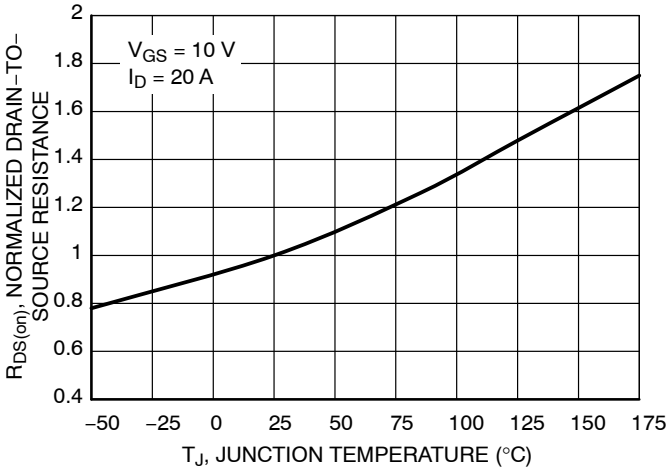


Figure 5. On−Resistance Variation with Temperature

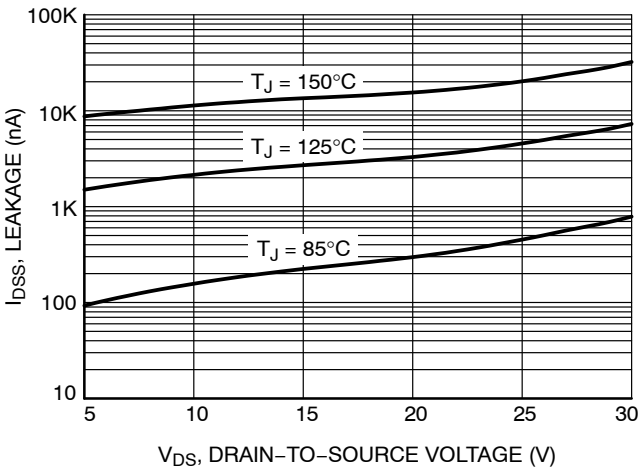


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

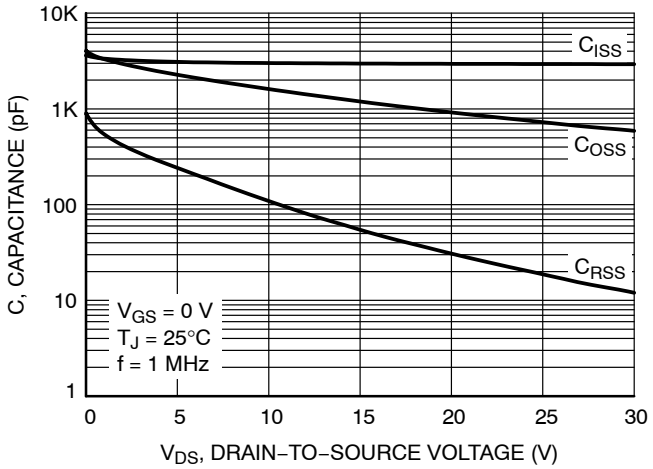


Figure 7. Capacitance Variation

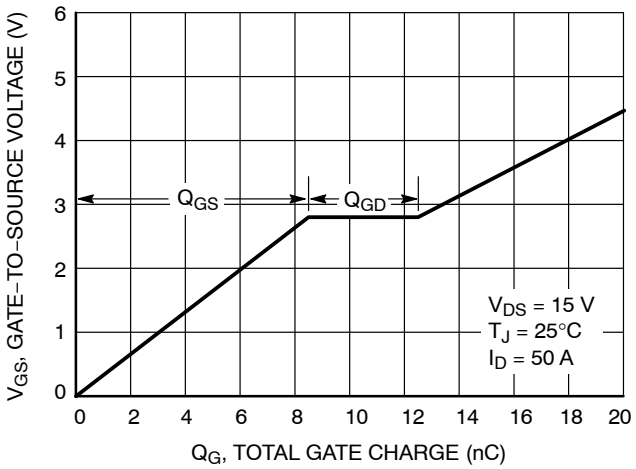


Figure 8. Gate−to−Source vs. Total Charge

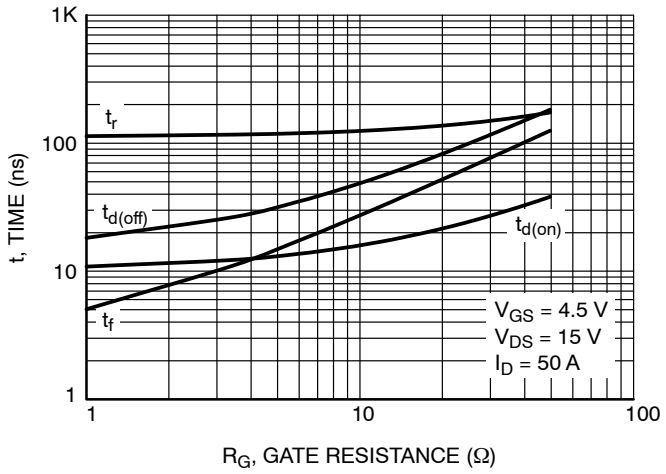


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

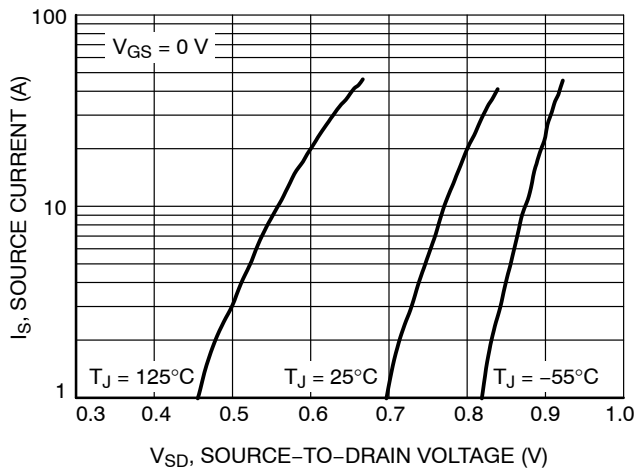


Figure 10. Diode Forward Voltage vs. Current

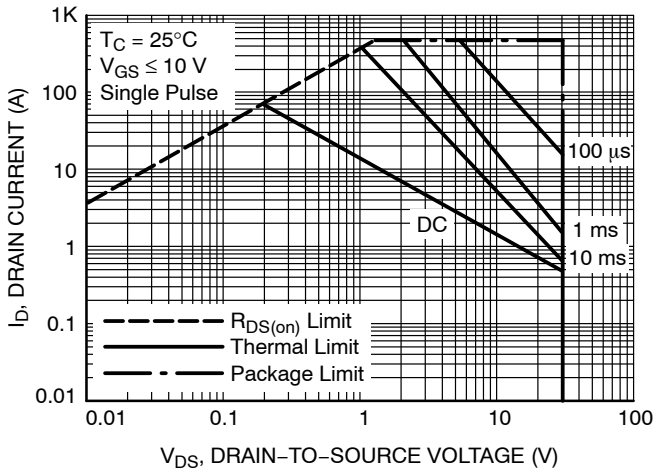


Figure 11. Maximum Rated Forward Biased Safe Operating Area

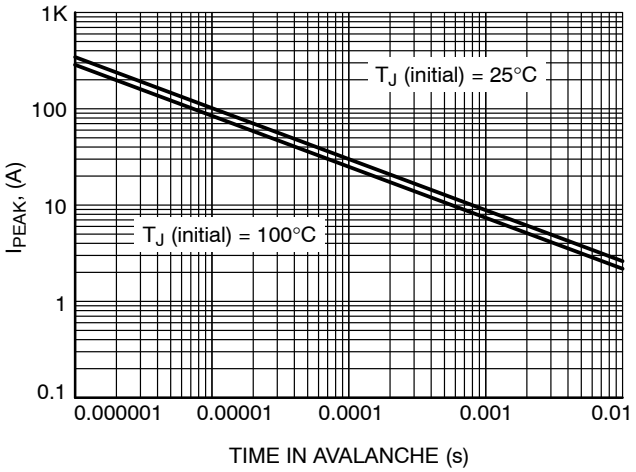


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

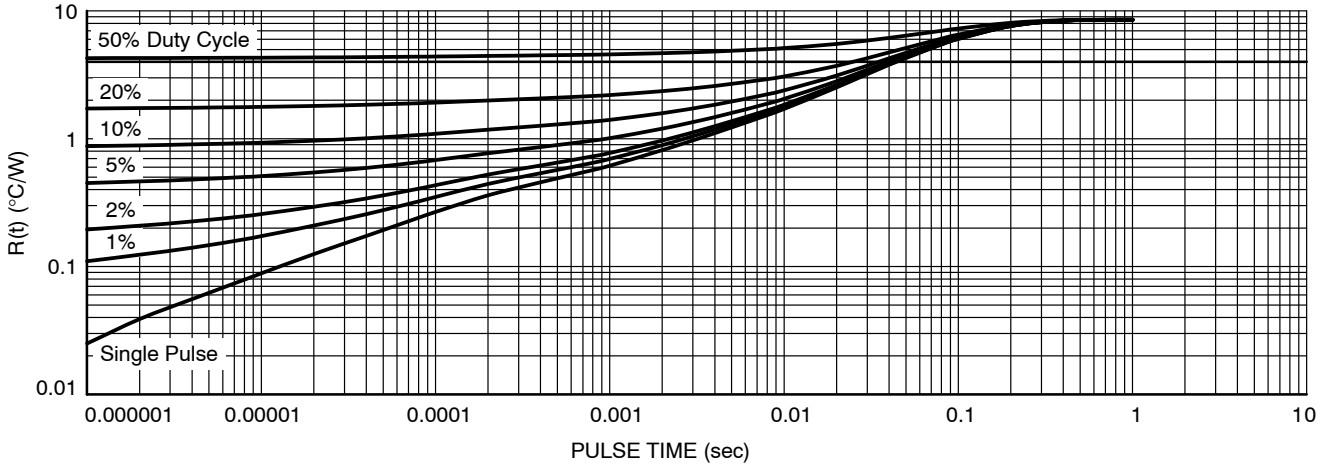
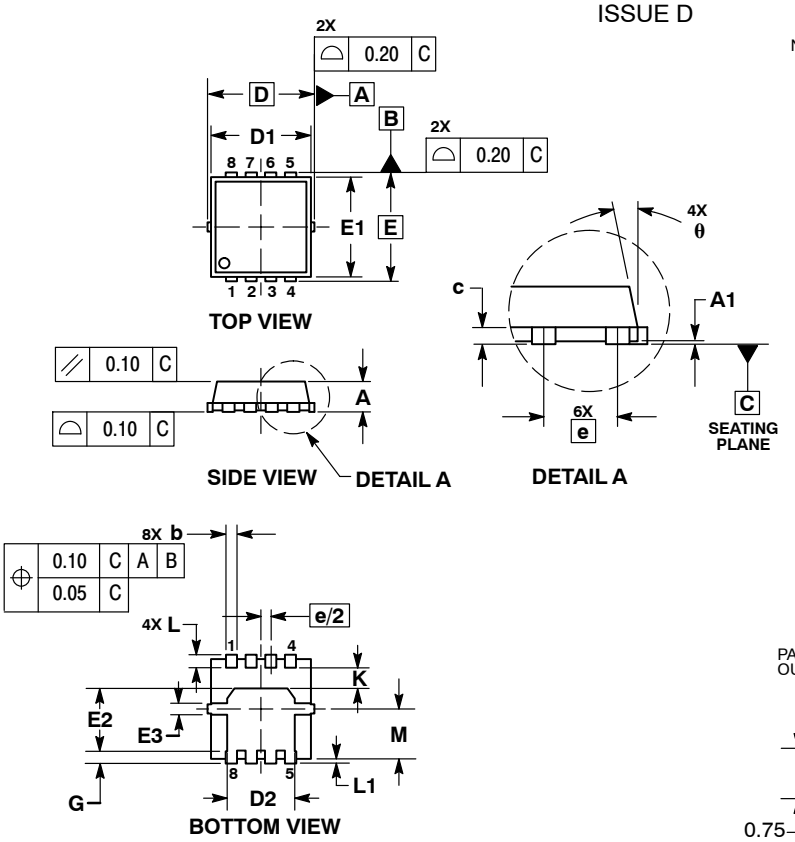


Figure 13. Thermal Characteristics

PACKAGE DIMENSIONS

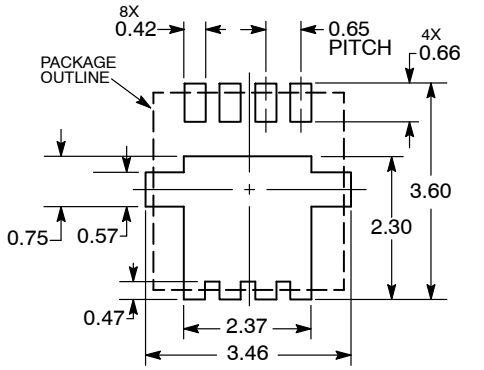
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*

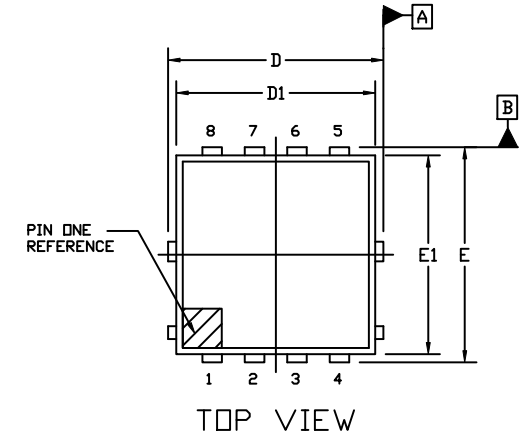


DIMENSION: MILLIMETERS

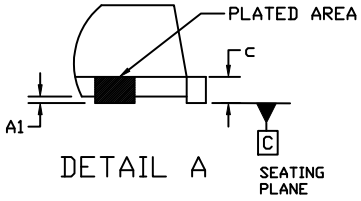
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WDFNW8 3.3x3.3, 0.65P (Full−Cut μ8FL WF)
CASE 515AN
ISSUE O



TOP VIEW

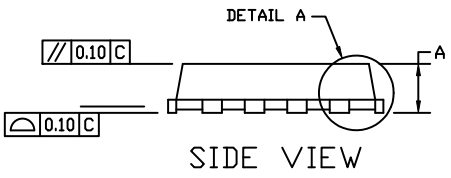


DETAIL A

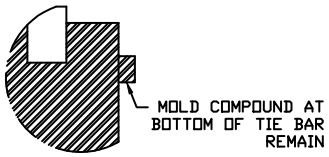
NOTES:

1. DIMENSIONING AND TOLERANCING PER.ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

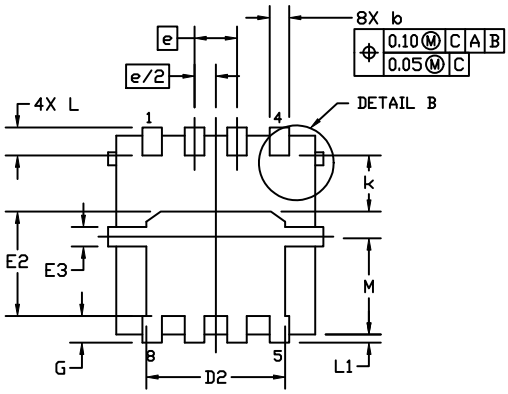
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



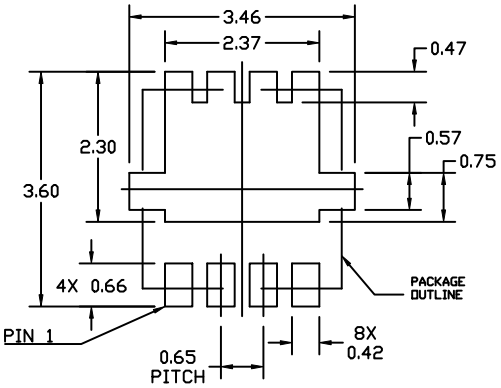
SIDE VIEW



DETAIL B



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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