

# MOSFET - Power, Single N-Channel, DFN5/DFNW5

## 30 V, 4.8 mΩ, 55 A

### NVMFS4C308N

#### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC-Q101 Qualified and PPAP Capable
- NVMFS4C308NWF – Wettable Flanks Option for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Applications

- Reverse Battery Protection
- DC-DC Converters Output Driver

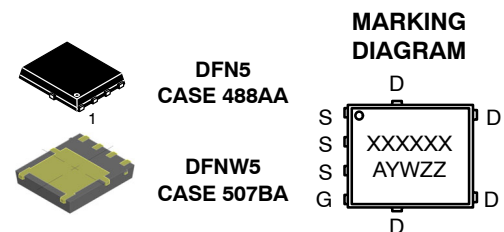
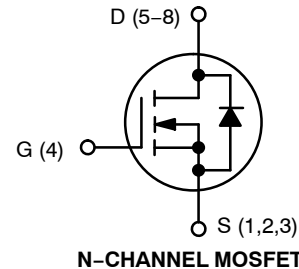
#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	$I_D$	$T_A = 25^\circ\text{C}$	17.2
		$T_A = 100^\circ\text{C}$	12.3
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	$P_D$	$T_A = 25^\circ\text{C}$	3
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	$I_D$	$T_C = 25^\circ\text{C}$	55
		$T_C = 100^\circ\text{C}$	39
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)	$P_D$	$T_C = 25^\circ\text{C}$	30.6
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	144
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	23	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_L = 29 \text{ A}_{pk}, L = 0.1 \text{ mH}, R_{GS} = 25 \Omega$ ) (Note 3)	$E_{AS}$	42	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. This is the absolute maximum rating. Parts are 100% tested at  $T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_L = 21 \text{ A}_{pk}, E_{AS} = 22 \text{ mJ}$ .

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	4.8 mΩ @ 10 V	55 A
	7.0 mΩ @ 4.5 V	



- 4C08N = Specific Device Code for NVMFS4C308N
- 4C08WF = Specific Device Code of NVMFS4C308NWF
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

#### ORDERING INFORMATION

Device	Package	Shipping†
NVMFS4C308NT1G	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS4C308NWF1G	DFNW5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVMFS4C308N

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.9	°C/W
Junction-to-Ambient – Steady State	$R_{\theta JA}$	49.8	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSSt}$	$V_{GS} = 0\text{ V}, I_{D(aval)} = 8.4\text{ A}, T_{case} = 25^\circ\text{C}, t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			13.8		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.9		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		4.0	4.8	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		5.9	7.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		42		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$	0.3	1.0	2.0	$\Omega$

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1113	1670	pF
Output Capacitance	$C_{OSS}$			702		
Reverse Transfer Capacitance	$C_{RSS}$			39		
Capacitance Ratio	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.035		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		8.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.8		
Gate-to-Source Charge	$Q_{GS}$			3.5		
Gate-to-Drain Charge	$Q_{GD}$			3.3		
Gate Plateau Voltage	$V_{GP}$			3.4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		18.2		nC

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.0		ns
Rise Time	$t_r$			33		
Turn-Off Delay Time	$t_{d(OFF)}$			15		
Fall Time	$t_f$			4.0		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0		ns
Rise Time	$t_r$			26		
Turn-Off Delay Time	$t_{d(OFF)}$			19		
Fall Time	$t_f$			3.0		

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

# NVMFS4C308N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.79	1.1	V
			$T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			28.3		ns
Charge Time	$t_a$				14.5		
Discharge Time	$t_b$				13.8		
Reverse Recovery Charge	$Q_{RR}$				15.3		

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NVMFS4C308N

## TYPICAL CHARACTERISTICS

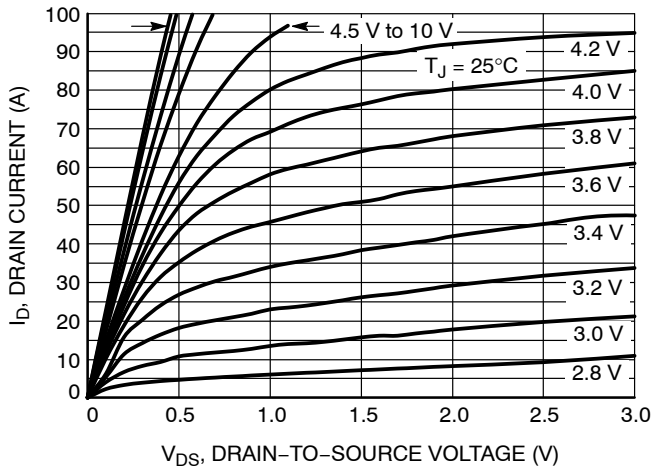


Figure 1. On-Region Characteristics

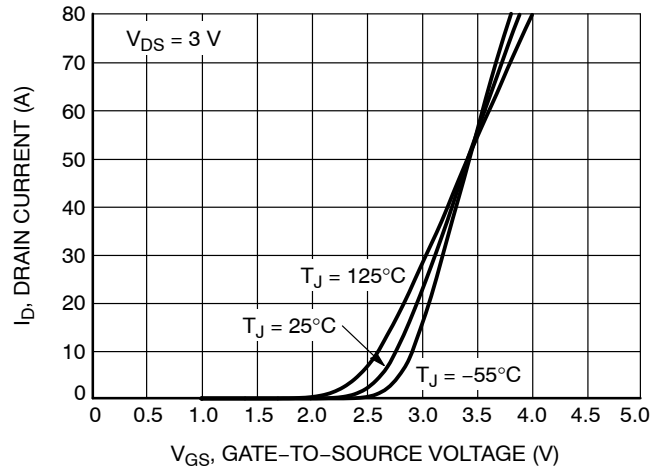


Figure 2. Transfer Characteristics

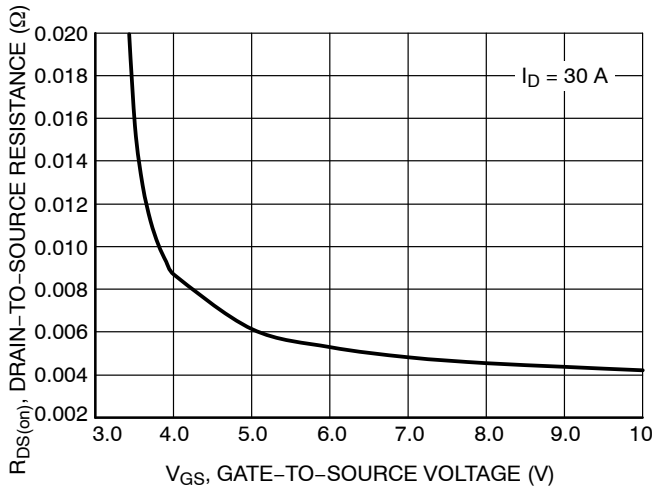


Figure 3. On-Resistance vs.  $V_{GS}$

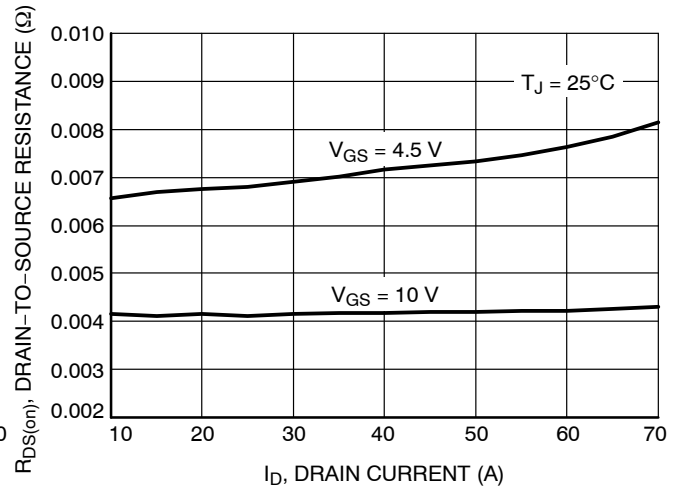


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

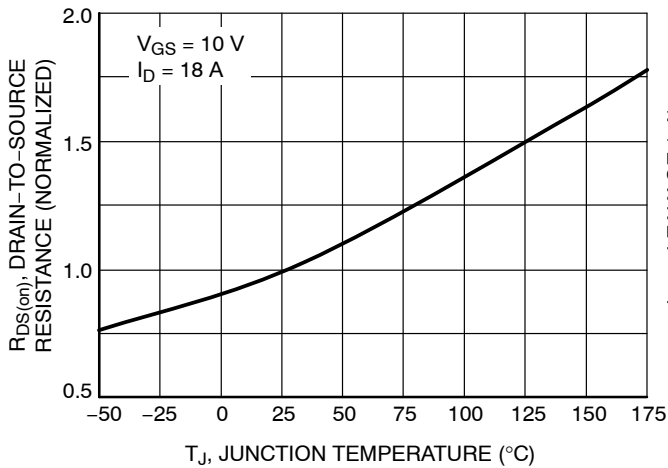


Figure 5. On-Resistance Variation with Temperature

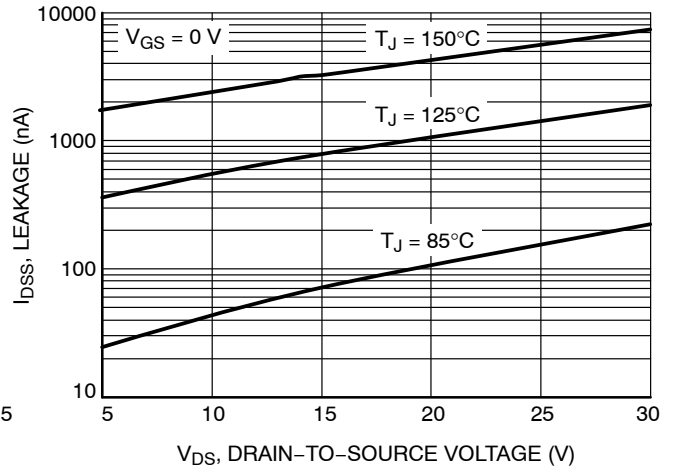


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFS4C308N

## TYPICAL CHARACTERISTICS

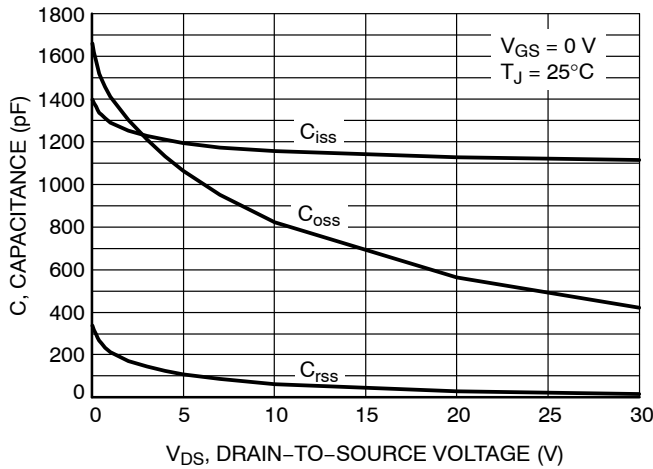


Figure 7. Capacitance Variation

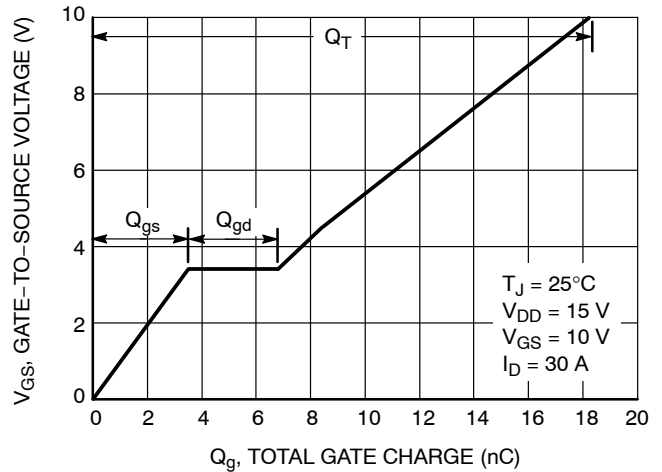


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

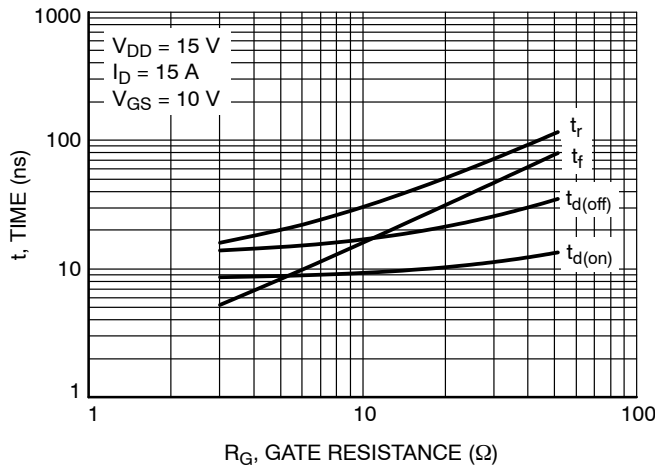


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

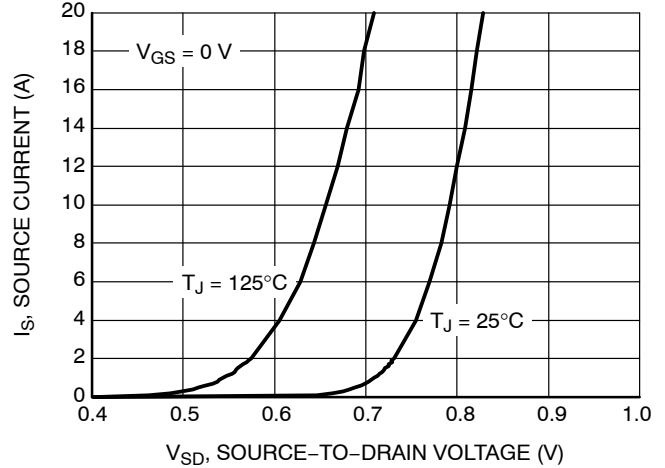


Figure 10. Diode Forward Voltage vs. Current

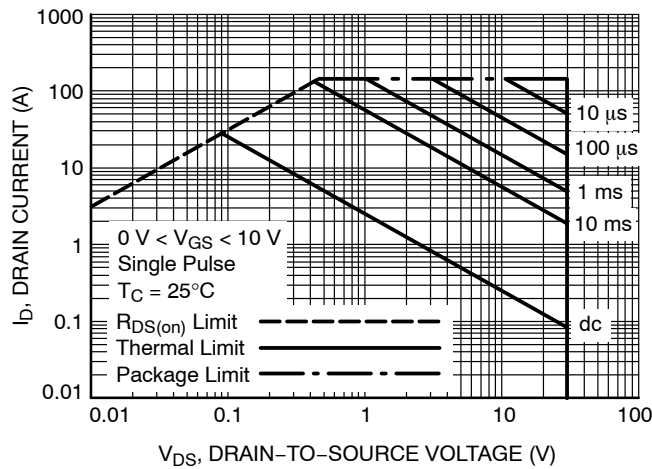


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NVMFS4C308N

## TYPICAL CHARACTERISTICS

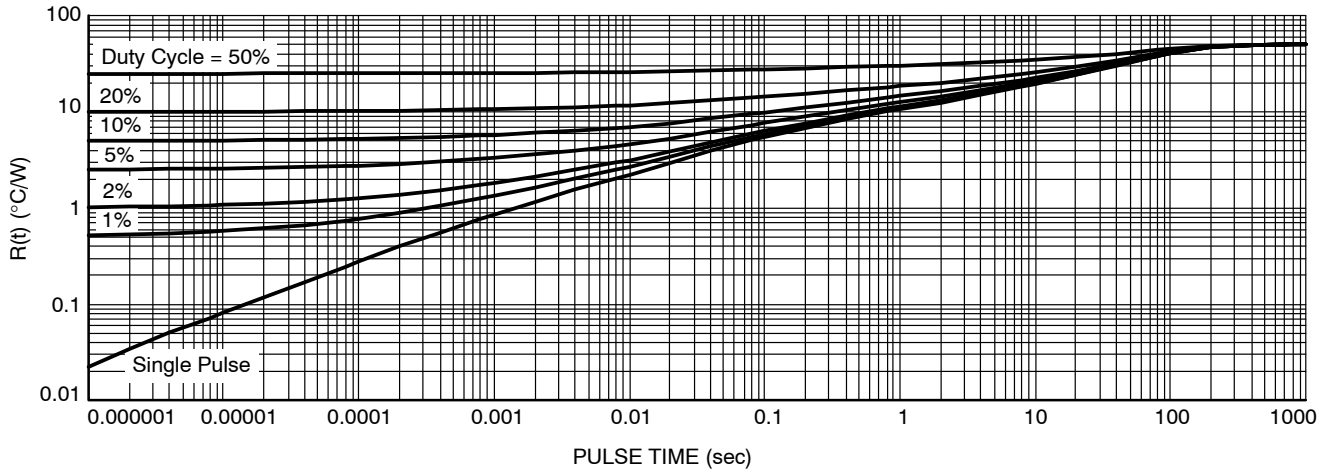


Figure 12. Thermal Response

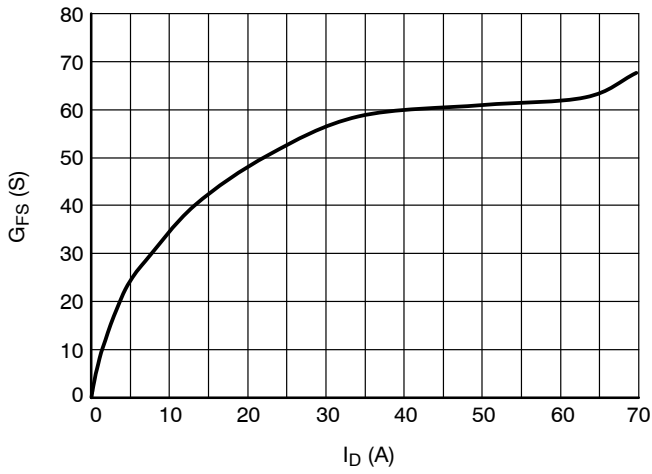


Figure 13.  $G_{FS}$  vs.  $I_D$

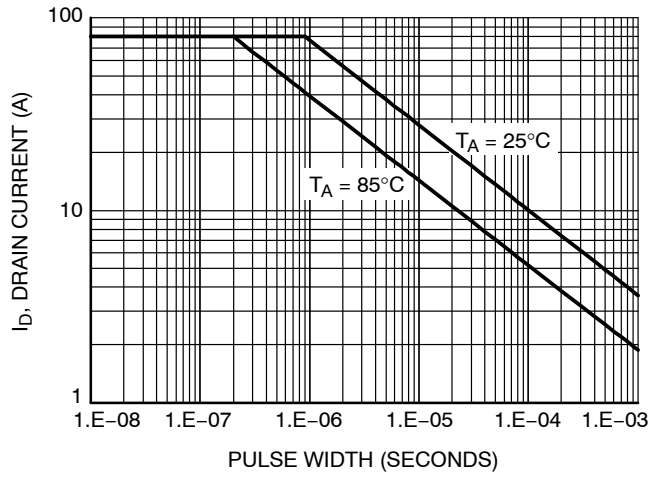


Figure 14. Avalanche Characteristics

# MECHANICAL CASE OUTLINE

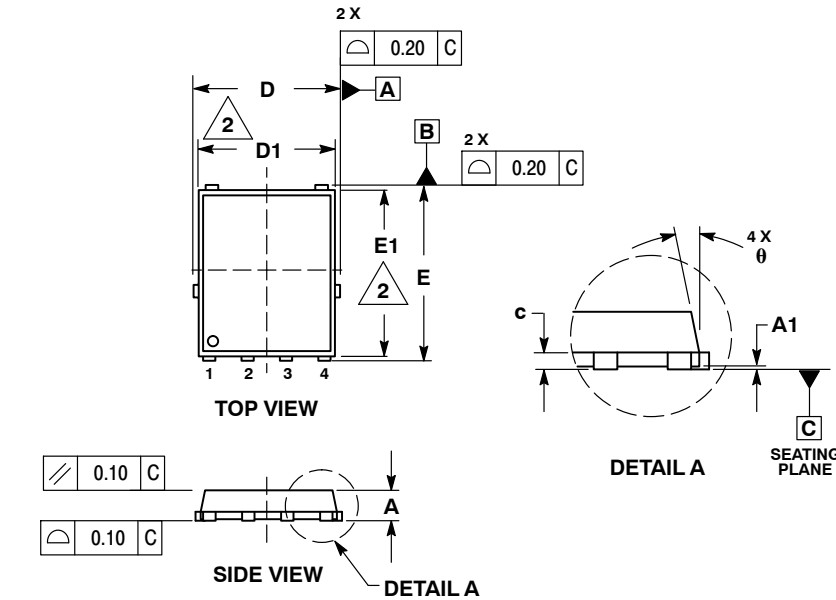
## PACKAGE DIMENSIONS



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

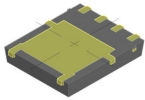
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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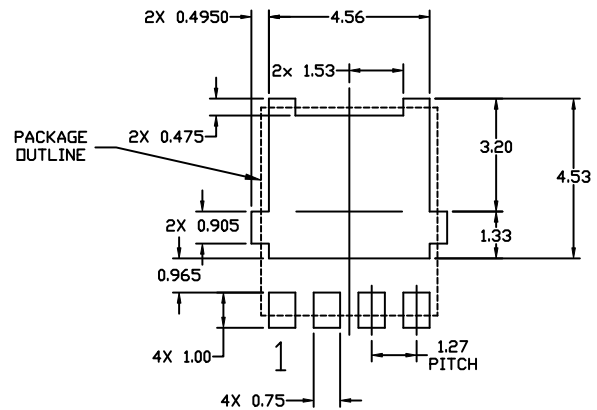
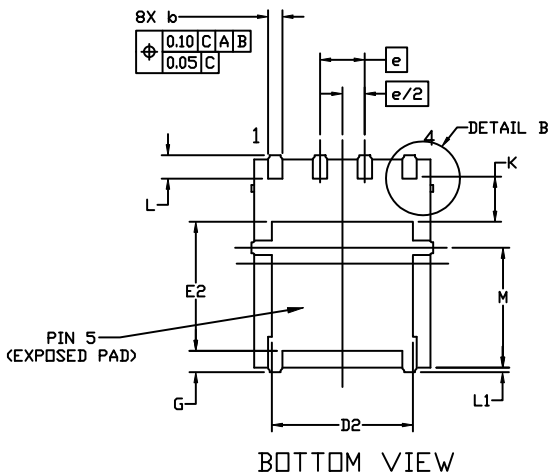
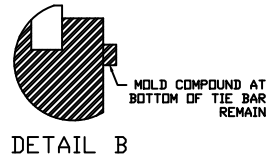
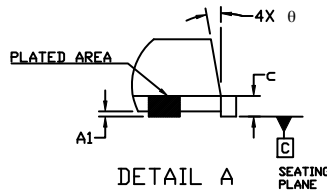
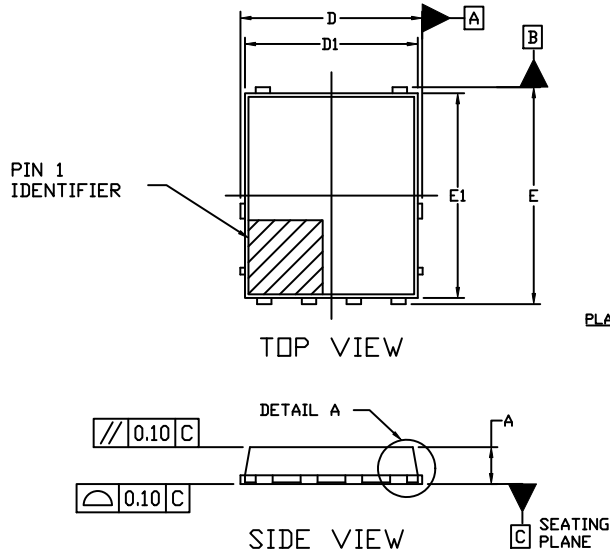
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## DFNW5 5x6 (FULL-CUT SO8FL WF) CASE 507BA ISSUE A

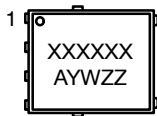
DATE 03 FEB 2021



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
theta	0°	---	12°

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<b>DESCRIPTION:</b>	<b>DFNW5 5x6 (FULL-CUT SO8FL WF)</b>	<b>PAGE 1 OF 1</b>

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