

MOSFET - Single N-Channel

150 V, 4.1 mΩ, 185 A

NVBGS4D1N15MC



ON Semiconductor®

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Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

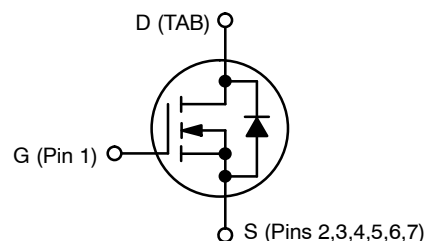
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	150	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	185	A	
Power Dissipation $R_{\theta JC}$ (Note 2)				P_D
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	20	A	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)				P_D
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	2564	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	263	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 81.5 \text{ A}_{pk}, L = 0.1 \text{ mH}$)	E_{AS}	332	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

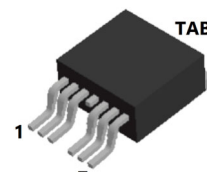
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	4.1 mΩ @ 10 V	185 A
	4.7 mΩ @ 8 V	

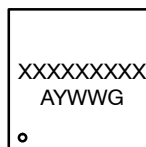


N-CHANNEL MOSFET



D²PAK7
CASE 418AY

MARKING DIAGRAM



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NVBGS4D1N15MC	D ² PAK7 (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.5	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, referenced to 25°C		20.28		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 574\ \mu\text{A}$	2.5	3.5	4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-10.21		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 104\text{ A}$		3.3	4.1	m Ω
		$V_{GS} = 8\text{ V}, I_D = 52\text{ A}$		3.5	4.7	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 90\text{ A}$		10.9		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		1.2		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		7285		pF
Output Capacitance	C_{OSS}			2025		
Reverse Transfer Capacitance	C_{RSS}			10.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 104\text{ A}$		88.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			22.8		
Gate-to-Source Charge	Q_{GS}			37.5		
Gate-to-Drain Charge	Q_{GD}			13.0		
Output Charge	Q_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$		272		nC

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 104\text{ A}, R_G = 6\ \Omega$		49		ns
Rise Time	t_r			38		
Turn-Off Delay Time	$t_{d(OFF)}$			64		
Fall Time	t_f			10		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 104\text{ A}, T_J = 25^\circ\text{C}$		0.88	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 104\text{ A}, T_J = 125^\circ\text{C}$		0.79		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 104\text{ A}, di_S/dt = 100\text{ A}/\mu\text{s}$		89		ns
Charge Time	t_a			47		
Discharge Time	t_b			42		
Reverse Recovery Charge	Q_{RR}			164		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperature

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TYPICAL CHARACTERISTICS

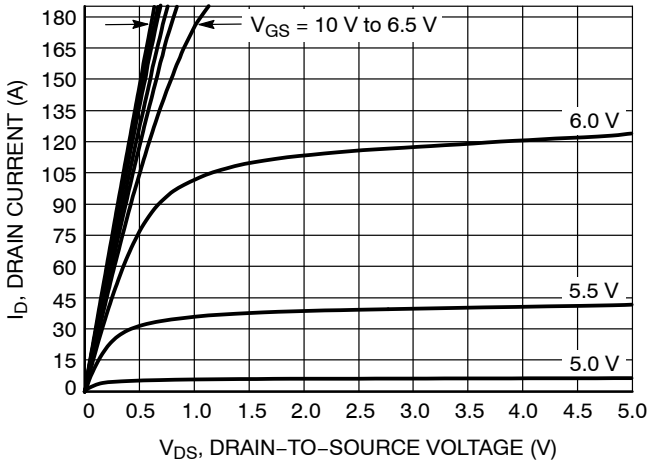


Figure 1. On-Region Characteristics

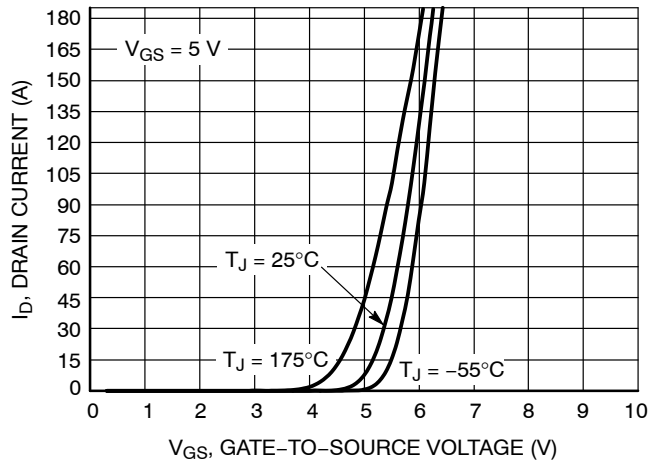


Figure 2. Transfer Characteristics

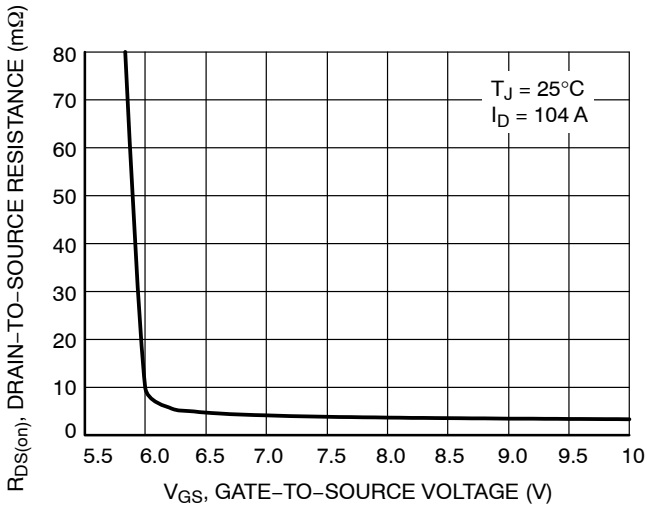


Figure 3. On-Resistance vs. Gate-to-Source Voltage

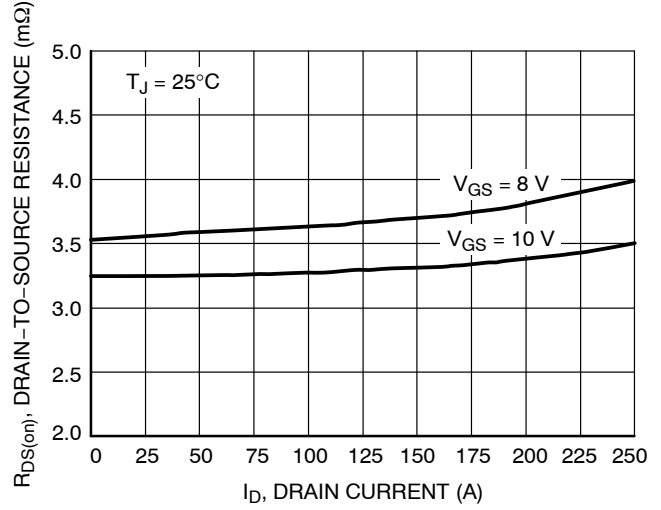


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

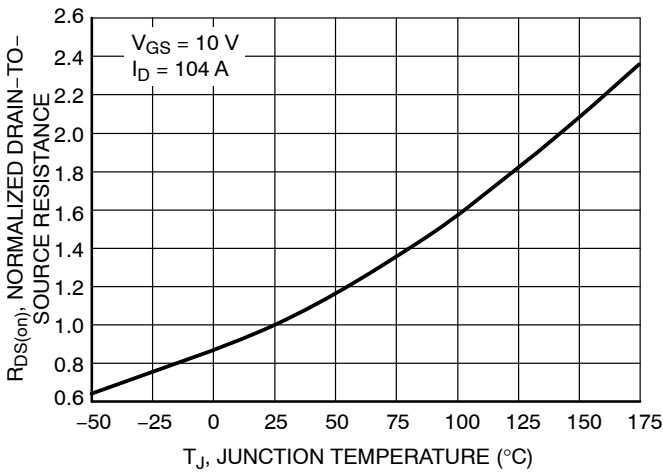


Figure 5. On-Resistance Variation with Temperature

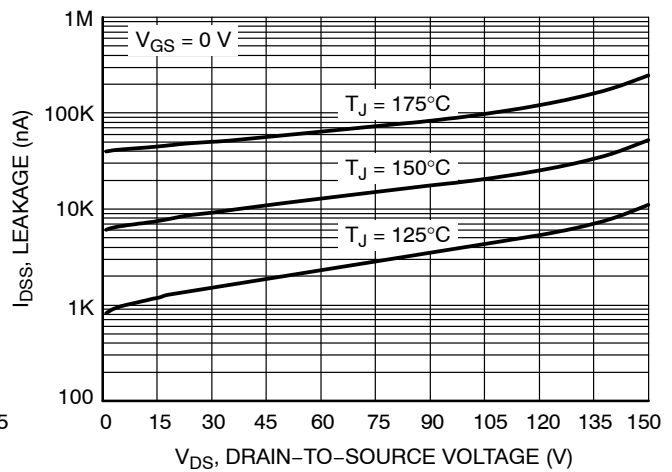


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

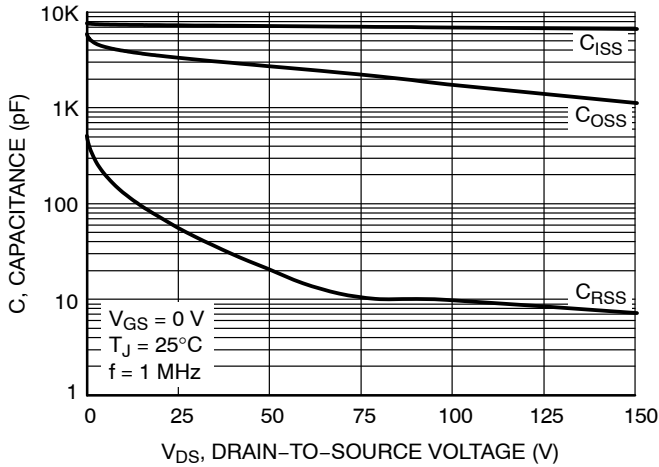


Figure 7. Capacitance Variation

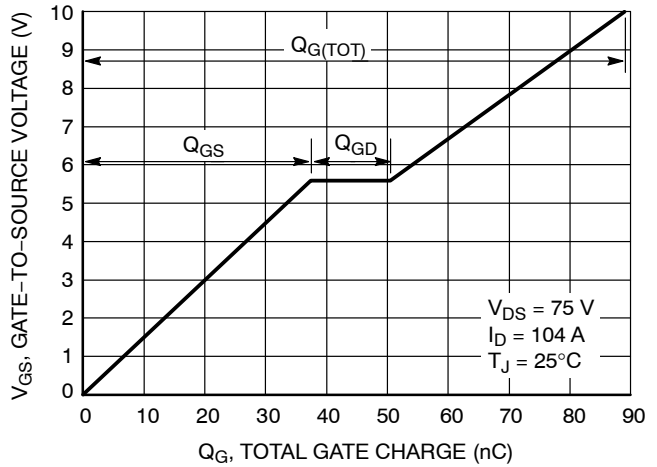


Figure 8. Gate-to-Source Voltage vs. Total Charge

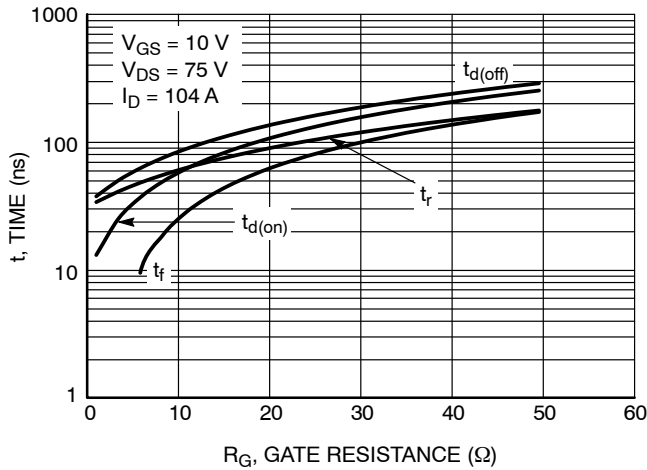


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

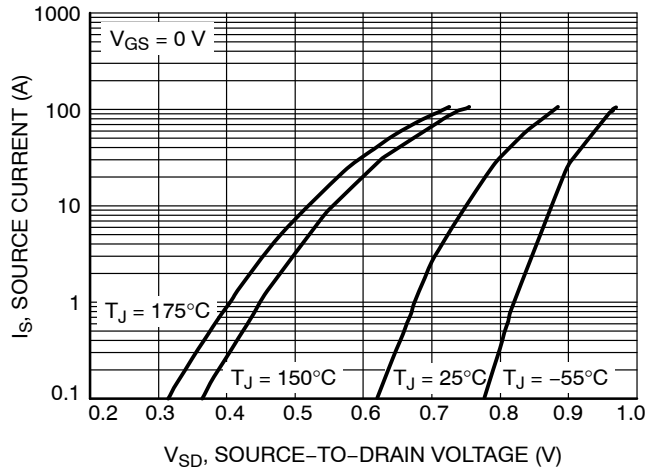


Figure 10. Diode Forward Voltage vs. Current

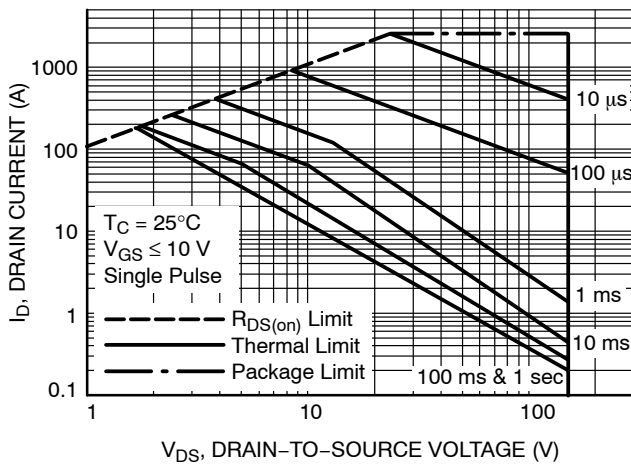


Figure 11. Maximum Rated Forward Biased Safe Operating Area

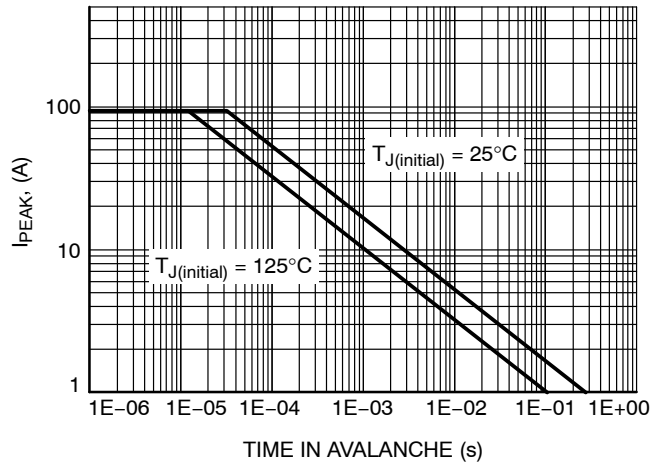


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

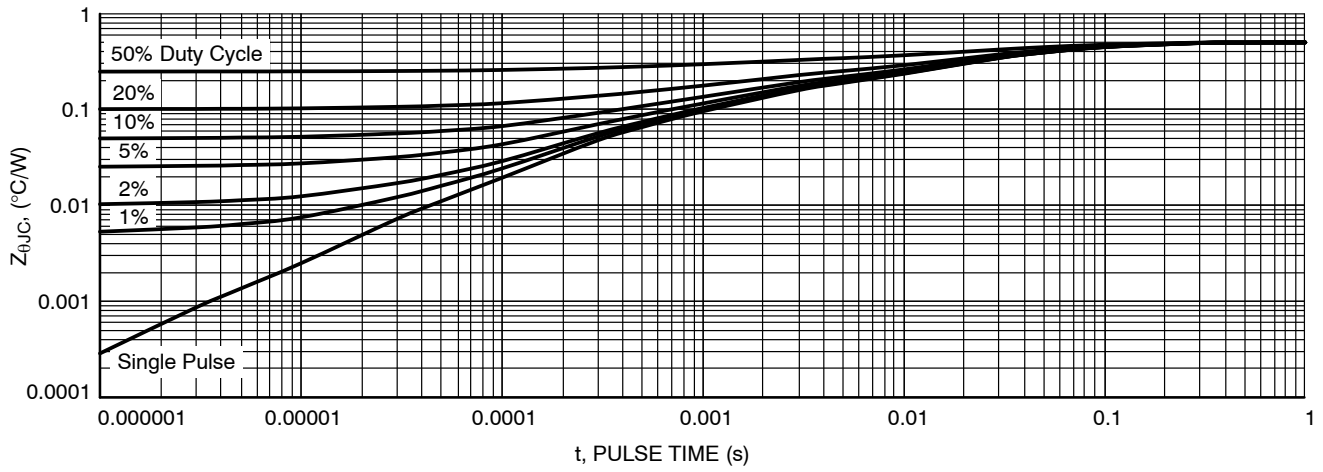


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

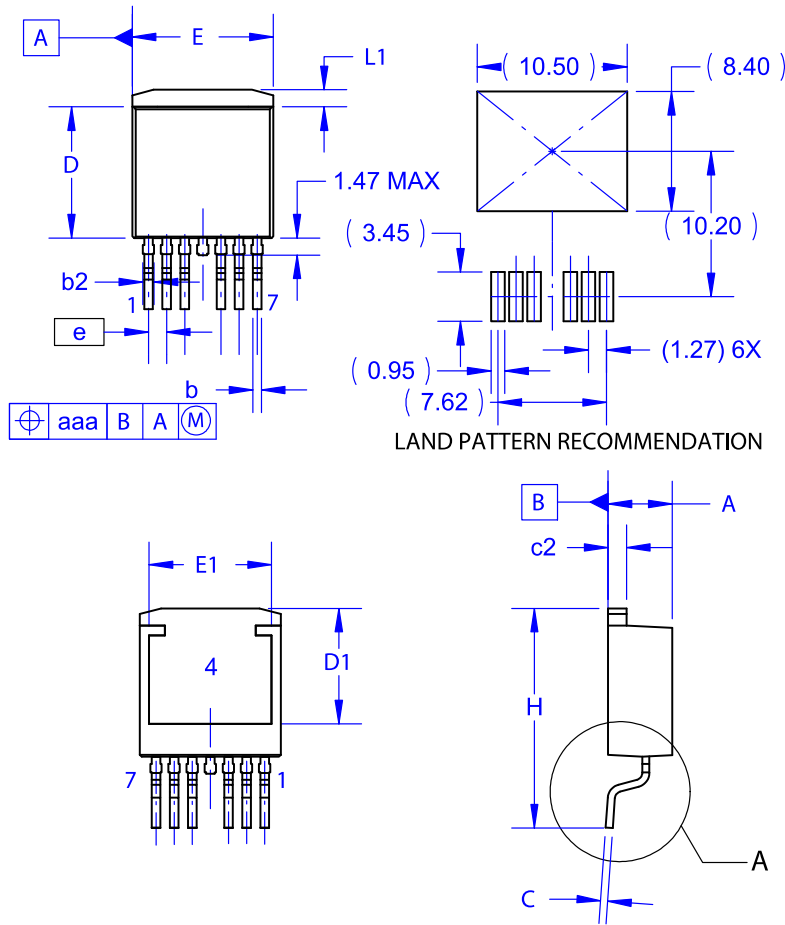
PACKAGE DIMENSIONS

ON Semiconductor®



D2PAK7 (TO-263 7 LD) CASE 418AY ISSUE C

DATE 15 JUL 2019

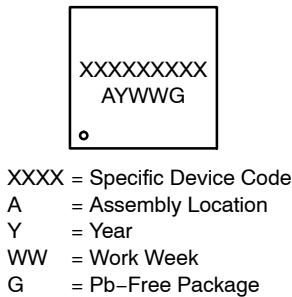


NOTES:

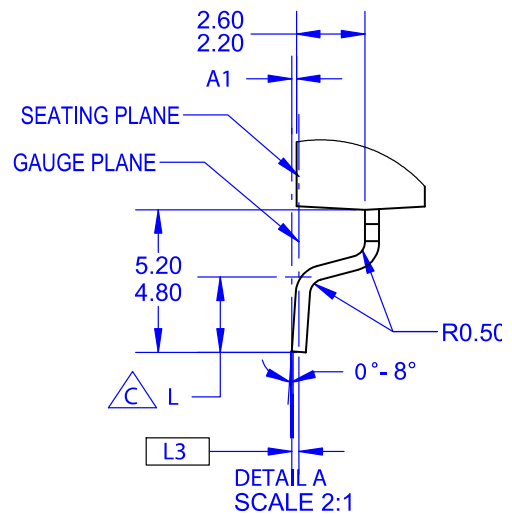
- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC-TO127P1524X465-8N.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.70	0.80	0.90
b	0.50	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	7.70	~	~
E	9.70	9.90	10.20
E1	8.38	8.58	8.78
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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