

NUS5531MT

Main Switch Power MOSFET and Single Charging BJT

-12 V, -6.2 A, Single P-Channel FET with Single PNP low $V_{ce(sat)}$ Transistor, 3x3 mm WDFN Package

This device integrates one high performance power MOSFET and one low $V_{ce(sat)}$ transistor, greatly reducing the layout space and optimizing charging performance in battery-powered portable electronics.

Features

- High Performance Power MOSFET
- Single Low $V_{ce(sat)}$ Transistor as Charging Power Mux
- 3.0x3.0x0.8 mm WDFN Package
- Independent Pin-out Provides Circuit Flexibility
- Low Profile (<0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- Main Switch and Battery Charging Mux for Portable Electronics
- Optimized for Commercial PMUs from Top Suppliers (See Figure 2)

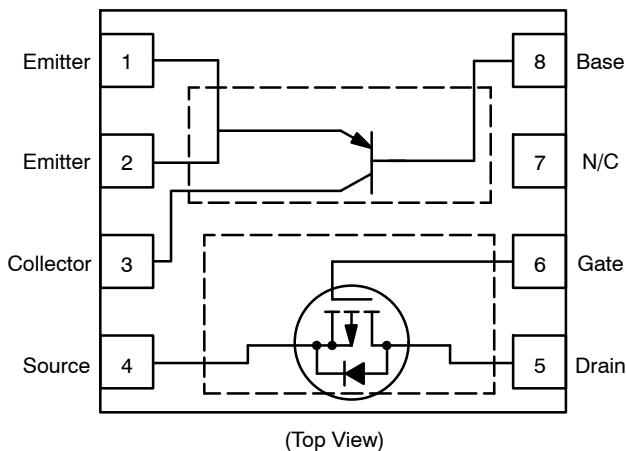


Figure 1. Simple Schematic



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<http://onsemi.com>

MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-12 V	32 mΩ @ -4.5 V	-6.2 A
	44 mΩ @ -2.5 V	

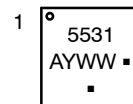
Low $V_{ce(sat)}$ PNP (Wall/USB)

V_{CEO} MAX	V_{EBO} MAX	I_C MAX
-20 V	-7.0 V	-2.0 A



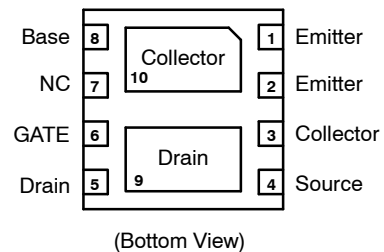
WDFN8
CASE 506BC

MARKING DIAGRAM



5531 = Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NUS5531MTR2G	WDFN8 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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P-Channel Power MOSFET Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		V_{DSS}	-12	V	
Gate-to-Source Voltage		V_{GS}	± 8.0	V	
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-5.47	A
			$T_A = 85^\circ\text{C}$	-4.0	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	-6.2		
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	1.46	W
	$t \leq 10 \text{ s}$			2.1	
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-4.4	A
			$T_A = 85^\circ\text{C}$	-3.2	
Power Dissipation (Note 3)	$T_A = 25^\circ\text{C}$		P_D	0.418	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	-25	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Operating Case Temperature (Note 3)		T_C	-55 to 125	$^\circ\text{C}$	
Source Current (Body Diode) ²		I_S	-2.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	299	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t < 10 \text{ s}$ (Note 3)	$R_{\theta JA}$	81.4	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	85.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t < 10 \text{ s}$ (Note 1)	$R_{\theta JA}$	58.7	$^\circ\text{C}/\text{W}$
Junction-to-Case – $t < 10 \text{ s}$ (Note 3)	ψ_{JC}	26	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 sq in [1 oz] including traces).
- Surface-mounted on FR4 board using 0.5 in sq pad size, 1 oz. Cu.
- Surface-mounted on FR4 board using 50 sq mm pad size, 1 oz. Cu.

P-Channel MOSFET Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-12.0			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250 \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-10.1		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 \text{ V}, V_{DS} = -12 \text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 125^\circ\text{C}$		-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 200	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-0.45	-0.67	-1.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.68		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -3.0 \text{ A}$		32	40	$\text{m}\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -3.0 \text{ A}$		44	50	
Forward Transconductance	g_{FS}	$V_{DS} = -16 \text{ V}, I_D = -3.0 \text{ A}$		5.9		S

- Pulsed Condition: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$

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P-Channel MOSFET Electrical Characteristics (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -12 V		1329		pF
Output Capacitance	C _{OSS}			200		
Reverse Transfer Capacitance	C _{RSS}			116		
Total Gate Charge	Q _{G(tot)}	V _{GS} = -4.5 V, V _{DS} = -12 V, I _D = -3.0 A		13		nC
Threshold Gate Charge	Q _{G(th)}			1.1		
Gate-to-Source Charge	Q _{GS}			1.7		
Gate-to-Drain Charge	Q _{GD}			2.5		

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DD} = -12 V, I _D = -3.0 A, R _G = 3.0		8		ns
Rise Time	t _r			17.5		
Turn-Off Delay Time	t _{d(off)}			80		
Fall Time	t _f			56.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.0 A	T _J = 25°C		-0.66	-1.2	V
			T _J = 125°C		-0.54		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, I _S = -1.0 A		70.8		ns	
Charge Time	t _a			14.3			
Discharge Time	t _b			56.4			
Reverse Recovery Charge	Q _{RR}			44			nC

Single-PNP Transistor Maximum Ratings (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Value	Units
Collector-Emitter Voltage	V _{CEO}	-20	V
Collector-Base Voltage	V _{CB0}	-20	V
Emitter-Base Voltage	V _{EBO}	-7.0	V
Collector Current, Continuous	I _C	-2.0	A
Collector Current, Peak	I _C	-4.0	A
Operating Junction and Storage Temperature	T _J , T _{STG}	-55 to 150	°C
Power Dissipation, T _A = 25°C (Note 5)	P _D	1.58	W
Thermal Resistance (Note 5)	R _{θJA}	61.5	°C/W
Power Dissipation, T _A = 25°C (Note 6)	P _D	0.43	W
Thermal Resistance (Note 6)	R _{θJA}	293	°C/W

5. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 sq in [1 oz] including traces)

6. Surface-mounted on FR4 board using 50 sq mm pad size, 1 oz. Cu.

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Single-PNP Transistor Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	$V_{br_{CEO}}$	$I_C = -10\text{ mA}, I_B = 0$	-20			V
Collector-Base Breakdown Voltage	$V_{br_{CBO}}$	$I_C = -0.1\text{ mA}, I_E = 0$	-20			V
Emitter-Base Breakdown Voltage	$V_{br_{EBO}}$	$I_E = -0.1\text{ mA}, I_C = 0$	-7.0			V
Collector-Emitter Cutoff Current	I_{CES}	$V_{CES} = -15\text{ V}$			-0.1	μA

ON CHARACTERISTICS

DC Current Gain (Note 7)	h_{FE}	$I_C = -1.0\text{ A}, V_{CE} = -2.0\text{ V}$	180			-
DC Current Gain (Note 7)	h_{FE}	$I_C = -2.0\text{ A}, V_{CE} = -2.0\text{ V}$	150			-
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.0\text{ A}, I_B = -0.01\text{ A}$		-0.10	-0.12	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.0\text{ A}, I_B = -0.1\text{ A}$		-0.065	-0.09	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -2.0\text{ A}, I_B = -0.2\text{ A}$		-0.13	-0.18	V
Base-Emitter Saturation Voltage (Note 7)	$V_{BE(sat)}$	$I_C = -1.0\text{ A}, I_B = -0.01\text{ A}$			-0.9	V
Base-Emitter Turn-On Voltage (Note 7)	$V_{BE(on)}$	$I_C = -1.0\text{ A}, I_B = -2.0\text{ A}$			-0.9	V
Cutoff Frequency (Note 8)	f_T	$I_C = -100\text{ mA}, V_{CE} = -5.0\text{ V}$ $f = 100\text{ MHz}$	100			MHz
Input Capacitance (Note 8)	C_{ibo}	$V_{EB} = -0.5\text{ V}, f = 1.0\text{ MHz}$			330	pF
Output Capacitance (Note 8)	C_{obo}	$V_{CB} = -3.0\text{ V}, f = 1.0\text{ MHz}$			100	pF

7. Pulsed Condition: Pulse Width = 300 μsec , Duty Cycle $\leq 2\%$
 8. Guaranteed by design but not tested.

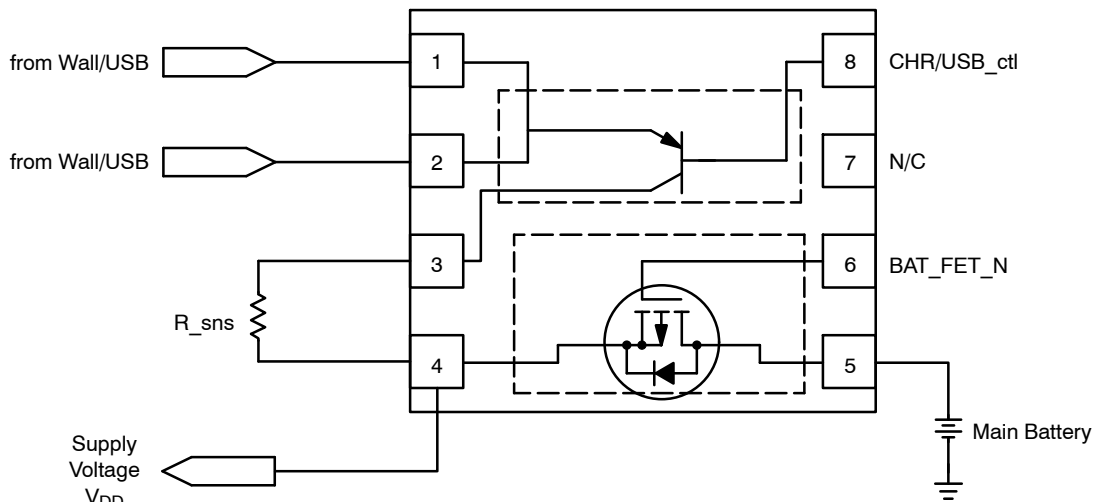


Figure 2. Typical Application Circuit

TYPICAL CHARACTERISTICS - MOSFET

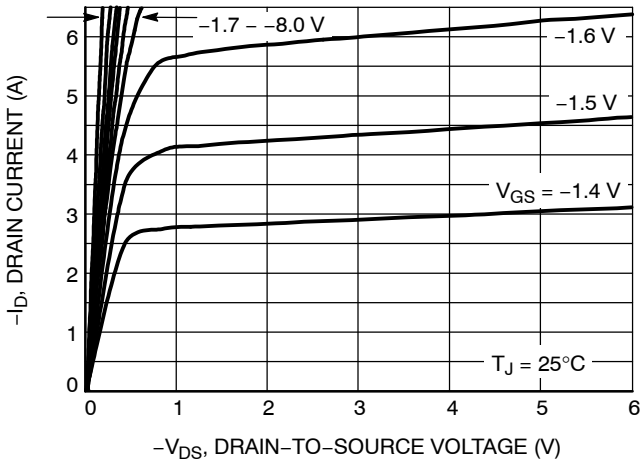


Figure 3. On-Region Characteristics

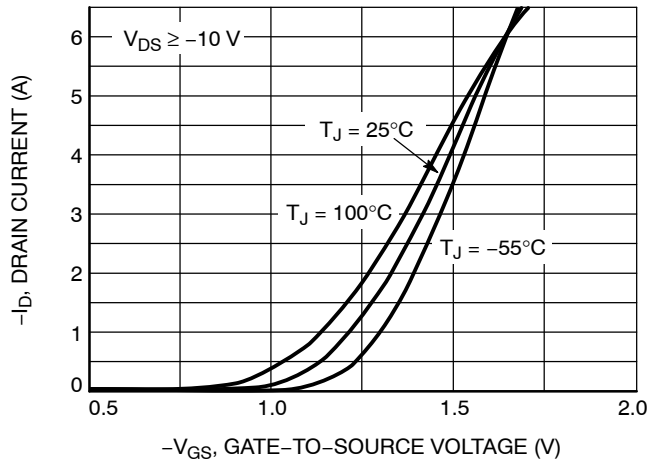


Figure 4. Transfer Characteristics

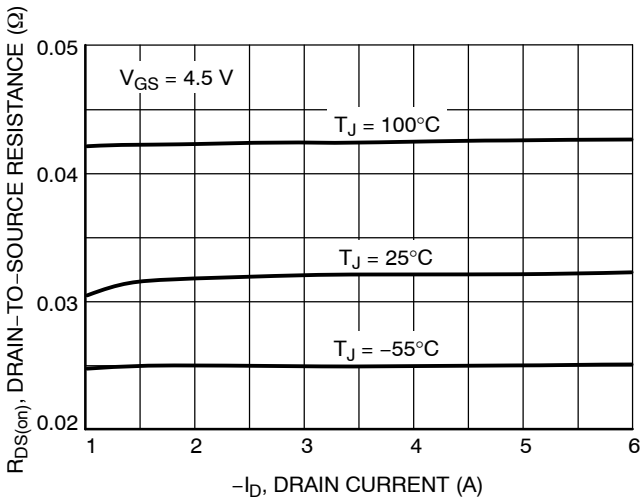


Figure 5. On-Resistance vs. Drain Current

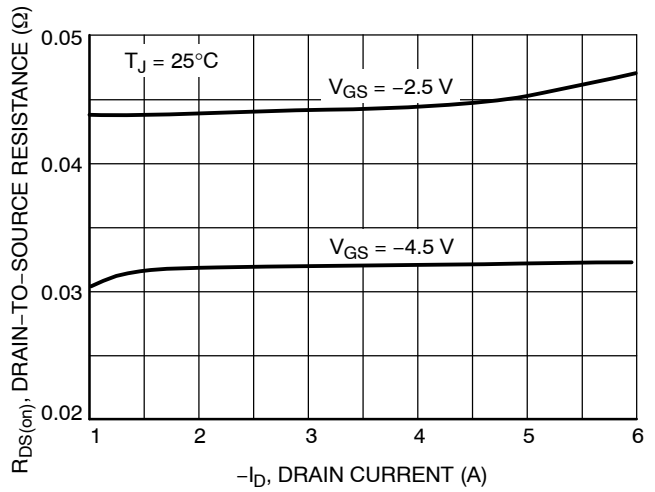


Figure 6. On-Resistance vs. Drain Current and Gate Voltage

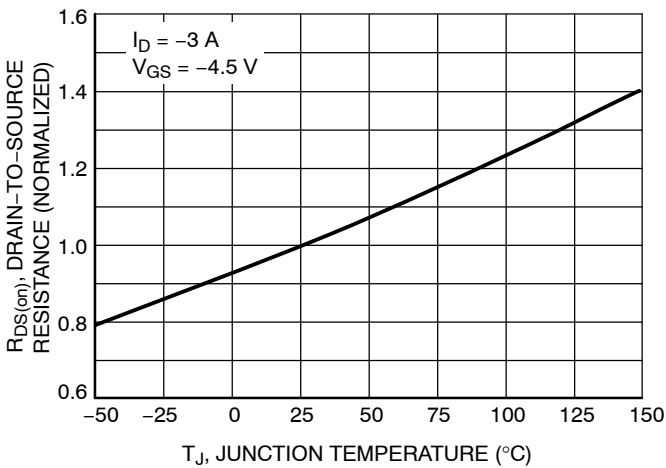


Figure 7. On-Resistance Variation with Temperature

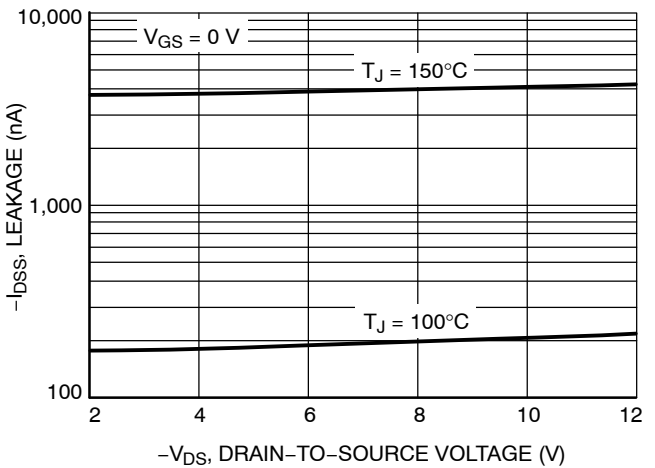


Figure 8. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS - MOSFET

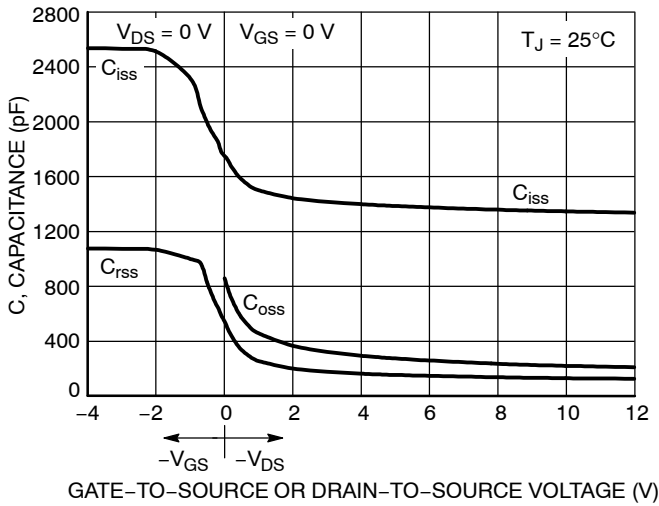


Figure 9. Capacitance Variation

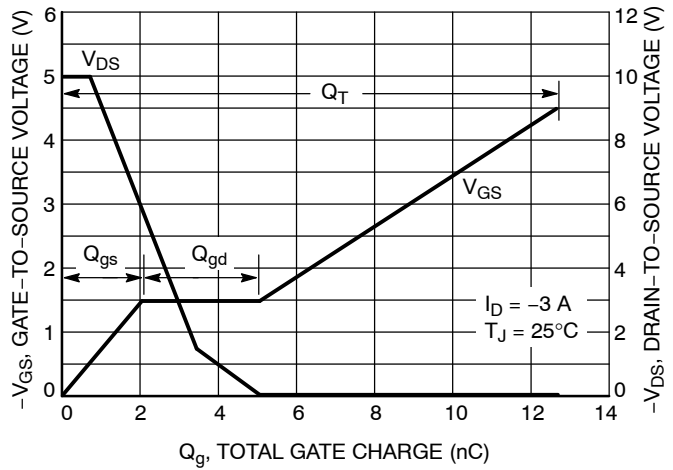


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

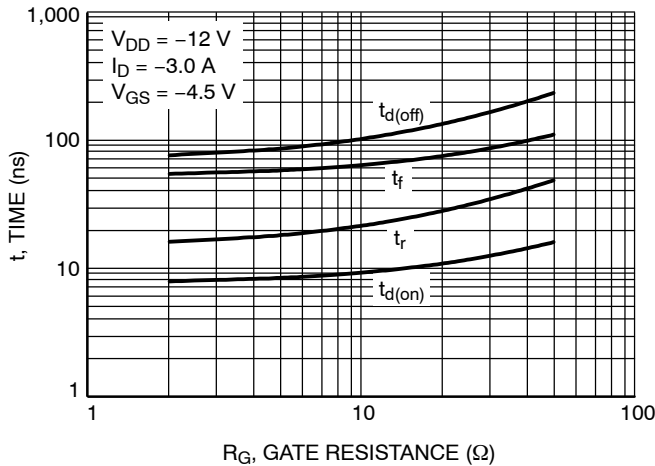


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

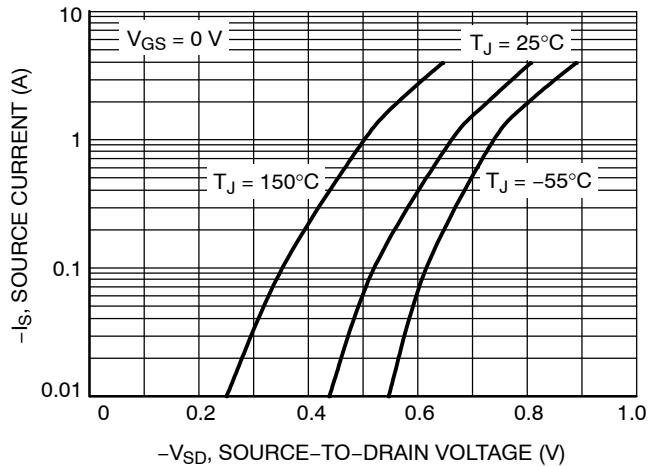
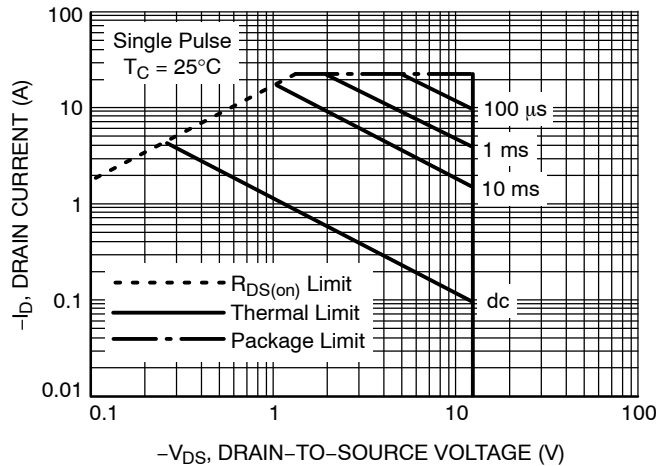


Figure 12. Diode Forward Voltage vs. Current



Mounted on 2" sq. FR4 board (0.5" sq. 2 oz. Cu single sided) with MOSFET die operating.

Figure 13. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS - MOSFET

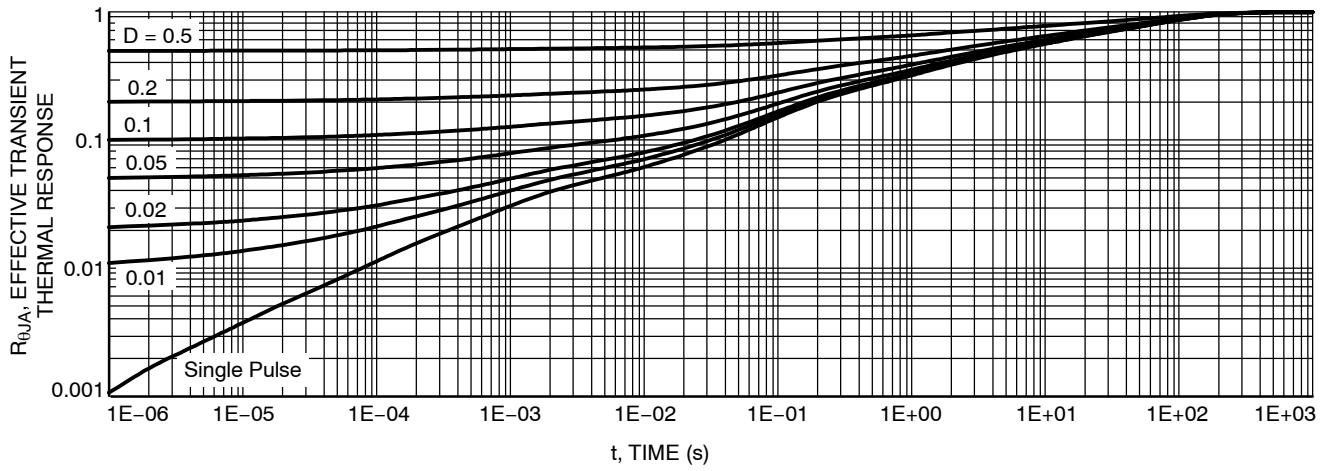


Figure 14. FET Thermal Response

TYPICAL CHARACTERISTICS - BJT

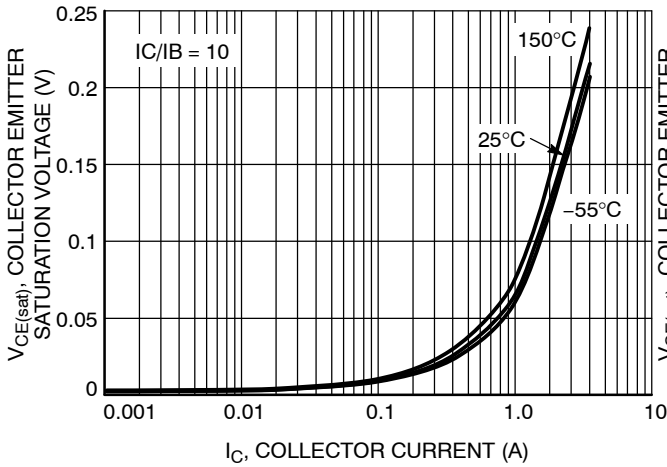


Figure 15. Collector Emitter Saturation Voltage vs. Collector Current

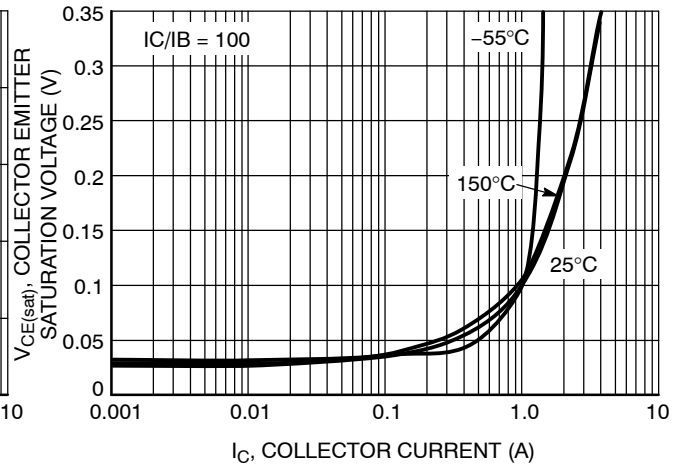


Figure 16. Collector Emitter Saturation Voltage vs. Collector Current

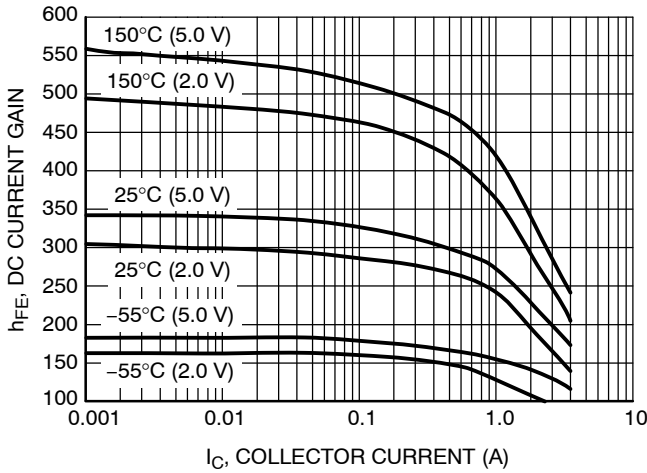


Figure 17. DC Current Gain vs. Collector Current

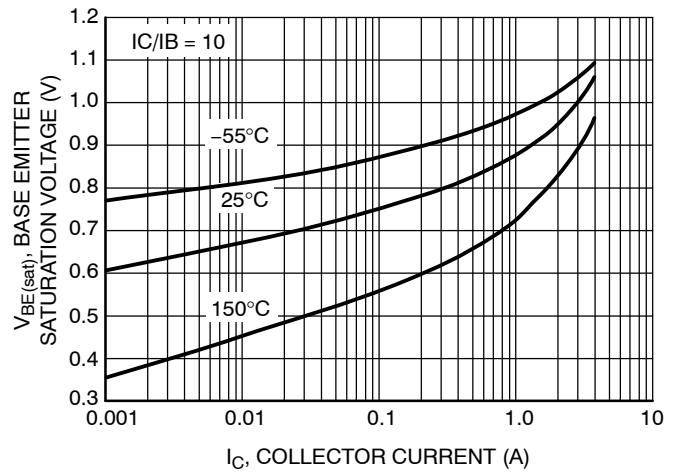


Figure 18. Base Emitter Saturation Voltage vs. Collector Current

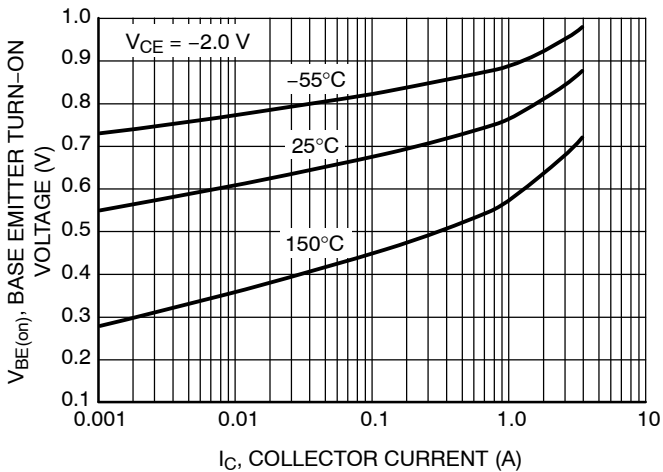


Figure 19. Base Emitter Turn-On Voltage vs. Collector Current

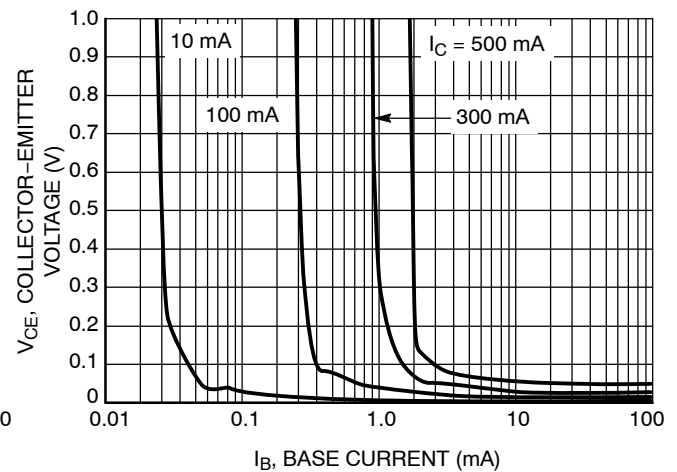


Figure 20. Saturation Region

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TYPICAL CHARACTERISTICS - BJT

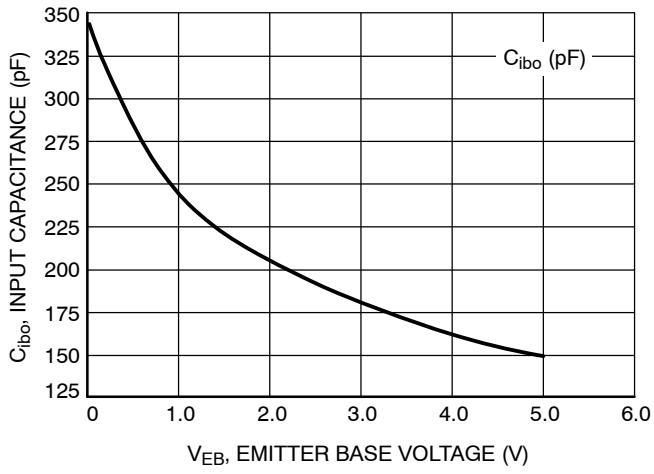


Figure 21. Input Capacitance

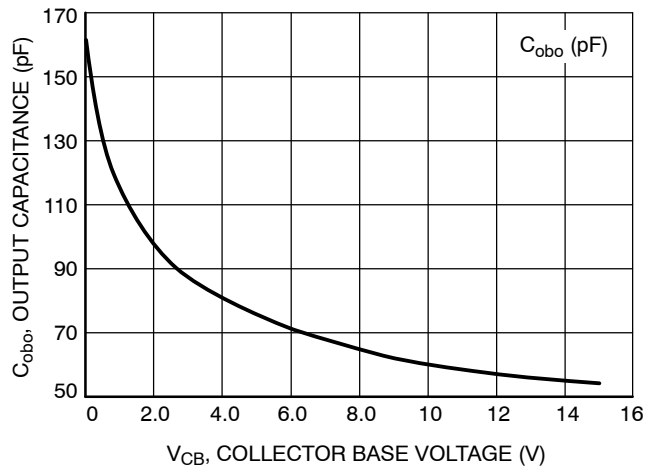


Figure 22. Output Capacitance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

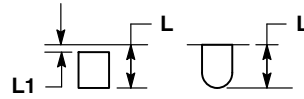
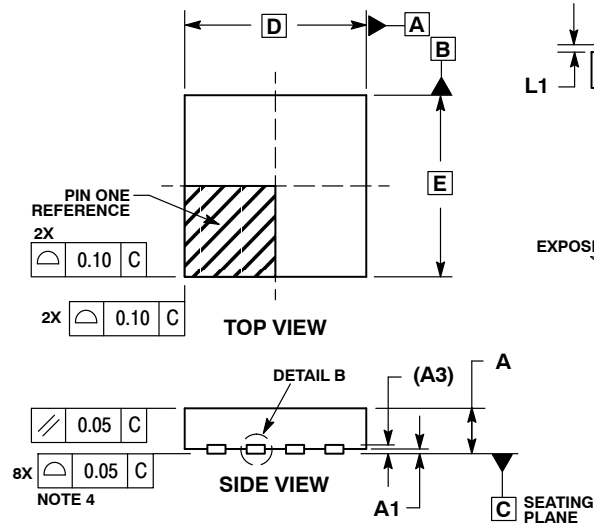
ON Semiconductor®



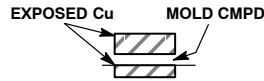
SCALE 2:1

WDFN8, 3x3, 0.65P
CASE 506BC-01
ISSUE A

DATE 28 MAY 2008



DETAIL A
OPTIONAL
CONSTRUCTIONS

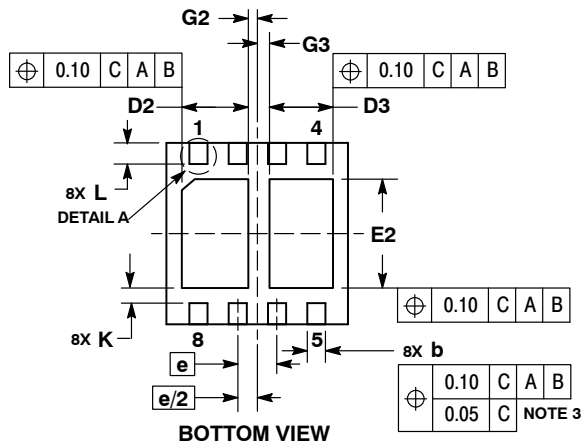


DETAIL B
OPTIONAL
CONSTRUCTIONS

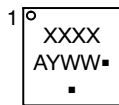
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20	REF
b	0.25	0.35
D	3.00	BSC
D2	1.00	1.20
D3	0.95	1.15
E	3.00	BSC
E2	1.70	1.90
e	0.65	BSC
G2	0.15	BSC
G3	0.20	BSC
K	0.20	---
L	0.25	0.45
L1	---	0.15



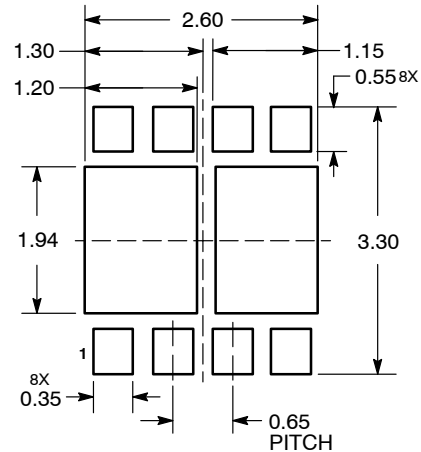
GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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