

# NUP4060AXV6

## ESD Protection Diode Array, 4-Line

This 4-line surge protection array is designed for application requiring transient voltage protection capability. It is intended for use in over-transient voltage and ESD sensitive equipment such as cell phones, portables, computers, printers and other applications. This device features a common cathode design which protects four independent lines in a single SOT-563 package.

### Features

- Protects up to 4 Lines in a Single SOT-563 Package
- ESD Rating: IEC61000-4-2: Level 4  
Contact (8 kV), Air (15 kV)
- $V_{CC}$  Pin = 16 V Protection  
D1, D2, and D3 Pins = 6.8 V Protection
- Low Capacitance (< 7 pF @ 3 V) for D1, D2, and D3
- This is a Pb-Free Device

### Applications

- Hand Held Portable Applications
- USB Interface
- Notebooks, Desktops, Servers
- SIM Card Protection

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Rating	Value	Unit
$P_{PK}$ 1	Peak Power Dissipation	200	W
	$V_{CC}$ Diode 8x20 $\mu\text{sec}$ double exponential waveform, (Note 1) D1, D2, and D3	20	W
$T_J$	Operating Junction Temperature Range	-40 to 125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Lead Solder Temperature – Maximum (10 seconds)	260	$^\circ\text{C}$
ESD	IEC 61000-4-2 Air IEC 61000-4-2 Contact	15000 8000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Nonrepetitive current pulse per Figure 1.

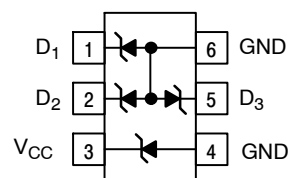


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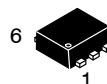
[www.onsemi.com](http://www.onsemi.com)

## SOT-563 4-LINE SURGE PROTECTION

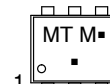
### PIN ASSIGNMENT



### MARKING DIAGRAM



SOT-563  
CASE 463A  
STYLE 6



MT = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NUP4060AXV6T1G	SOT-563 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## NUP4060AXV6

### ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage ( $D_1$ , $D_2$ , and $D_3$ )	(Note 2)	$V_{RWM}$	-	-	5.0	V
Breakdown Voltage ( $D_1$ , $D_2$ , and $D_3$ )	$I_T = 1 \text{ mA}$ , (Note 3)	$V_{BR}$	6.2	6.8	7.2	V
Breakdown Voltage ( $V_{CC}$ )	$I_T = 5 \text{ mA}$ , (Note 3)	$V_{BR2}$	15.3	16	17.1	V
Reverse Leakage Current ( $D_1$ , $D_2$ , and $D_3$ )	$V_{RWM} = 3 \text{ V}$	$I_R$	-	0.01	0.5	$\mu\text{A}$
Reverse Leakage Current ( $V_{CC}$ )	$V_{BR} = 11 \text{ V}$	$I_R$	-	-	0.05	$\mu\text{A}$
Capacitance ( $D_1$ , $D_2$ , and $D_3$ )	$V_R = 3 \text{ V}$ , $f = 1 \text{ MHz}$ (Line to GND)	$C_J$	-	7	10	pF

- Surge protection devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
- $V_{BR}$  is measured at pulse test current  $I_T$ .

# NUP4060AXV6

## TYPICAL ELECTRICAL CHARACTERISTICS

(Diode D<sub>1</sub>, D<sub>2</sub>, and D<sub>3</sub> only)

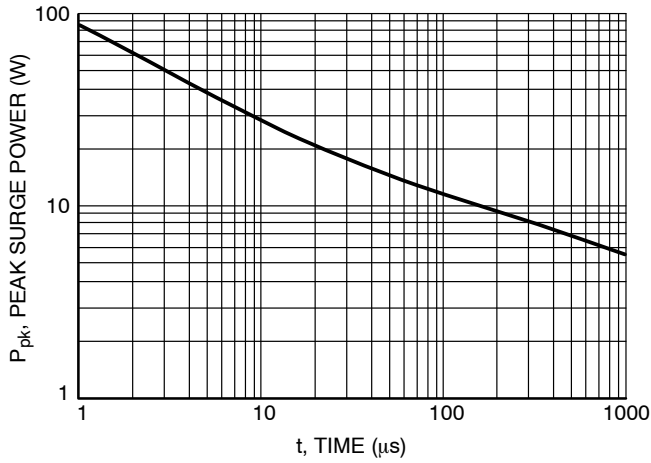


Figure 1. Pulse Width

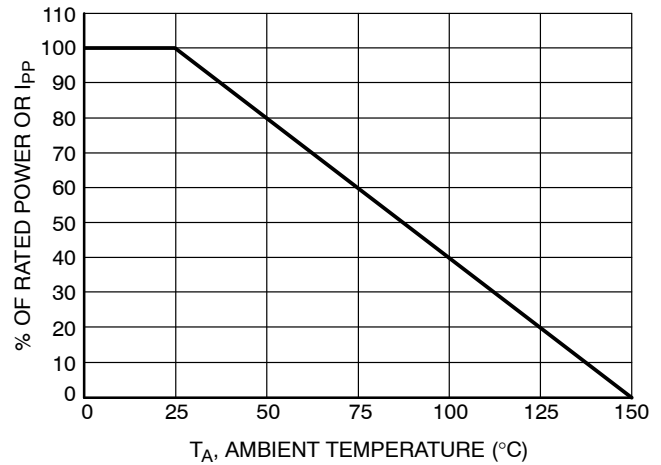


Figure 2. Power Derating Curve

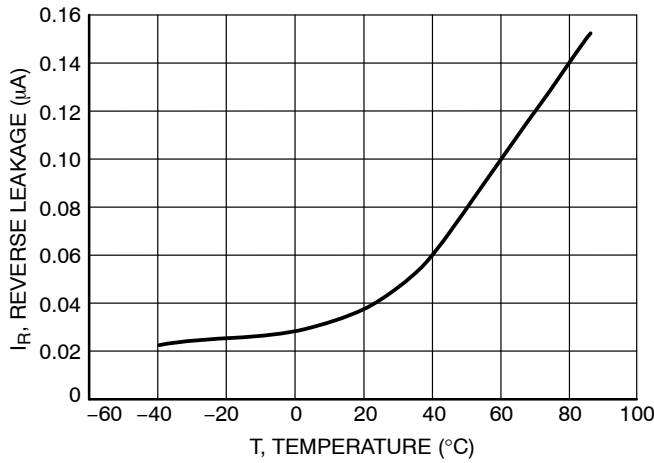


Figure 3. Reverse Leakage versus Temperature

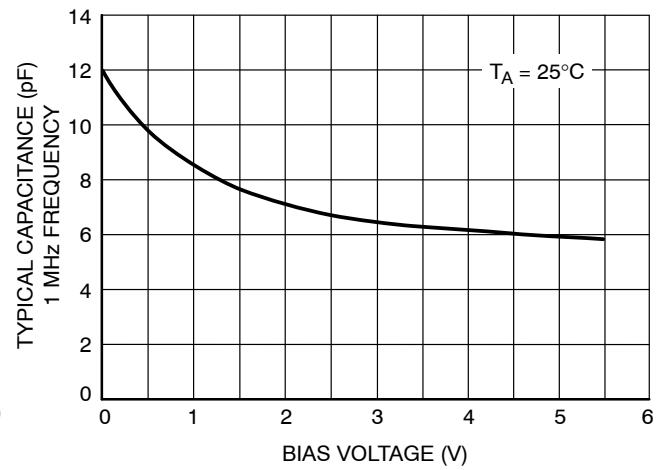


Figure 4. Capacitance

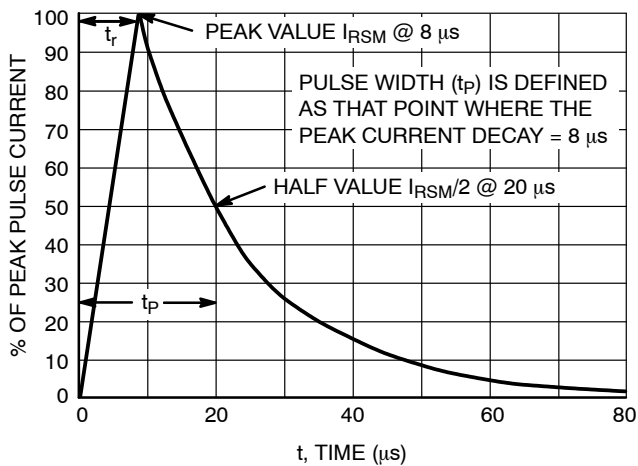


Figure 5. 8 × 20 μs Pulse Waveform

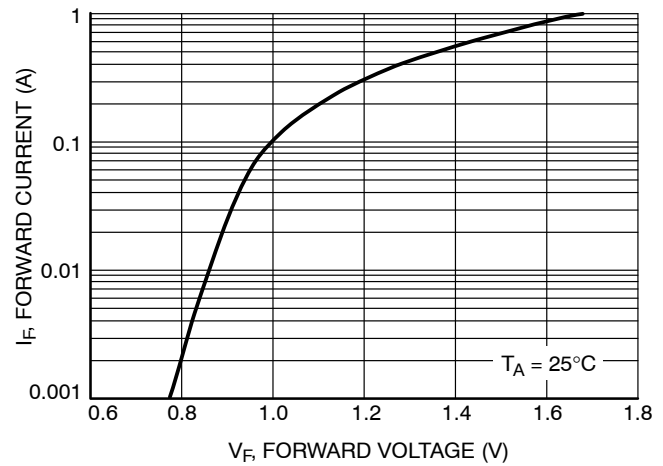
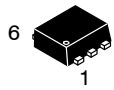


Figure 6. Forward Voltage

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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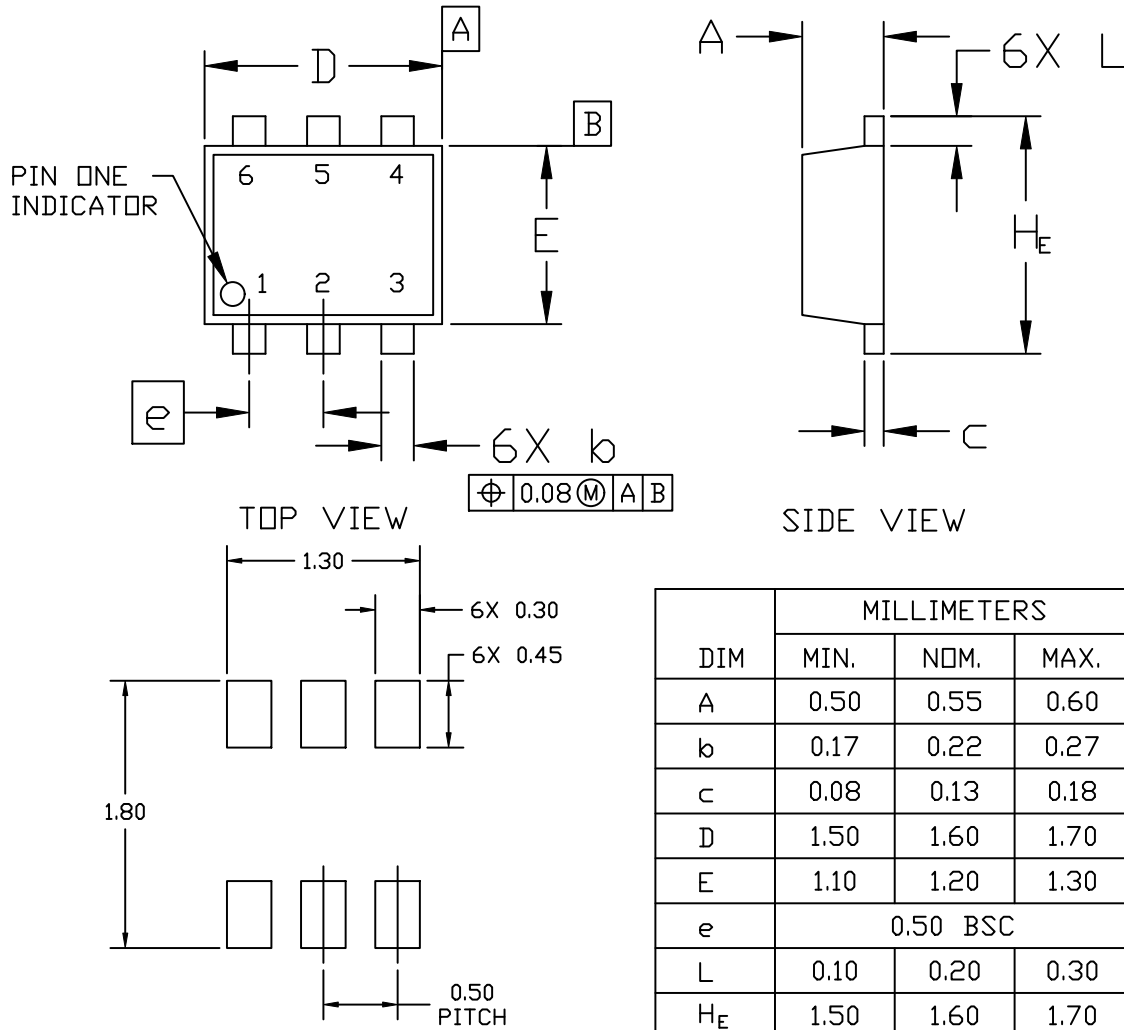
SCALE 4:1

**SOT-563, 6 LEAD**  
CASE 463A  
ISSUE H

DATE 26 JAN 2021

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



**RECOMMENDED MOUNTING FOOTPRINT\***

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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CASE 463A  
ISSUE H

DATE 26 JAN 2021

STYLE 1:  
PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

STYLE 2:  
PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

STYLE 3:  
PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

STYLE 4:  
PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

STYLE 6:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

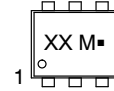
STYLE 8:  
PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

STYLE 9:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

STYLE 10:  
PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

STYLE 11:  
PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2

**GENERIC  
MARKING DIAGRAM\***



XX = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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