

# MOSFET - Power, Single P-Channel, WDFN8 -100 V, 120 mΩ, -13 A



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## NTTFS115P10M5

### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- These Devices are non-ESD Protected
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	-100	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	I <sub>D</sub>	T <sub>C</sub> = 25°C	-13
		T <sub>C</sub> = 100°C	-8.0
Power Dissipation R <sub>θJC</sub> (Note 2)	P <sub>D</sub>	T <sub>C</sub> = 25°C	41
		T <sub>C</sub> = 100°C	16
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2)	I <sub>D</sub>	T <sub>A</sub> = 25°C	-2.0
		T <sub>A</sub> = 100°C	-1.1
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	P <sub>D</sub>	T <sub>A</sub> = 25°C	0.9
		T <sub>A</sub> = 100°C	0.3
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	-137
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)	I <sub>S</sub>	-34	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = -9.1 A)	E <sub>AS</sub>	41	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

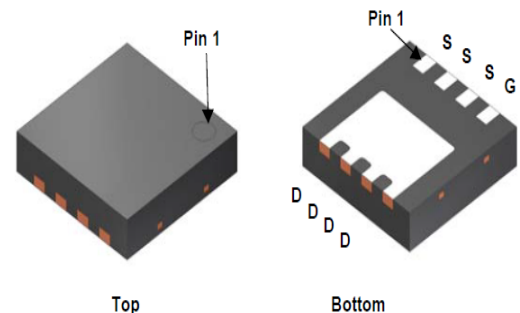
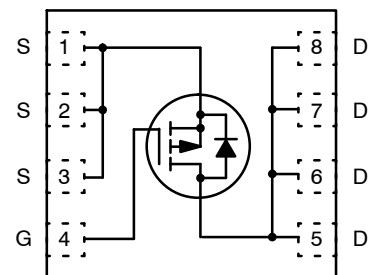
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	R <sub>θJC</sub>	3.0	°C/W
Junction-to-Ambient - Steady State (Note 2)	R <sub>θJA</sub>	134	

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
-100 V	120 mΩ @ -10 V	-13 A
	254 mΩ @ -6 V	



WDFN8  
CASE 511DH

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NTTFS115P10M5

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	-100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-67		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -80\text{ V}$	$T_J = 25^\circ\text{C}$		-1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		-100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -45\ \mu\text{A}$	-2.0	-3.0	-4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		6.2		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -2.4\text{ A}$		97	120	$\text{m}\Omega$
		$V_{GS} = -6\text{ V}, I_D = -1.6\text{ A}$		127	254	
Forward Transconductance	$g_{FS}$	$V_{DS} = -10\text{ V}, I_D = -2.1\text{ A}$		5.5		S
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		3.5		$\Omega$

## CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -50\text{ V}$		637		$\text{pF}$
Output Capacitance	$C_{OSS}$			93.5		
Reverse Transfer Capacitance	$C_{RSS}$			4.5		
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = -6\text{ V}, V_{DS} = -50\text{ V}, I_D = -2.4\text{ A}$		5.7		$\text{nC}$
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = -10\text{ V}, V_{DS} = -50\text{ V}, I_D = -2.4\text{ A}$		9.2		
Gate-to-Source Charge	$Q_{GS}$			3.0		
Gate-to-Drain Charge	$Q_{GD}$			1.3		
Plateau Voltage	$V_{GP}$			4.4		

## SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DS} = -50\text{ V}, I_D = -2.4\text{ A}, R_G = 2.5\ \Omega$		8.7		ns
Rise Time	$t_r$			2.1		
Turn-Off Delay Time	$t_{d(OFF)}$			13.4		
Fall Time	$t_f$			4.1		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = -2.4\text{ A}$	$T_J = 25^\circ\text{C}$		0.84	1.2	V
			$T_J = 125^\circ\text{C}$		0.71		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, \text{d}I_S/\text{d}t = 300\text{ A}/\mu\text{s}, I_S = -1.2\text{ A}$		28.7		ns	
Reverse Recovery Charge	$Q_{RR}$			87.6		nC	
Charge Time	$t_a$			18.4		ns	
Discharge Charge	$t_b$			10.4		ns	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

4. Pulse Test: Pulse Width < 300  $\mu\text{s}$ . Duty Cycle < 2%.

5. Maximum current for pulses as long as 1s is higher but is independent on pulse duration or duty cycles.

TYPICAL CHARACTERISTICS

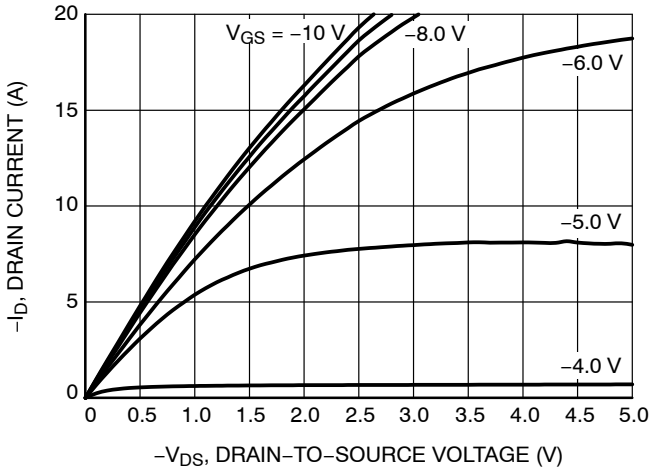


Figure 1. On-Region Characteristics

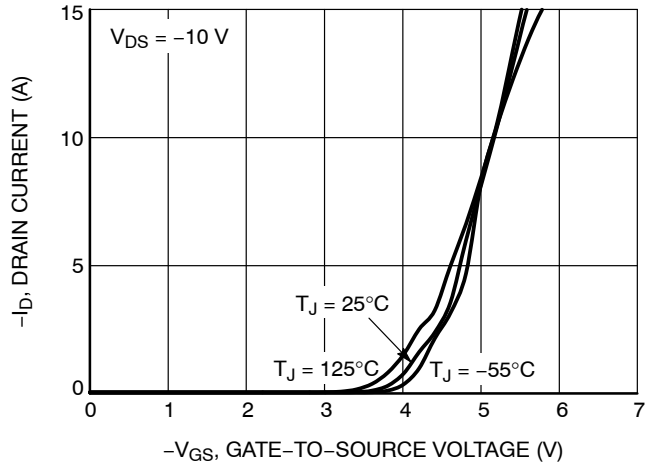


Figure 2. Transfer Characteristics

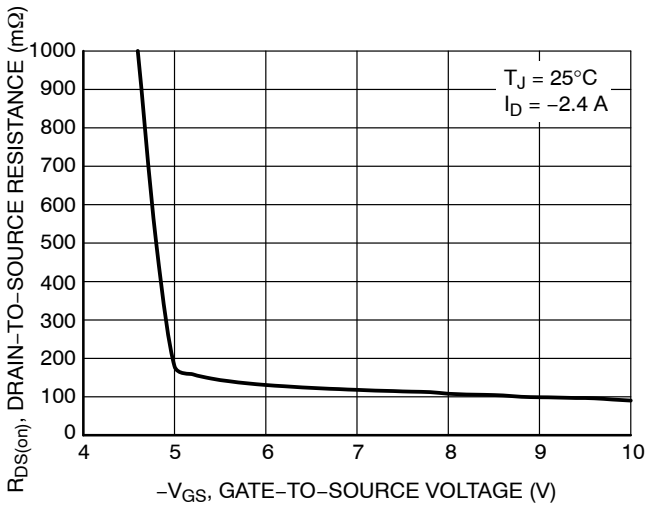


Figure 3. On-Resistance vs. Gate-to-Source Voltage

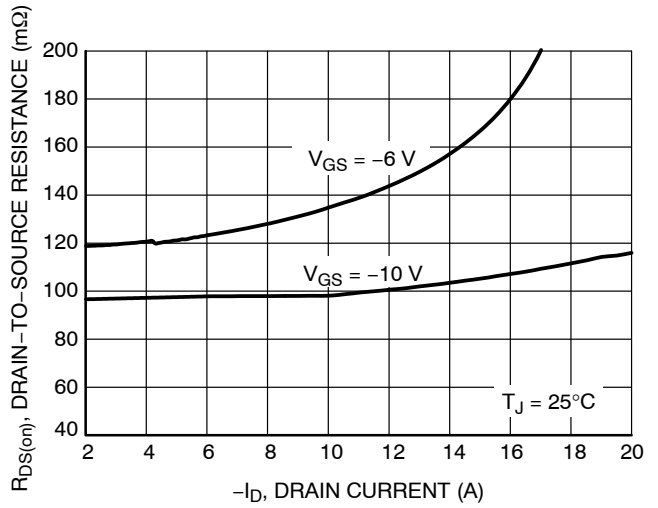


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

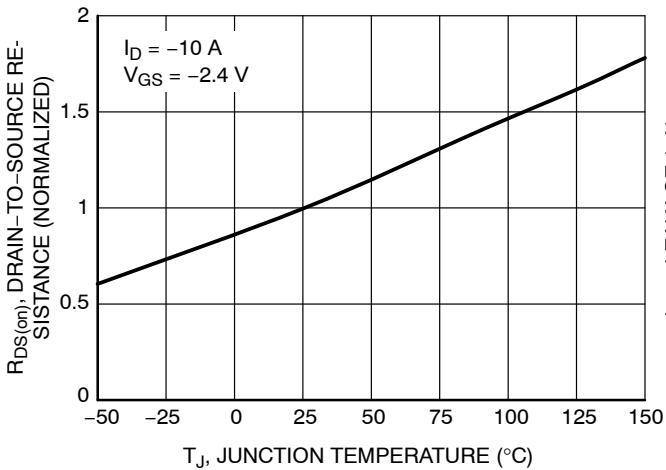


Figure 5. On-Resistance Variation with Temperature

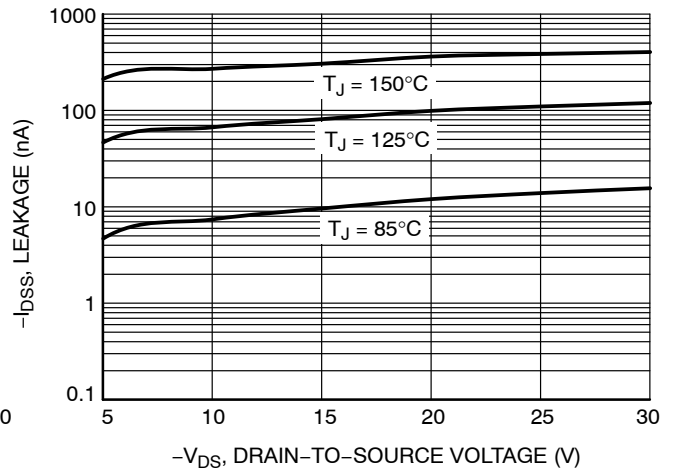


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTTFS115P10M5

## TYPICAL CHARACTERISTICS

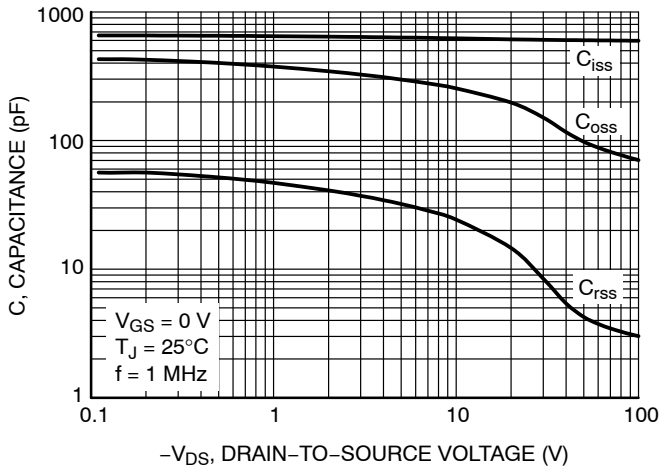


Figure 7. Capacitance Variation

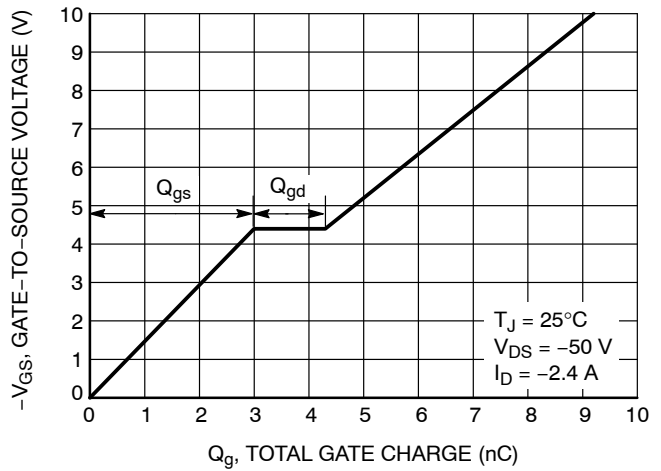


Figure 8. Gate-to-Source vs. Total Charge

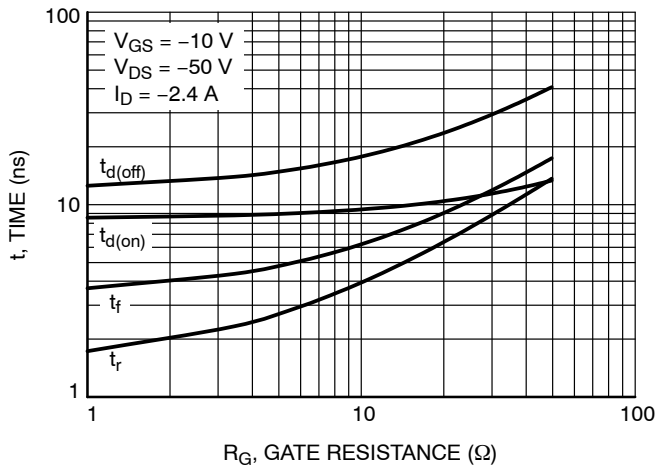


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

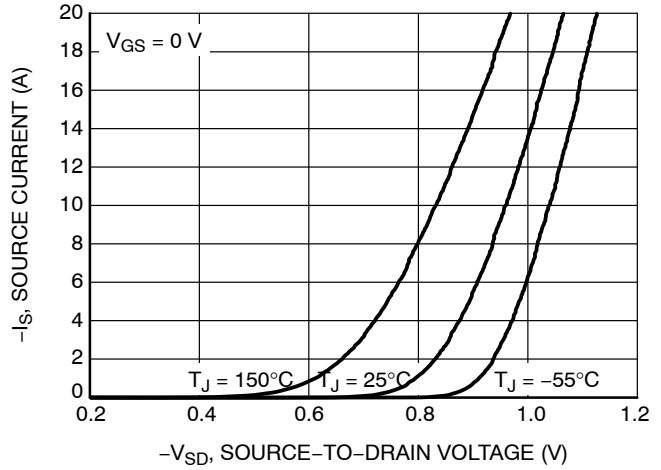


Figure 10. Diode Forward Voltage vs. Current

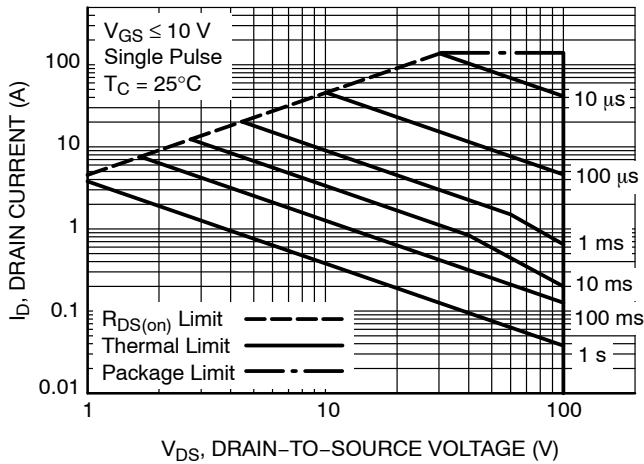


Figure 11. Maximum Rated Forward Biased Safe Operating Area

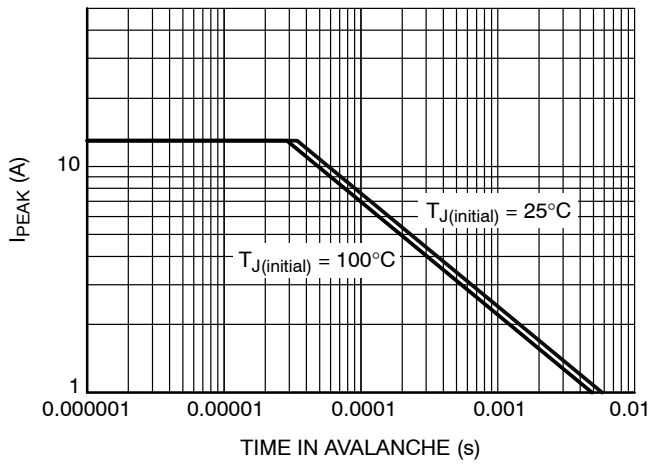


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NTTFS115P10M5

## TYPICAL CHARACTERISTICS

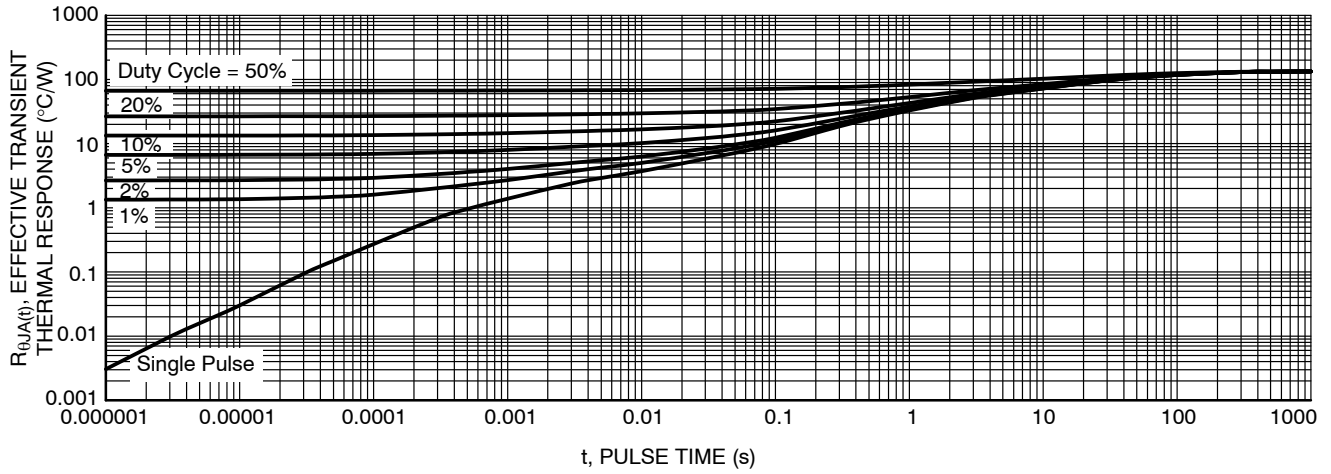


Figure 13. Thermal Response

### DEVICE ORDERING AND MARKING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
NTTFS115P10M5	115P10M5	WDFN8 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

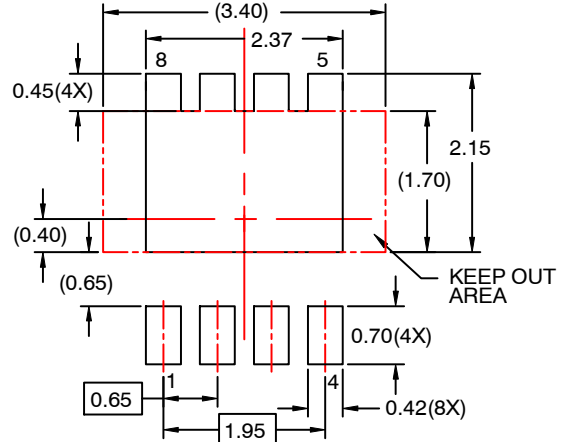
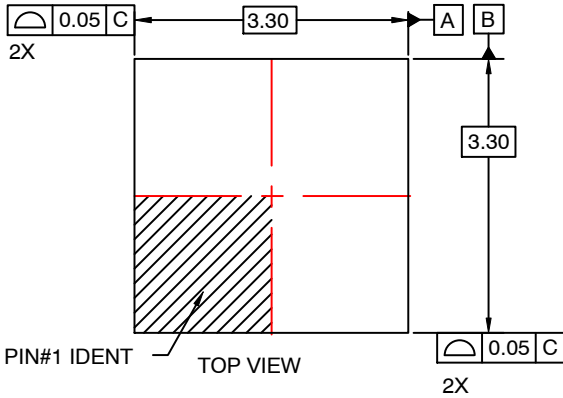
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

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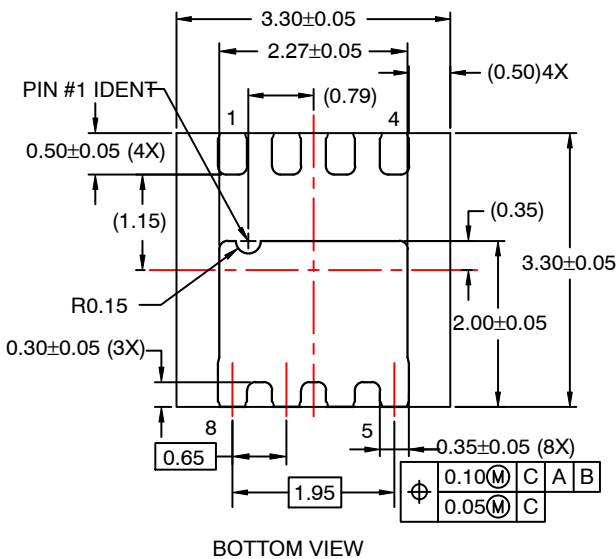
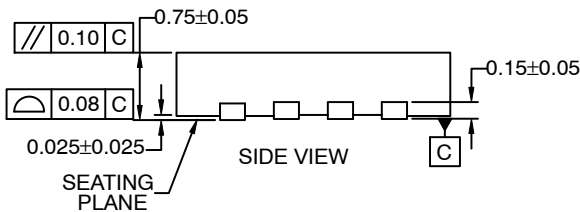


**WDFN8 3.3x3.3, 0.65P**  
 CASE 511DH  
 ISSUE O

DATE 31 JUL 2016



RECOMMENDED LAND PATTERN



NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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