

# NTR5198NL

## MOSFET – Power, Single, N-Channel, Logic Level, SOT-23

60 V, 155 mΩ



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### Features

- Small Footprint Industry Standard Surface Mount SOT–23 Package
- Low  $R_{DS(on)}$  for Low Conduction Losses and Improved Efficiency
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

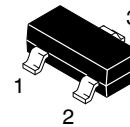
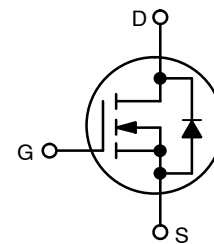
| Parameter   | Symbol   | Value                     | Unit             |   |
|---|--|---------------------------|------------------|---|
| Drain-to-Source Voltage   | $V_{DSS}$  | 60                        | V                |   |
| Gate-to-Source Voltage  | $V_{GS}$   | $\pm 20$                  | V                |   |
| Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, and 4)   | Steady State   | $T_A = 25^\circ\text{C}$  | $I_D$ 2.2        | A |
|   |  | $T_A = 100^\circ\text{C}$ | 1.6              |   |
| Power Dissipation $R_{\Psi J-mb}$ (Notes 1 and 3)                 | Steady State   | $T_A = 25^\circ\text{C}$  | $P_D$ 1.5        | W |
|   |  | $T_A = 100^\circ\text{C}$ | 0.6              |   |
| Continuous Drain Current $R_{\theta JA}$ (Note 1, 2, 3, and 4)    | Steady State   | $T_A = 25^\circ\text{C}$  | $I_D$ 1.7        | A |
|   |  | $T_A = 100^\circ\text{C}$ | 1.2              |   |
| Power Dissipation $R_{\theta JA}$ (Notes 1 and 3)                 | Steady State   | $T_A = 25^\circ\text{C}$  | $P_D$ 0.9        | W |
|   |  | $T_A = 100^\circ\text{C}$ | 0.4              |   |
| Pulsed Drain Current  | $T_A = 25^\circ\text{C}$ ,<br>$t_p = 10 \mu\text{s}$ | $I_{DM}$ 27               | A                |   |
| Operating Junction and Storage Temperature                        | $T_J$ ,<br>$T_{stg}$                                 | -55 to 150                | $^\circ\text{C}$ |   |
| Source Current (Body Diode)                                       | $I_S$  | 1.9                       | A                |   |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | $T_L$  | 260                       | $^\circ\text{C}$ |   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

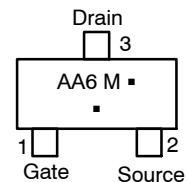
| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---------------|------------------|-----------|
| 60 V          | 155 mΩ @ 10 V    | 2.2 A     |
|               | 205 mΩ @ 4.5 V   |           |

### N-Channel



SOT-23  
CASE 318  
STYLE 21

### MARKING DIAGRAM/ PIN ASSIGNMENT



AA6 = Device Code  
M = Date Code\*  
▪ = Pb–Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

| Device       | Package             | Shipping†              |
|--------------|---------------------|------------------------|
| NTR5198NLT1G | SOT–23<br>(Pb–Free) | 3000 /<br>Tape & Reel  |
| NTR5198NLT3G | SOT–23<br>(Pb–Free) | 10000 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTR5198NL

## THERMAL RESISTANCE RATINGS

| Parameter                                   | Symbol          | Max | Unit |
|---|-----------------|-----|------|
| Junction-to-Lead #3 – Drain (Notes 2 and 3) | $R_{\Psi J-mb}$ | 86  | °C/W |
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 139 | °C/W |

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter   | Symbol            | Test Conditions  | Min                       | Typ | Max       | Unit          |
|---|-------------------|--|---------------------------|-----|-----------|---------------|
| <b>OFF CHARACTERISTICS</b>                                |                   |  |                           |     |           |               |
| Drain-to-Source Breakdown Voltage                         | $V_{(BR)DSS}$     | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$              | 60                        |     |           | V             |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | Reference to $25^\circ\text{C}$ , $I_D = 250\ \mu\text{A}$ |                           | 70  |           | mV/°C         |
| Zero Gate Voltage Drain Current                           | $I_{DSS}$         | $V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$                | $T_J = 25^\circ\text{C}$  |     | 1.0       | $\mu\text{A}$ |
|   |                   |  | $T_J = 125^\circ\text{C}$ |     | 10        |               |
| Gate-to-Source Leakage Current                            | $I_{GSS}$         | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$            |                           |     | $\pm 100$ | nA            |

## ON CHARACTERISTICS (Note 5)

|                                   |                  |  |     |      |     |            |
|-----------------------------------|------------------|--|-----|------|-----|------------|
| Gate Threshold Voltage            | $V_{GS(TH)}$     | $V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$                  | 1.5 |      | 2.5 | V          |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | Reference to $25^\circ\text{C}$ , $I_D = 250\ \mu\text{A}$ |     | -6.5 |     | mV/°C      |
| Drain-to-Source On-Resistance     | $R_{DS(on)}$     | $V_{GS} = 10\text{ V}, I_D = 1\text{ A}$                   |     | 107  | 155 | m $\Omega$ |
|                                   |                  | $V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}$                  |     | 142  | 205 |            |
| Forward Transconductance          | $g_{FS}$         | $V_{DS} = 5.0\text{ V}, I_D = 1\text{ A}$                  |     | 3    |     | S          |

## CHARGES, CAPACITANCES & GATE RESISTANCE

|                              |              |   |                         |     |     |    |
|------------------------------|--------------|---|-------------------------|-----|-----|----|
| Input Capacitance            | $C_{iss}$    | $V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$ |                         | 182 |     | pF |
| Output Capacitance           | $C_{oss}$    |   |                         | 25  |     |    |
| Reverse Transfer Capacitance | $C_{rss}$    |   |                         | 16  |     |    |
| Total Gate Charge            | $Q_{G(TOT)}$ | $V_{DS} = 48\text{ V}, I_D = 1\text{ A}$                        | $V_{GS} = 4.5\text{ V}$ |     | 2.8 | nC |
|                              |              |   | $V_{GS} = 10\text{ V}$  |     | 5.1 |    |
| Threshold Gate Charge        | $Q_{G(TH)}$  | $V_{DS} = 48\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}$  |                         |     | 0.3 | V  |
| Gate-to-Source Charge        | $Q_{GS}$     |   |                         |     | 0.8 |    |
| Gate-to-Drain Charge         | $Q_{GD}$     |   |                         |     | 1.5 |    |
| Plateau Voltage              | $V_{GP}$     |   |                         |     | 3.1 |    |
| Gate Resistance              | $R_G$        |   |                         |     | 8   |    |

## SWITCHING CHARACTERISTICS (Note 6)

|                     |              |  |  |    |  |    |
|---------------------|--------------|--|--|----|--|----|
| Turn-On Delay Time  | $t_{d(on)}$  | $V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 1\text{ A}, R_G = 10\ \Omega$ |  | 5  |  | ns |
| Rise Time           | $t_r$        |  |  | 7  |  |    |
| Turn-Off Delay Time | $t_{d(off)}$ |  |  | 13 |  |    |
| Fall Time           | $t_f$        |  |  | 2  |  |    |

## DRAIN-SOURCE DIODE CHARACTERISTICS

|                                |          |   |                           |  |     |     |    |
|--------------------------------|----------|---|---------------------------|--|-----|-----|----|
| Forward Diode Voltage          | $V_{SD}$ | $V_{GS} = 0\text{ V}, I_S = 1\text{ A}$   | $T_J = 25^\circ\text{C}$  |  | 0.8 | 1.2 | V  |
|                                |          |   | $T_J = 125^\circ\text{C}$ |  | 0.6 |     |    |
| Reverse Recovery Time          | $t_{rr}$ | $I_S = 1\text{ A}_{dc}, V_{GS} = 0\text{ V}_{dc}, dI_S/dt = 100\text{ A}/\mu\text{s}$ |                           |  | 12  |     | ns |
| Charge Time                    | $t_a$    |   |                           |  | 9   |     |    |
| Discharge Time                 | $t_b$    |   |                           |  | 3   |     |    |
| Reverse Recovery Stored Charge | $Q_{RR}$ |   |                           |  | 6   |     |    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

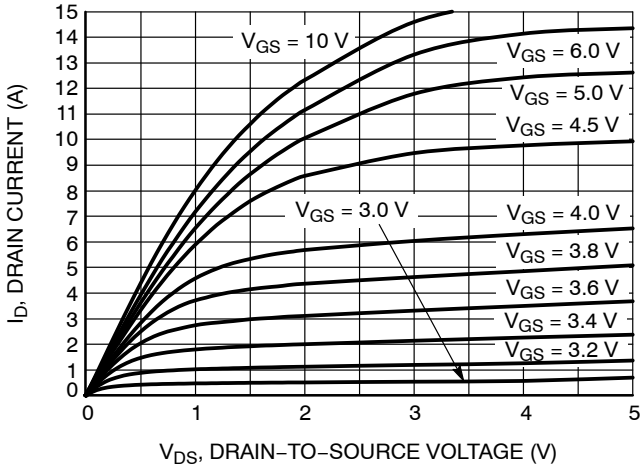


Figure 1. On-Region Characteristics

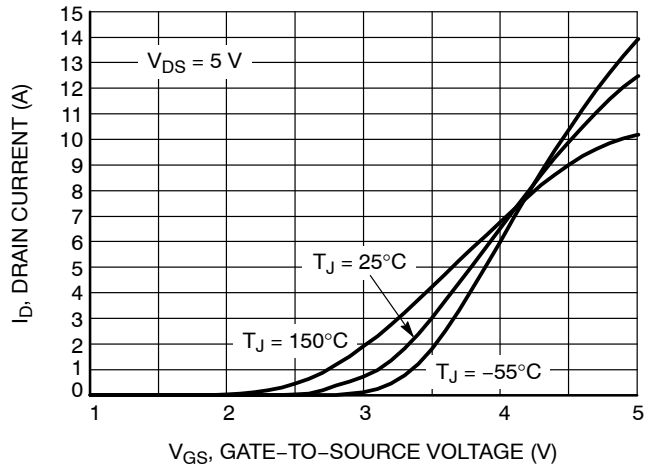


Figure 2. Transfer Characteristics

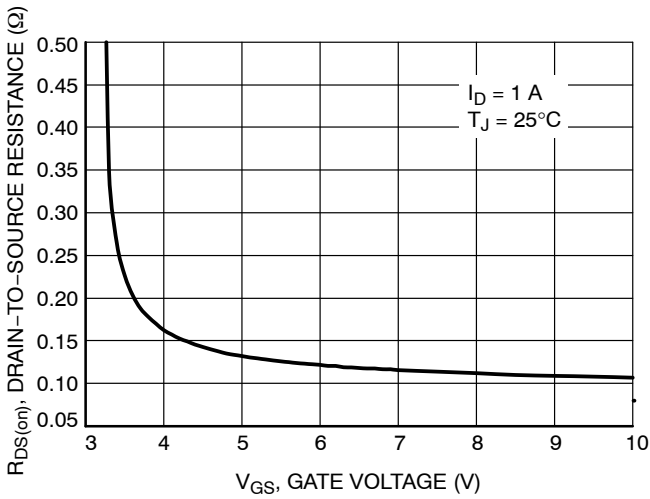


Figure 3. On-Resistance vs. Gate-to-Source Voltage

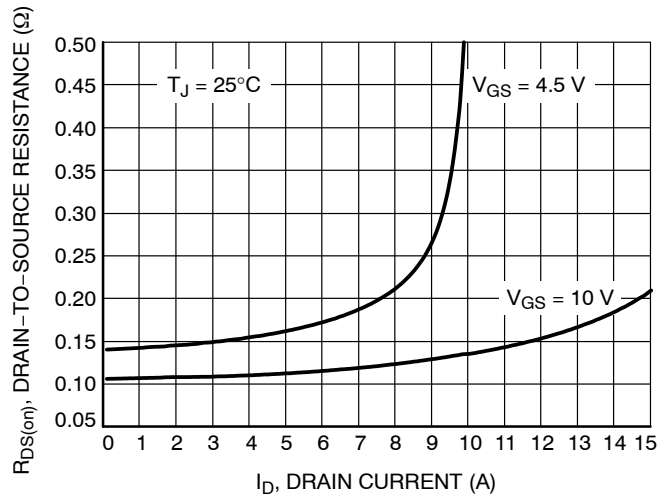


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

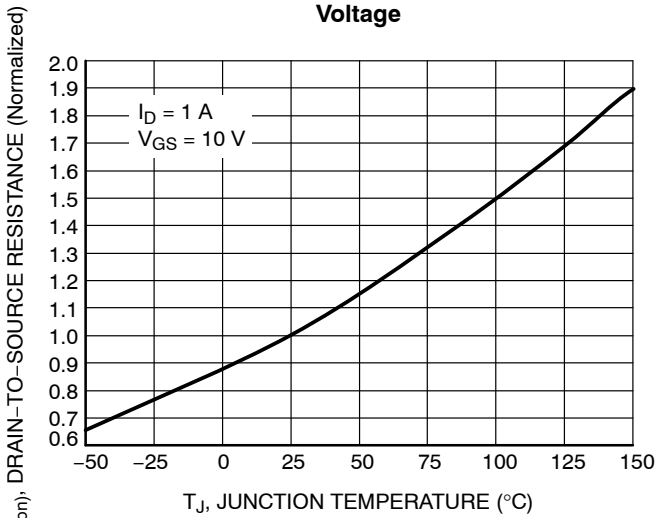


Figure 5. On-Resistance Variation with Temperature

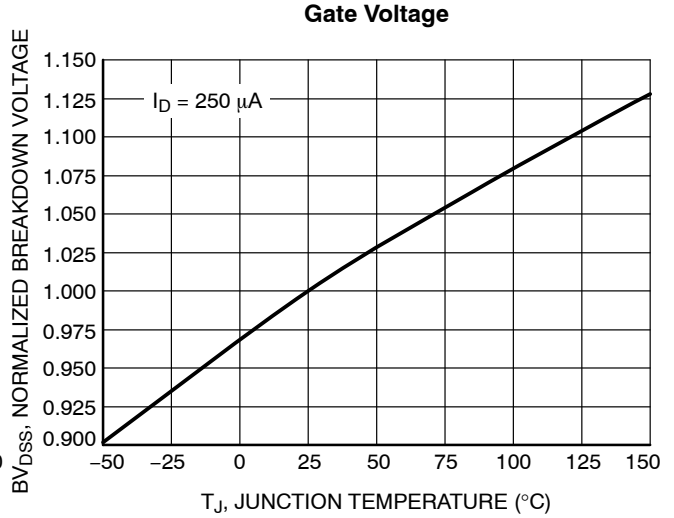


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

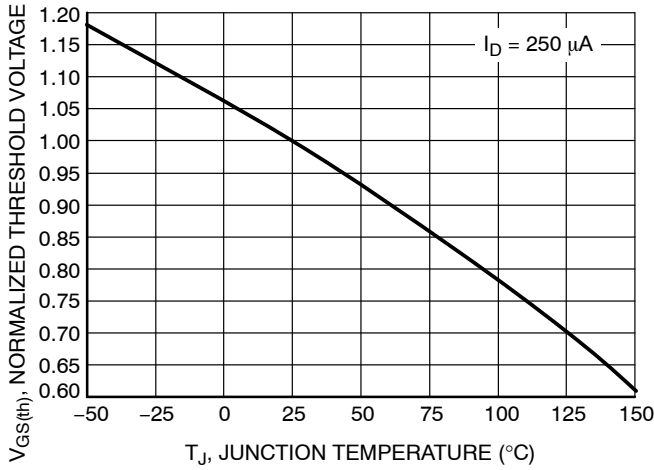


Figure 7. Threshold Voltage Variation with Temperature

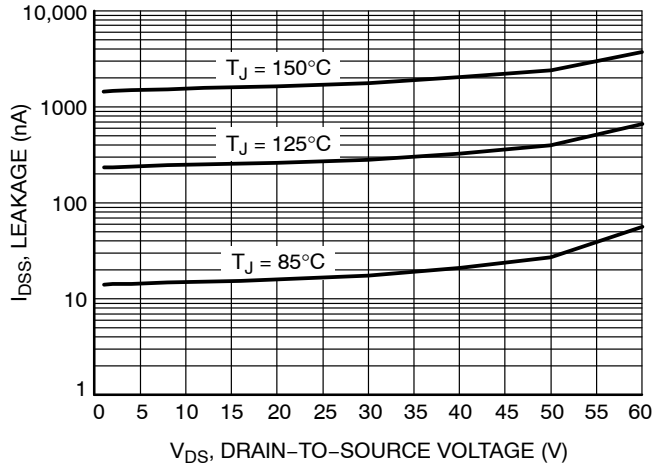


Figure 8. Drain-to-Source Leakage Current vs. Voltage

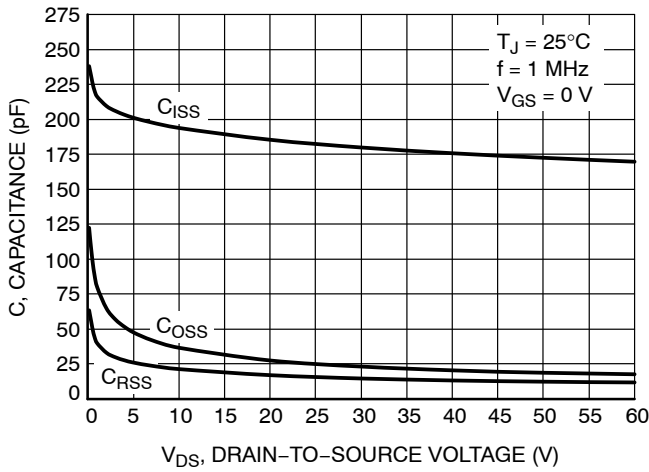


Figure 9. Capacitance Variation

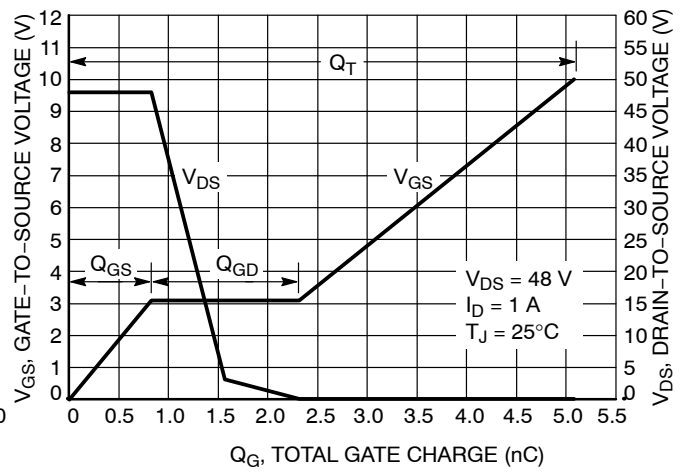


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

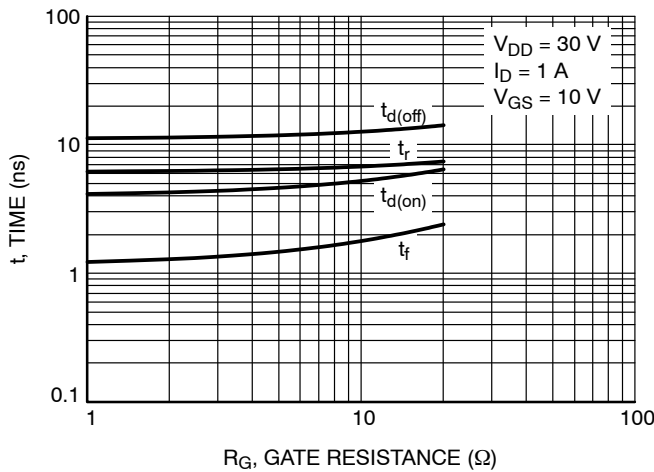


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

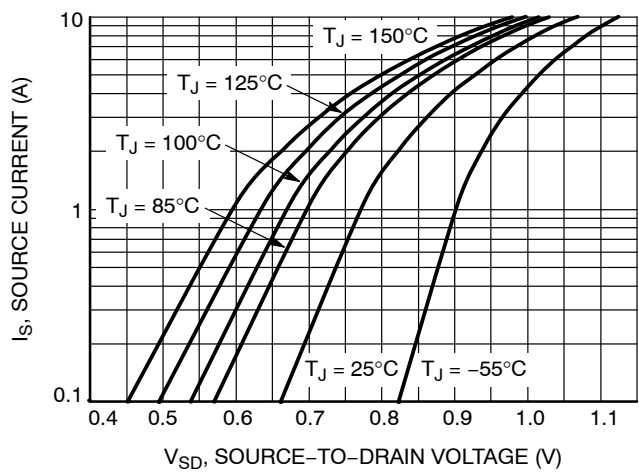


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

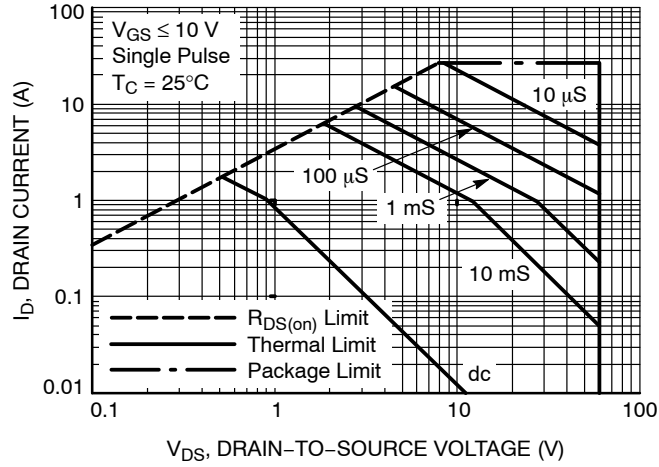


Figure 13. Maximum Rated Forward Biased Safe Operating Area

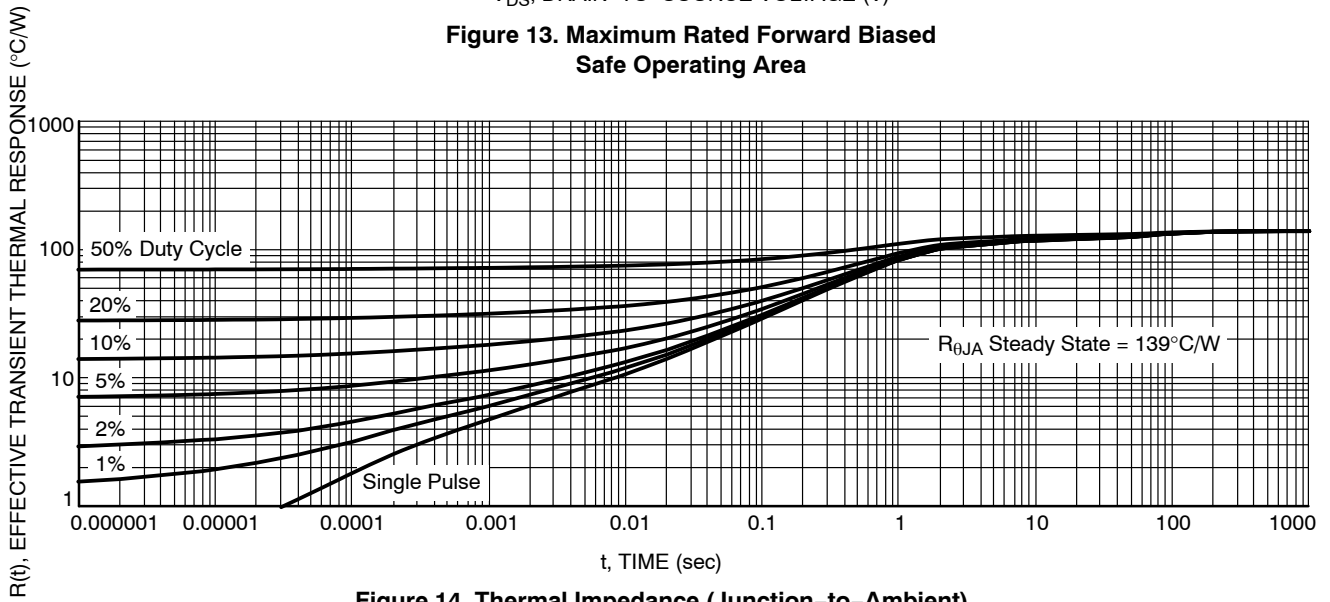


Figure 14. Thermal Impedance (Junction-to-Ambient)

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

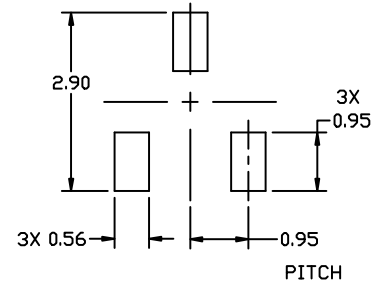
| DIM            | MILLIMETERS |      |      | INCHES |       |       |
|----------------|-------------|------|------|--------|-------|-------|
|                | MIN.        | NOM. | MAX. | MIN.   | NOM.  | MAX.  |
| A              | 0.89        | 1.00 | 1.11 | 0.035  | 0.039 | 0.044 |
| A1             | 0.01        | 0.06 | 0.10 | 0.000  | 0.002 | 0.004 |
| b              | 0.37        | 0.44 | 0.50 | 0.015  | 0.017 | 0.020 |
| c              | 0.08        | 0.14 | 0.20 | 0.003  | 0.006 | 0.008 |
| D              | 2.80        | 2.90 | 3.04 | 0.110  | 0.114 | 0.120 |
| E              | 1.20        | 1.30 | 1.40 | 0.047  | 0.051 | 0.055 |
| e              | 1.78        | 1.90 | 2.04 | 0.070  | 0.075 | 0.080 |
| L              | 0.30        | 0.43 | 0.55 | 0.012  | 0.017 | 0.022 |
| L1             | 0.35        | 0.54 | 0.69 | 0.014  | 0.021 | 0.027 |
| H <sub>E</sub> | 2.10        | 2.40 | 2.64 | 0.083  | 0.094 | 0.104 |
| T              | 0°          | ---  | 10°  | 0°     | ---   | 10°   |

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

|                         |                        |  |
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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

STYLE 1 THRU 5:  
 CANCELLED

STYLE 6:  
 PIN 1. BASE  
 2. EMITTER  
 3. COLLECTOR

STYLE 7:  
 PIN 1. EMITTER  
 2. BASE  
 3. COLLECTOR

STYLE 8:  
 PIN 1. ANODE  
 2. NO CONNECTION  
 3. CATHODE

STYLE 9:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 10:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE

STYLE 11:  
 PIN 1. ANODE  
 2. CATHODE  
 3. CATHODE-ANODE

STYLE 12:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. ANODE

STYLE 13:  
 PIN 1. SOURCE  
 2. DRAIN  
 3. GATE

STYLE 14:  
 PIN 1. CATHODE  
 2. GATE  
 3. ANODE

STYLE 15:  
 PIN 1. GATE  
 2. CATHODE  
 3. ANODE

STYLE 16:  
 PIN 1. ANODE  
 2. CATHODE  
 3. CATHODE

STYLE 17:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. CATHODE

STYLE 18:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. ANODE

STYLE 19:  
 PIN 1. CATHODE  
 2. ANODE  
 3. CATHODE-ANODE

STYLE 20:  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE

STYLE 21:  
 PIN 1. GATE  
 2. SOURCE  
 3. DRAIN

STYLE 22:  
 PIN 1. RETURN  
 2. OUTPUT  
 3. INPUT

STYLE 23:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 24:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE

STYLE 25:  
 PIN 1. ANODE  
 2. CATHODE  
 3. GATE

STYLE 26:  
 PIN 1. CATHODE  
 2. ANODE  
 3. NO CONNECTION

STYLE 27:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE

STYLE 28:  
 PIN 1. ANODE  
 2. ANODE  
 3. ANODE

|                         |                        |   |
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