

MOSFET - Power, N-Channel, SUPERFET[®] III, FAST

650 V, 55 mΩ, 47 A

NTP055N65S3H

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

Features

- 700 V @ T_J = 150°C
- Typ. R_{DS(on)} = 45 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 96 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 880 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

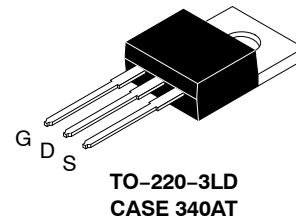
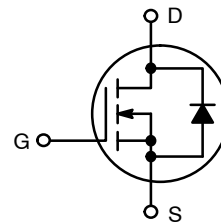
- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar



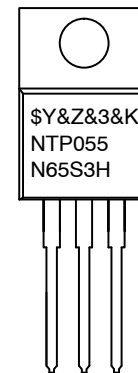
ON Semiconductor[®]

www.onsemi.com

V _{DSS}	R _{DS(on)} MAX	I _D MAX
650 V	55 mΩ @ 10 V	47 A



MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
NTP055N65S3H	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTP055N65S3H

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	DC	±30
		AC (f > 1 Hz)	±30
I _D	Drain Current	Continuous (T _C = 25°C)	47
		Continuous (T _C = 100°C)	30
I _{DM}	Drain Current	Pulsed (Note 1)	132
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	491	mJ
I _{AS}	Avalanche Current (Note 2)	6.8	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	3.05	mJ
dv/dt	MOSFET dv/dt	120	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	305
		Derate Above 25°C	2.44
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 6.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 23.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.41	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
NTP055N65S3H	NTP055N65S3H	TO-220-3LD (Pb-Free / Halogen Free)	50 Units / Tube

NTP055N65S3H

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	650			V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C		0.63		V/ $^\circ\text{C}$
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			2	μA
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$		3.2		
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 4.8\text{ mA}$	2.4		4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 23.5\text{ A}$		45	55	m Ω
g _{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 23.5\text{ A}$		52		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$		4305		pF
C _{oss}	Output Capacitance			73		pF
C _{oss(eff.)}	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		880		pF
C _{oss(er.)}	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		127		pF
Q _{g(tot)}	Total Gate Charge at 10 V	$V_{DS} = 400\text{ V}, I_D = 23.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)		96		nC
Q _{gs}	Gate to Source Gate Charge			23		nC
Q _{gd}	Gate to Drain "Miller" Charge			27		nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$		0.6		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 23.5\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$ (Note 4)		30		ns
t _r	Turn-On Rise Time			16		ns
t _{d(off)}	Turn-Off Delay Time			90		ns
t _f	Turn-Off Fall Time			2.8		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current			47		A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			132		A
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 23.5\text{ A}$			1.2	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 23.5\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		481		ns
Q _{rr}	Reverse Recovery Charge			7.7		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

NTP055N65S3H

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

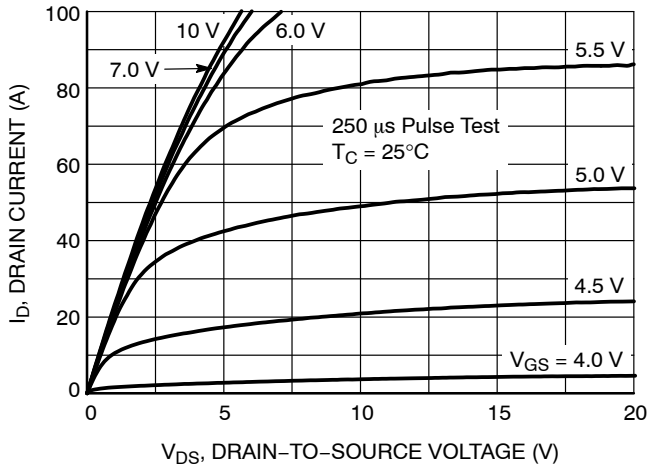


Figure 1. On-Region Characteristics

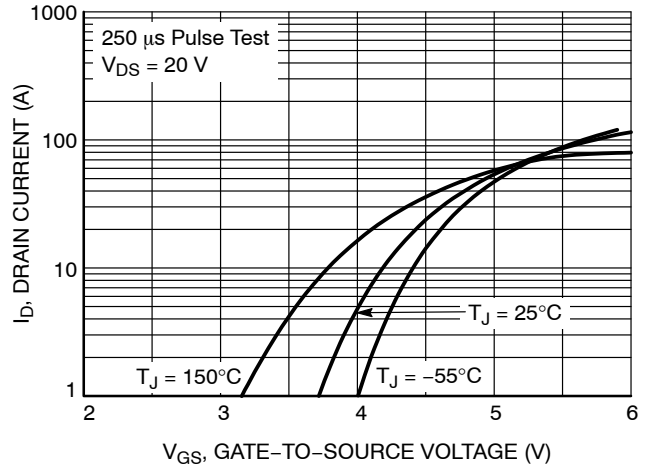


Figure 2. Transfer Characteristics

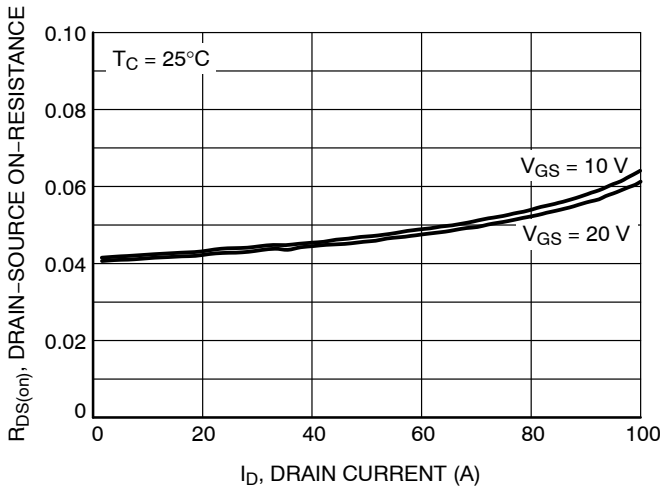


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

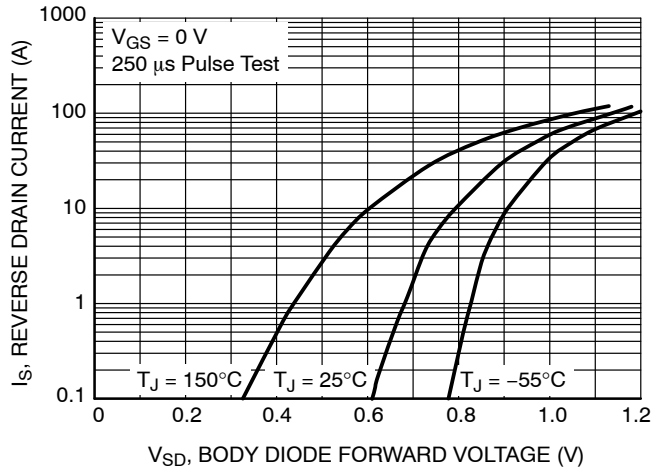


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

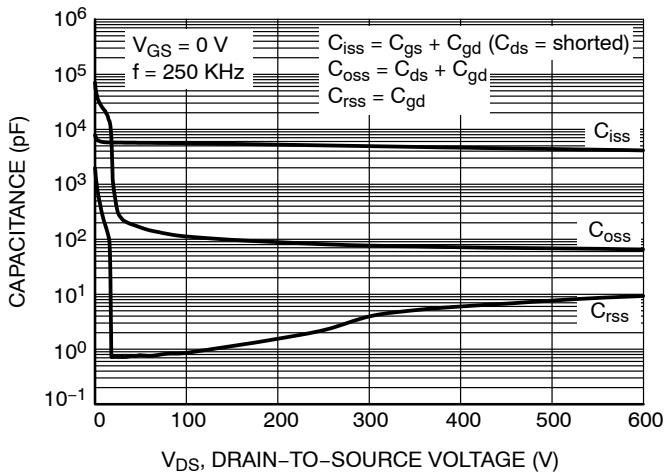


Figure 5. Capacitance Characteristics

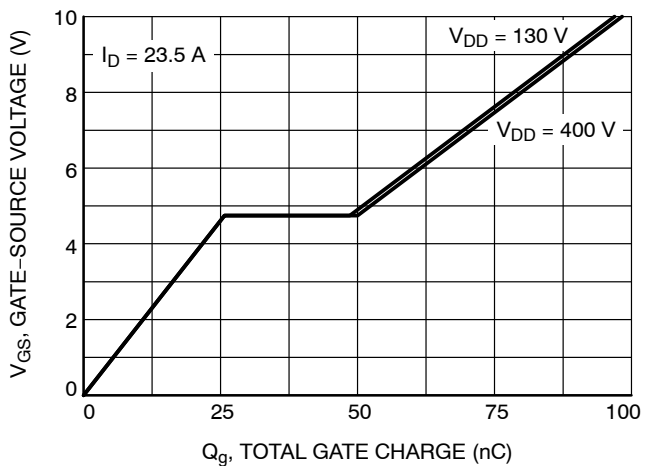


Figure 6. Gate Charge Characteristics

NTP055N65S3H

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

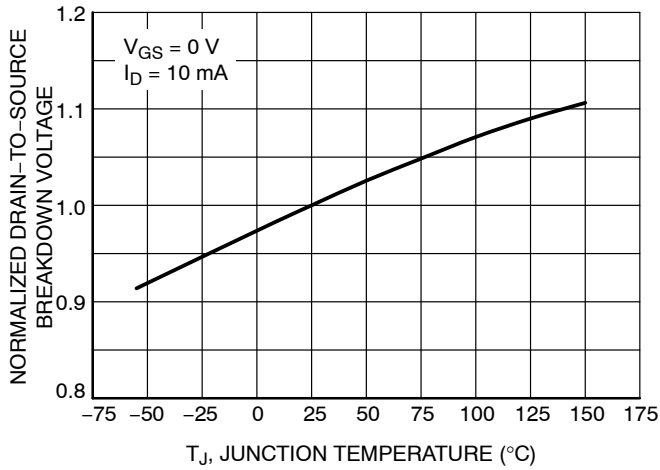


Figure 7. Breakdown Voltage Variation vs. Temperature

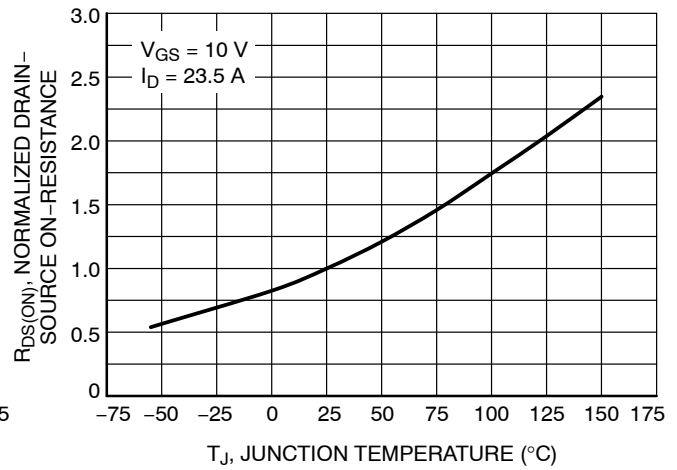


Figure 8. On-Resistance Variation vs. Temperature

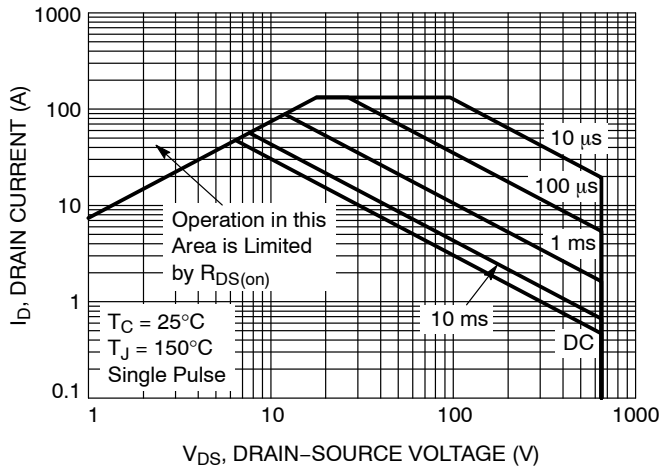


Figure 9. Maximum Safe Operating Area

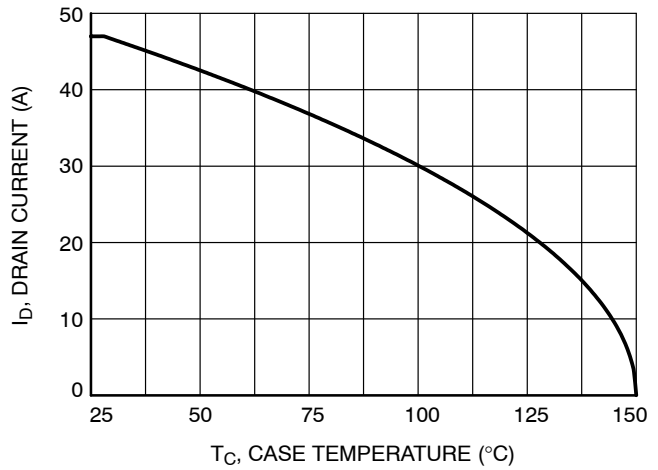


Figure 10. Maximum Drain Current vs. Case Temperature

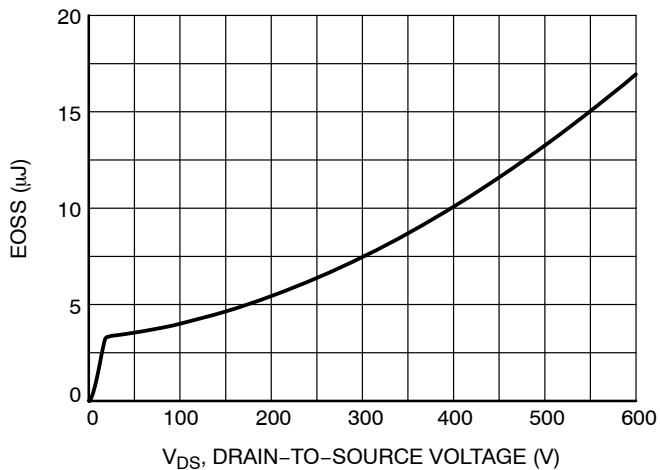


Figure 11. E_{OSS} vs. Drain to Source Voltage

NTP055N65S3H

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

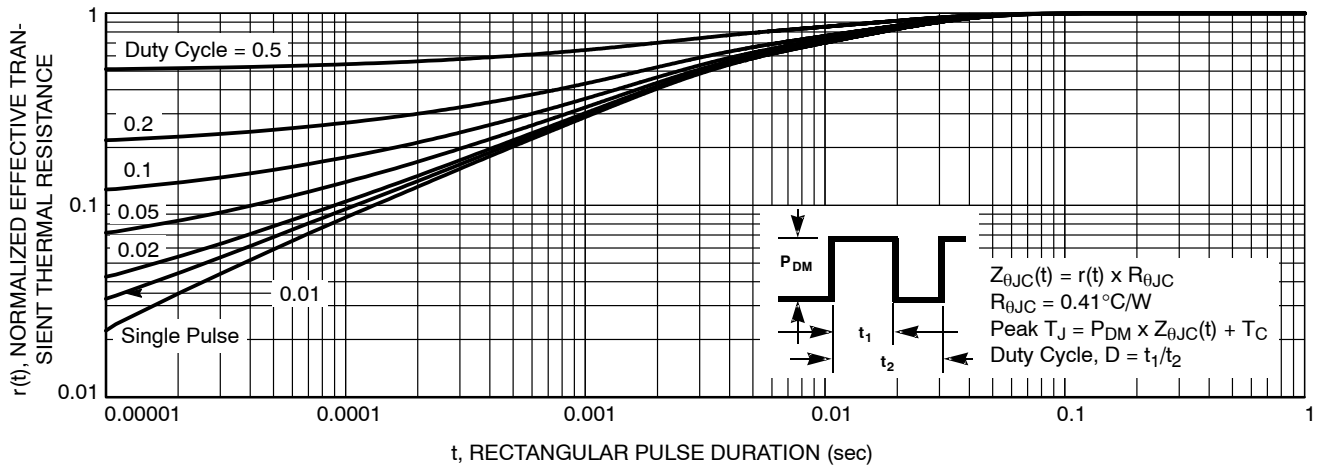


Figure 12. Transient Thermal Impedance

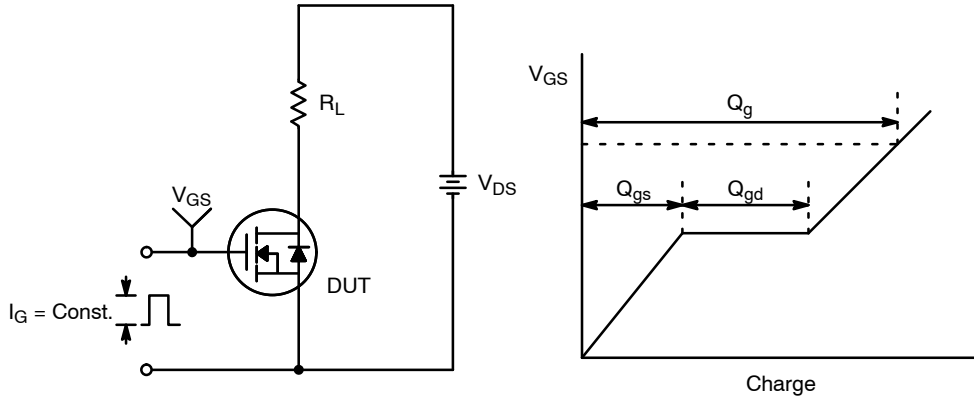


Figure 13. Gate Charge Test Circuit & Waveform

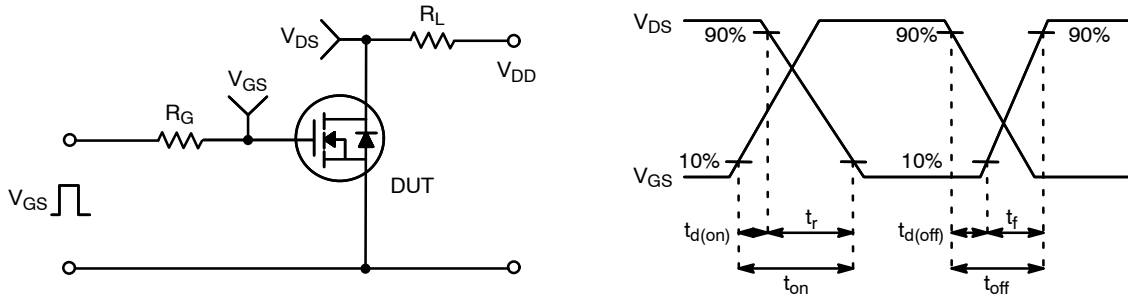


Figure 14. Resistive Switching Test Circuit & Waveforms

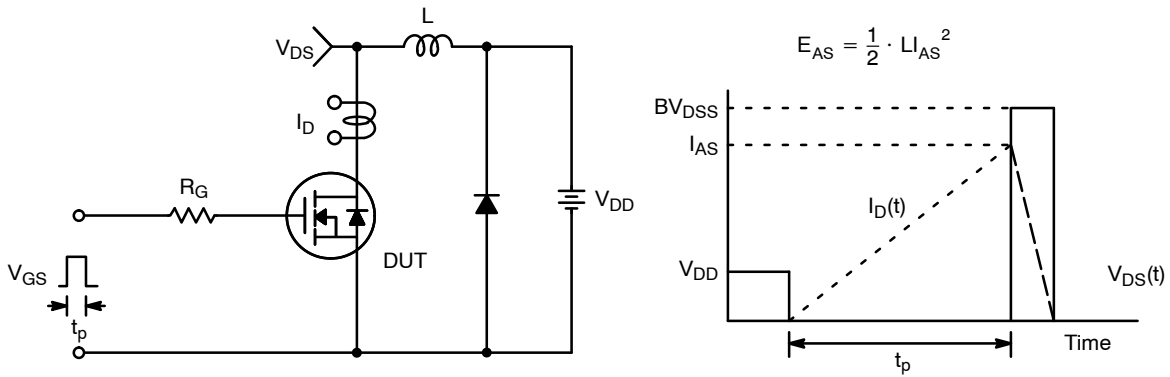


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

NTP055N65S3H

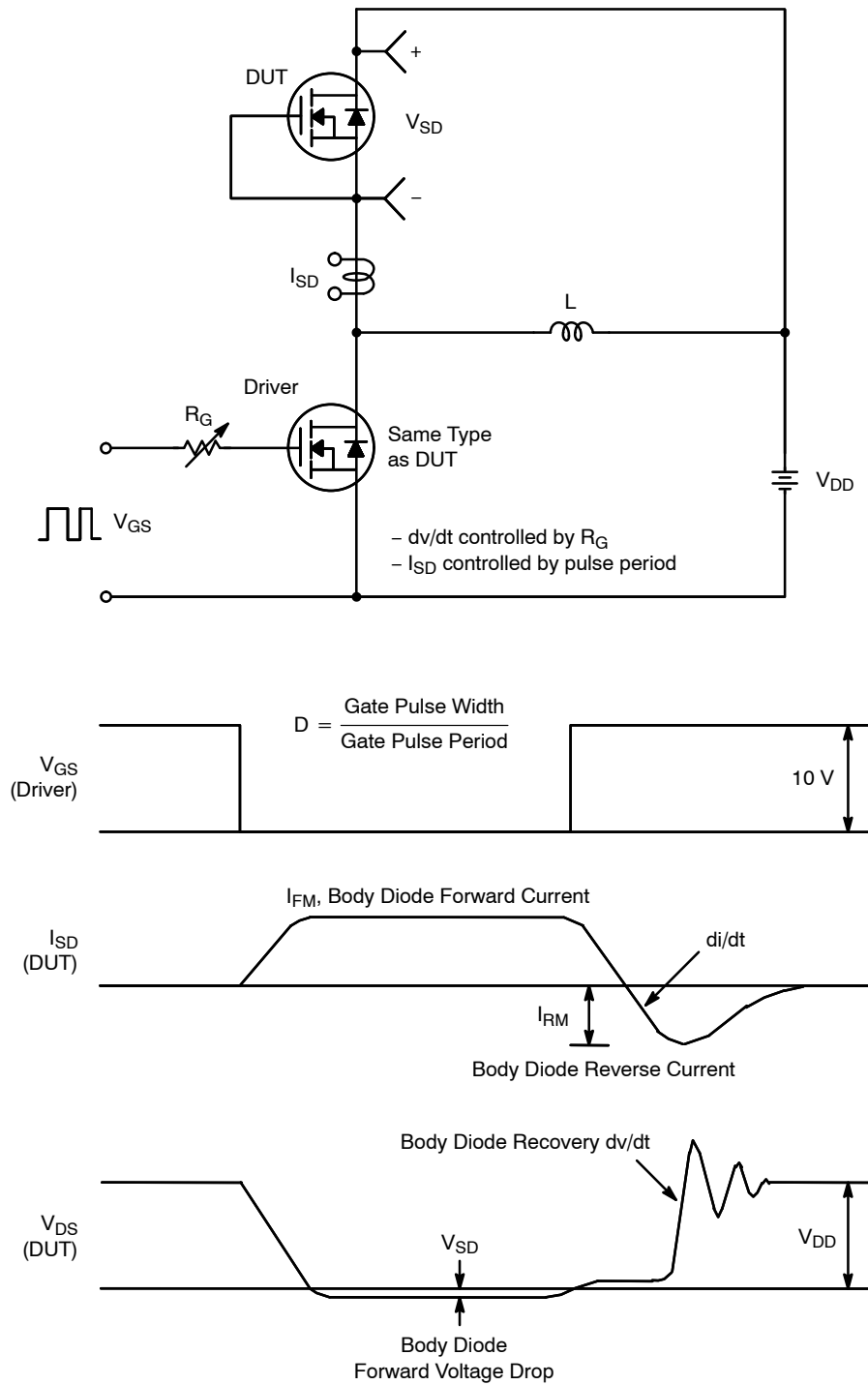


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
- G) PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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