

# Silicon Carbide (SiC) MOSFET – EliteSiC, 33 mohm, 650 V, M2, Power88

## NTMT045N065SC1

### Features

- Typ.  $R_{DS(on)} = 33\text{ m}\Omega$  @  $V_{GS} = 18\text{ V}$   
Typ.  $R_{DS(on)} = 45\text{ m}\Omega$  @  $V_{GS} = 15\text{ V}$
- Ultra Low Gate Charge ( $Q_{G(tot)} = 105\text{ nC}$ )
- Low Effective Output Capacitance ( $C_{oss} = 162\text{ pF}$ )
- 100% Avalanche Tested
- $T_J = 175^\circ\text{C}$
- RoHS Compliant

### Typical Applications

- SMPS (Switching Mode Power Supplies)
- Solar Inverters
- UPS (Uninterruptable Power Supplies)
- Energy Storage

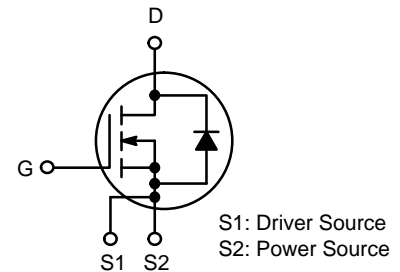
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	650	V	
Gate-to-Source Voltage		$V_{GS}$	-8/+22	V	
Recommended Operation Values of Gate – Source Voltage		$T_C < 175^\circ\text{C}$ $V_{GSop}$	-5/+18	V	
Continuous Drain Current (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	55	A
			$P_D$	187	W
Continuous Drain Current (Notes 1, 2)	Steady State	$T_C = 100^\circ\text{C}$	$I_D$	39	A
			$P_D$	94	W
Pulsed Drain Current (Note 3)		$T_C = 25^\circ\text{C}$	$I_{DM}$	197	A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	45	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 12\text{ A}_{pk}$ , $L = 1\text{ mH}$ ) (Note 4)		$E_{AS}$	72	mJ	
Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		$T_L$	260	$^\circ\text{C}$	

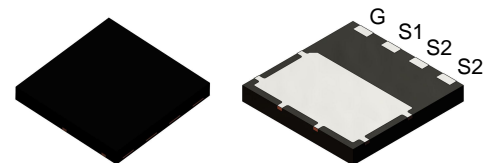
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4.  $E_{AS}$  of 72 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 50\text{ V}$ ,  $V_{GS} = 18\text{ V}$ .

$V_{DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	50 m $\Omega$ @ 18 V	55 A

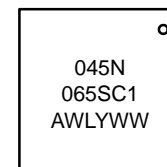


POWER MOSFET



TDFN4 8x8 2P  
CASE 520AB

### MARKING DIAGRAM



045N065SC1 = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NTMT045N065SC1	TDFN4 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.80	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	45	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650	–	–	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 20\text{ mA}$ , refer to $25^\circ\text{C}$	–	0.15	–	V/°C	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	10	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$	–	–	1	mA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +18/-5\text{ V}, V_{DS} = 0\text{ V}$	–	–	250	nA	

### ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 8\text{ mA}$	1.8	2.8	4.3	V
Recommended Gate Voltage	$V_{GOP}$		–5	–	+18	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 15\text{ V}, I_D = 25\text{ A}, T_J = 25^\circ\text{C}$	–	45	–	m $\Omega$
		$V_{GS} = 18\text{ V}, I_D = 25\text{ A}, T_J = 25^\circ\text{C}$	–	33	50	
		$V_{GS} = 18\text{ V}, I_D = 25\text{ A}, T_J = 175^\circ\text{C}$	–	40	–	
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 25\text{ A}$	–	16	–	S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 325\text{ V}$	–	1870	–	pF
Output Capacitance	$C_{OSS}$		–	162	–	
Reverse Transfer Capacitance	$C_{RSS}$		–	14	–	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 520\text{ V}, I_D = 25\text{ A}$	–	105	–	nC
Gate-to-Source Charge	$Q_{GS}$		–	27	–	
Gate-to-Drain Charge	$Q_{GD}$		–	30	–	
Gate-Resistance	$R_G$	$f = 1\text{ MHz}$	–	3.1	–	$\Omega$

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 400\text{ V}, I_D = 25\text{ A}, R_G = 2.2\text{ }\Omega$ , Inductive Load	–	13	–	ns
Rise Time	$t_r$		–	14	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	26	–	
Fall Time	$t_f$		–	7	–	
Turn-On Switching Loss	$E_{ON}$		–	47	–	$\mu\text{J}$
Turn-Off Switching Loss	$E_{OFF}$		–	33	–	
Total Switching Loss	$E_{TOT}$		–	80	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Source-Drain Diode Forward Current	$I_{SD}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$	–	–	45	A
Pulsed Source-Drain Diode Forward Current (Note 3)	$I_{SDM}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$	–	–	197	A
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}, T_J = 25^\circ\text{C}$	–	4.4	–	V

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise stated) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SOURCE-DRAIN DIODE CHARACTERISTICS</b>						
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -5/18\text{ V}$ , $I_{SD} = 25\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$	-	20	-	ns
Reverse Recovery Charge	$Q_{RR}$		-	108	-	nC
Reverse Recovery Energy	$E_{REC}$		-	4.5	-	$\mu\text{J}$
Peak Reverse Recovery Current	$I_{RRM}$		-	11	-	A
Charge time	$T_a$		-	11	-	ns
Discharge time	$T_b$		-	8.5	-	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

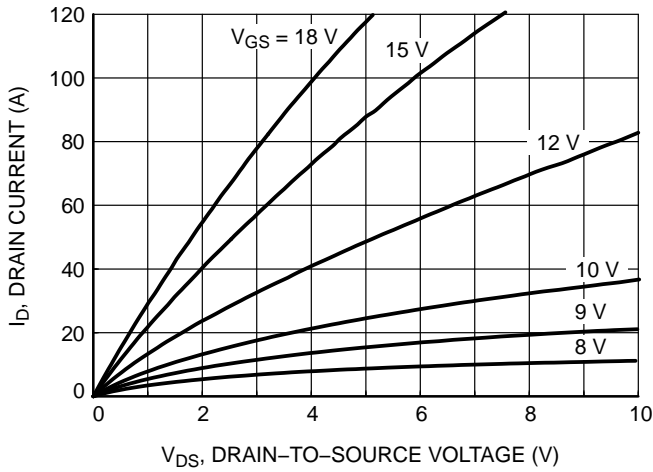


Figure 1. On-Region Characteristics

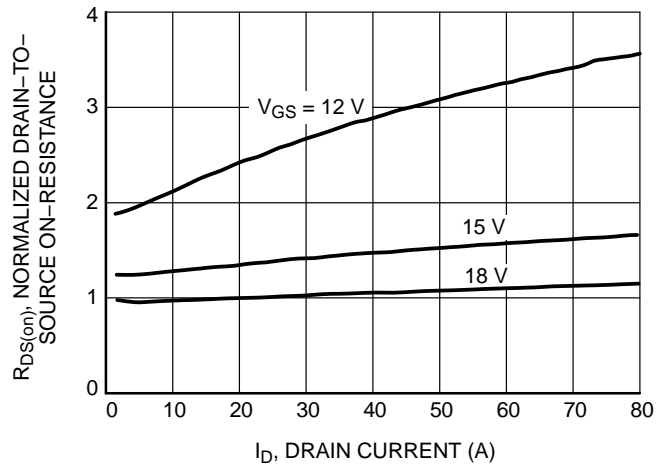


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

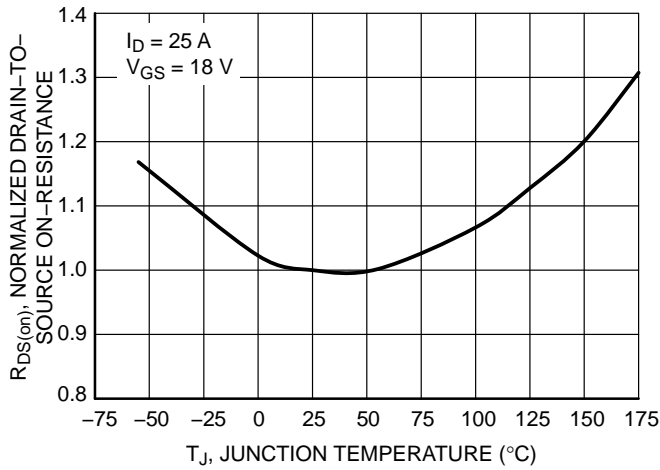


Figure 3. On-Resistance Variation with Temperature

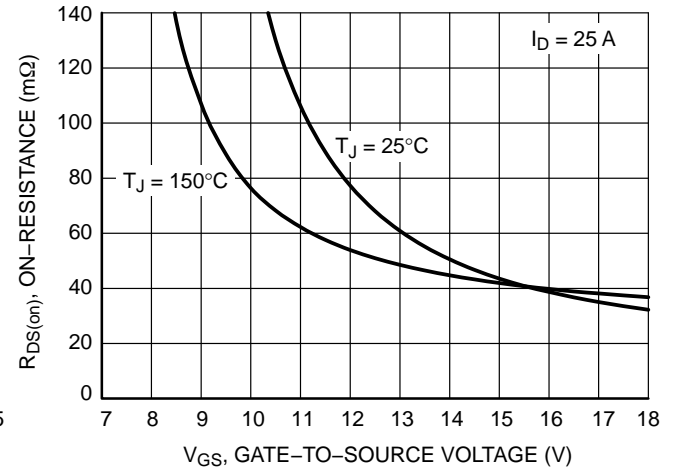


Figure 4. On-Resistance vs. Gate-to-Source Voltage

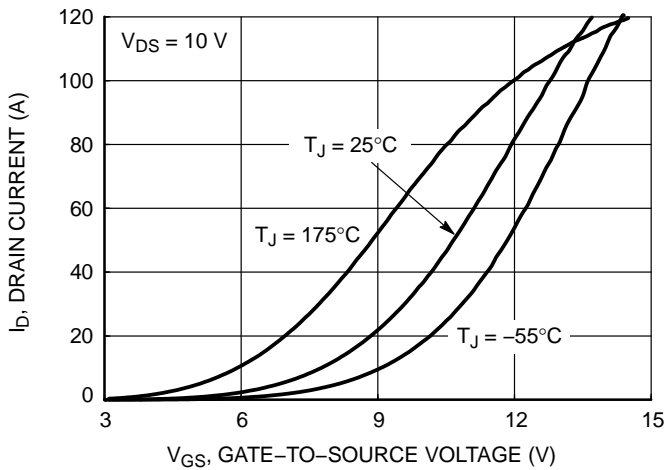


Figure 5. Transfer Characteristics

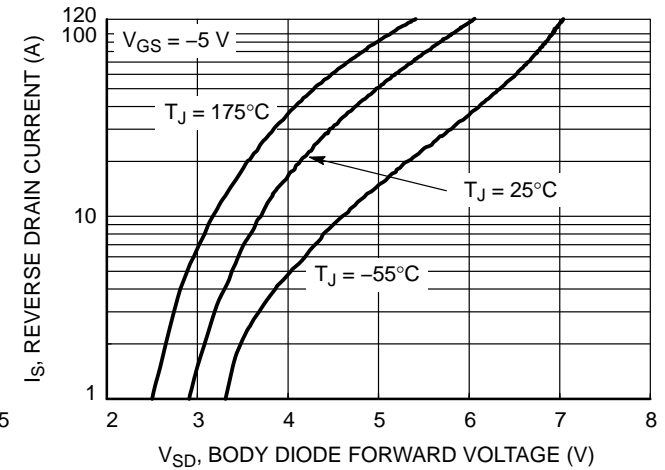


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (Continued)

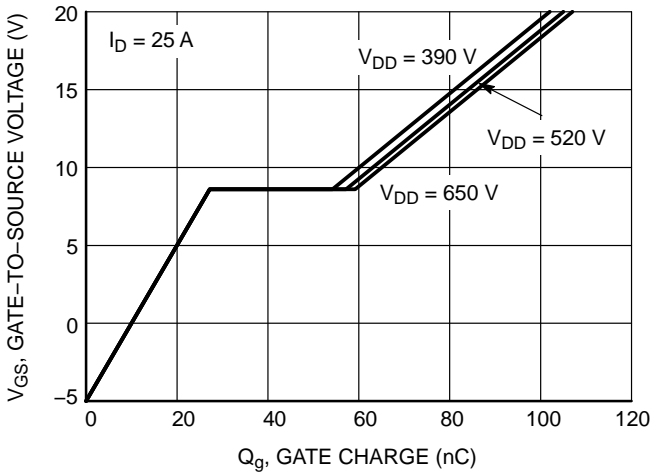


Figure 7. Gate-to-Source Voltage vs. Total Charge

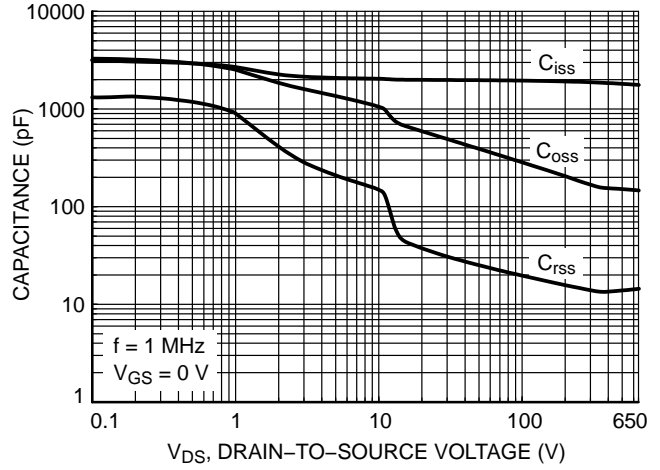


Figure 8. Capacitance vs. Drain-to-Source Voltage

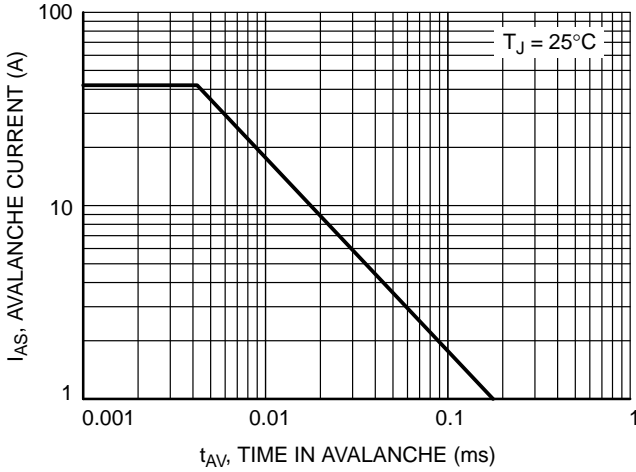


Figure 9. Unclamped Inductive Switching Capability

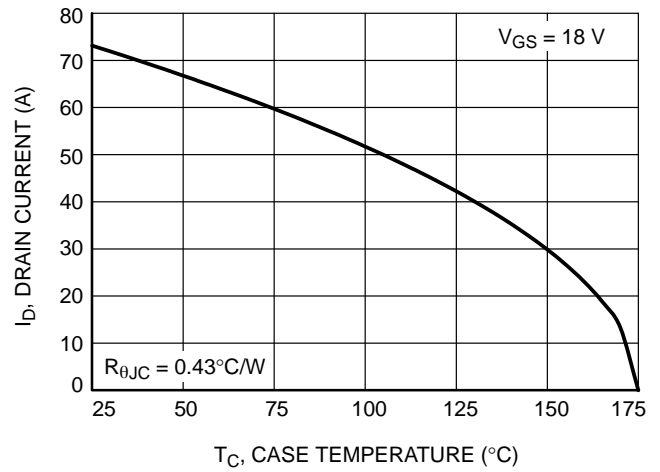


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

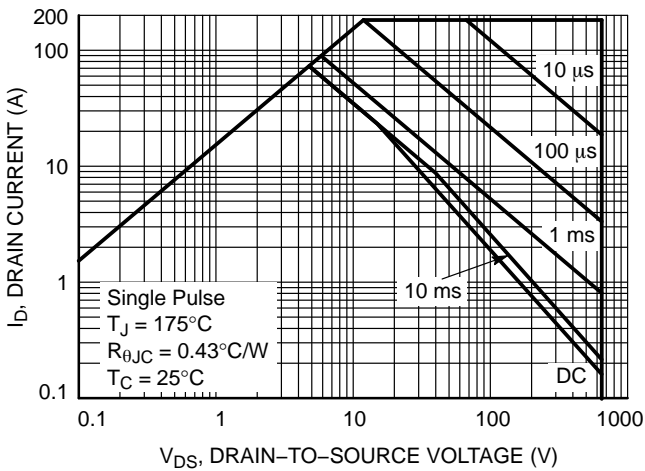


Figure 11. Safe Operating Area

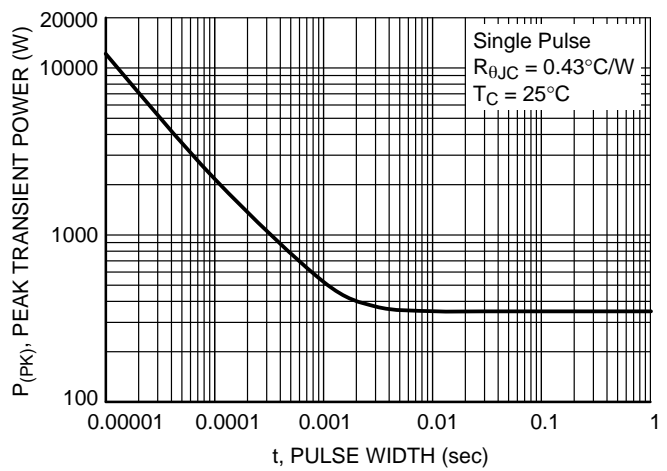


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS (Continued)

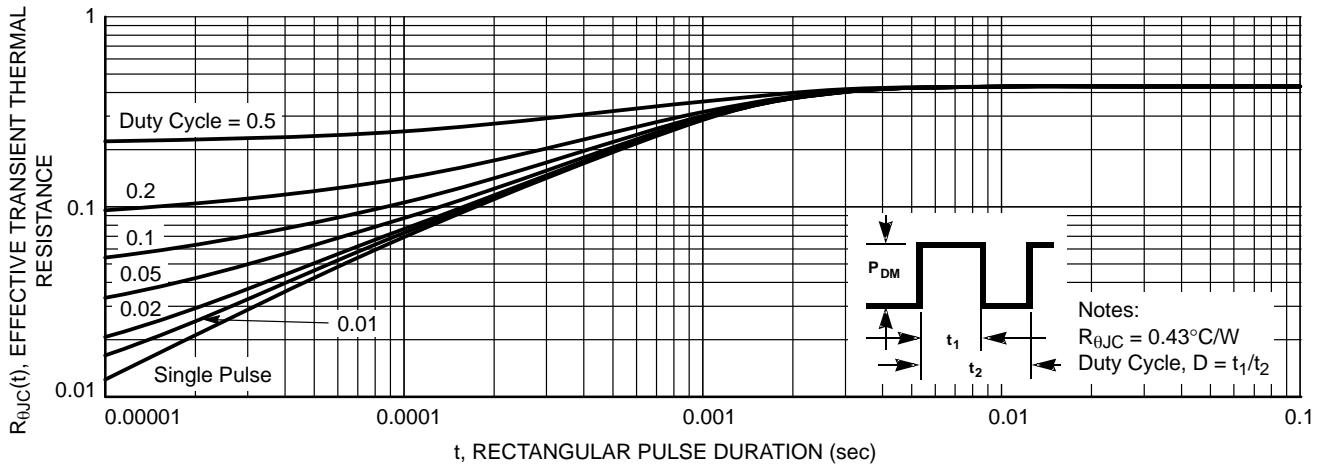
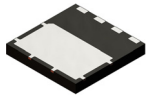


Figure 13. Transient Thermal Impedance

# MECHANICAL CASE OUTLINE

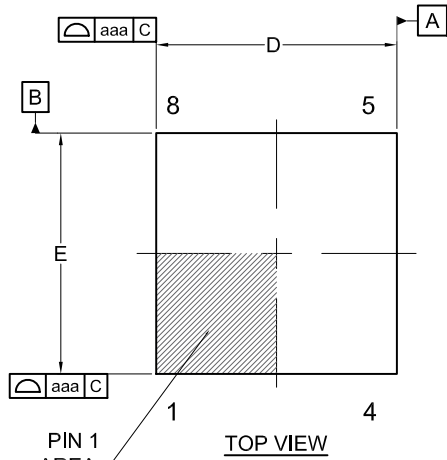
## PACKAGE DIMENSIONS

ON Semiconductor®

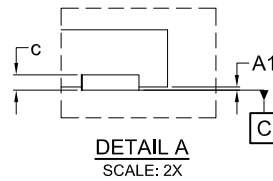


**TDFN4 8x8, 2P**  
**CASE 520AB**  
**ISSUE O**

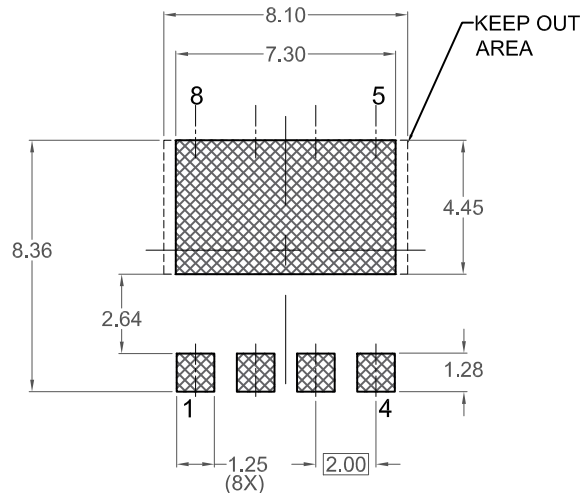
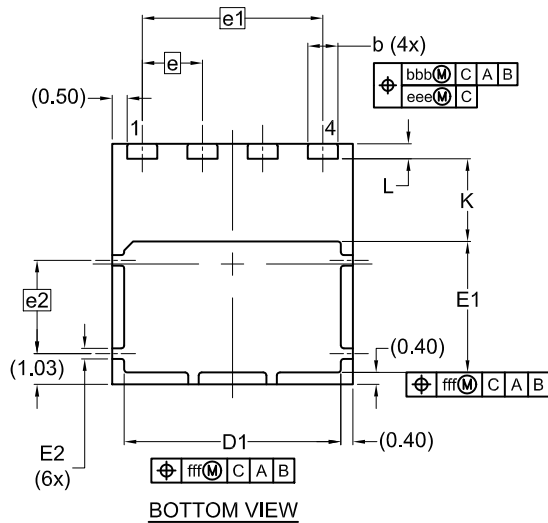
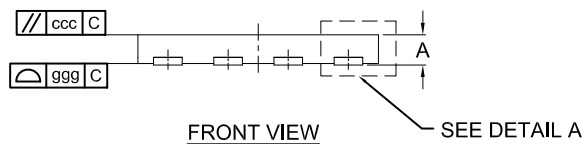
DATE 24 APR 2019



NOTES: UNLESS OTHERWISE SPECIFIED  
 A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



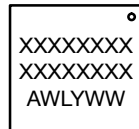
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	0.15	0.25	0.35
e	2.00 BSC		
e1	6.00 BSC		
e2	3.10 BSC		
K	(2.75)		
L	0.40	0.50	0.60
aaa	0.10		
bbb	0.10		
ccc	0.05		
eee	0.05		
fff	0.10		
ggg	0.15		



**RECOMMENDED LAND PATTERN**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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