

MOSFET - Power, Single N-Channel, DUAL COOL[®], DFN8

80 V, 4.0 mΩ, 136 A

NTMFSC004N08MC

Features

- Advanced Dual-Sided Cooled Packaging
- Ultra Low R_{DS(on)} to Minimize Conduction Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Orring FET/Load Switching
- Synchronous Rectifier
- DC-DC Conversion

MAXIMUM RATINGS (T_J = 25°C, Unless otherwise specified)

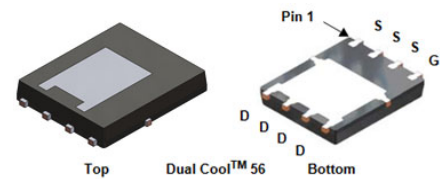
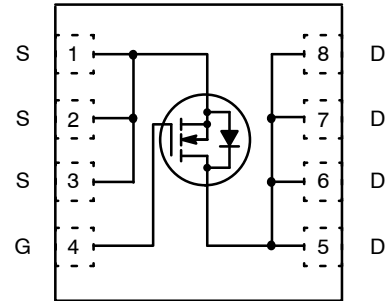
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	80	V
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 2)	Steady State T _C = 25°C	I _D	136	A
Power Dissipation R _{θJC} (Note 2)		P _D	127	W
Continuous Drain Current R _{θJA} (Note 1, 2)	Steady State T _A = 25°C	I _D	80	A
Power Dissipation R _{θJA} (Note 1, 2)		P _D	3.2	W
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs	I _{DM}	487	A
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C
Source Current (Body Diode)		I _S	157	A
Single Pulse Drain-to-Source Avalanche Energy (I _{AV} = 55 A, L = 0.1 mH)		E _{AS}	178	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T _L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

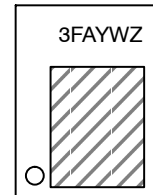
V _{SSS}	R _{SS(ON)} MAX	I _D MAX
80 V	4.0 mΩ @ 10 V	136 A
	8.5 mΩ @ 6 V	

N-Channel MOSFET



DFN8 5x6.15
CASE 506EG

MARKING DIAGRAM



- 3F = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	0.98	°C/W
$R_{\theta JT}$	Junction-to-Case Top – Steady State	1.49	
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 1)	39	

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC004N08MC	4N08MC	DFN8 5x6.15 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		0.05		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate – to – Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	2.9	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-6.5		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 44\text{ A}$		3.1	4.0	mΩ
		$V_{GS} = 6\text{ V}, I_D = 22\text{ A}$		5.0	8.5	
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		1.3		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		2980		pF
Output Capacitance	C_{OSS}			950		
Reverse Transfer Capacitance	C_{RSS}			50		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 40\text{ V}, I_D = 22\text{ A}$		27.8		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 22\text{ A}$		43.4		
Gate-to-Source Charge	Q_{GS}			15		
Gate-to-Drain Charge	Q_{GD}			7		

SWITCHING CHARACTERISTICS (Note 3)

Turn – On Delay Time	$t_d(ON)$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 44\text{ A}, R_G = 2.5\ \Omega$		11.7		ns
Rise Time	t_r			21.5		
Turn – Off Delay Time	$t_d(OFF)$			28.7		
Fall Time	t_f			5.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 44\text{ A}$	$T_J = 25^\circ\text{C}$	0.83	1.30	V
			$T_J = 125^\circ\text{C}$	0.69		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 44\text{ A}$		44		ns
Reverse Recovery Charge	Q_{RR}			50		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

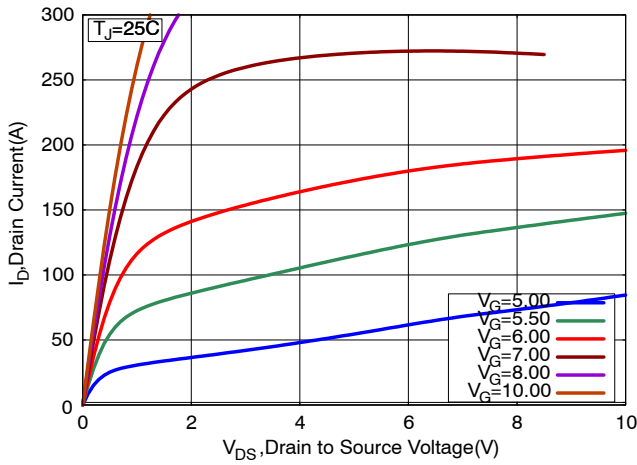


Figure 1. On-Region Characteristics

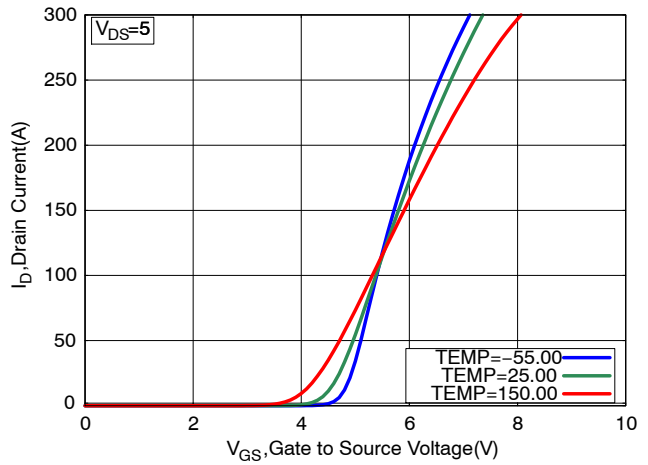


Figure 2. Transfer Characteristics

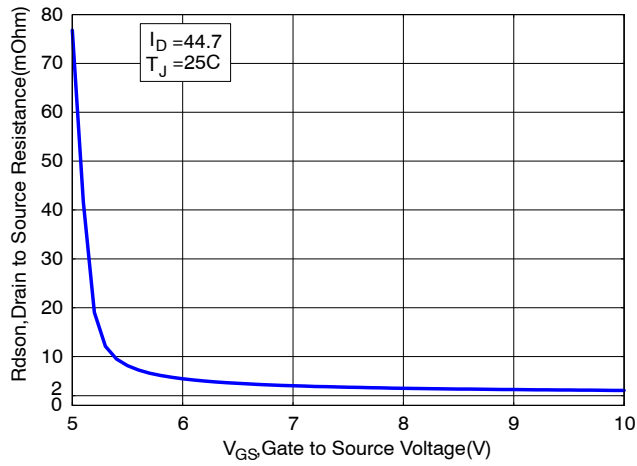


Figure 3. On-Resistance vs. V_{GS}

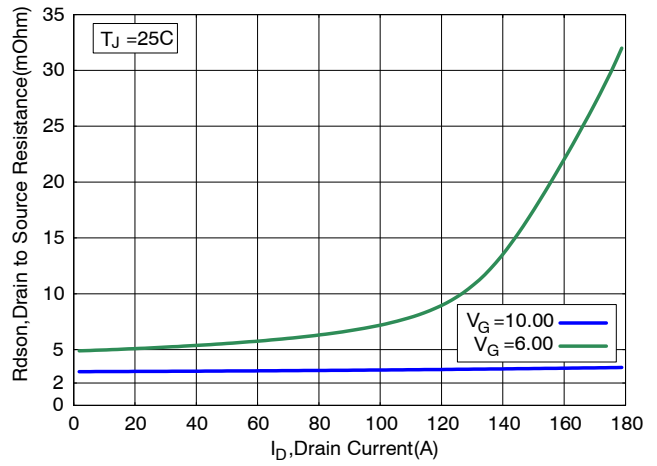


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

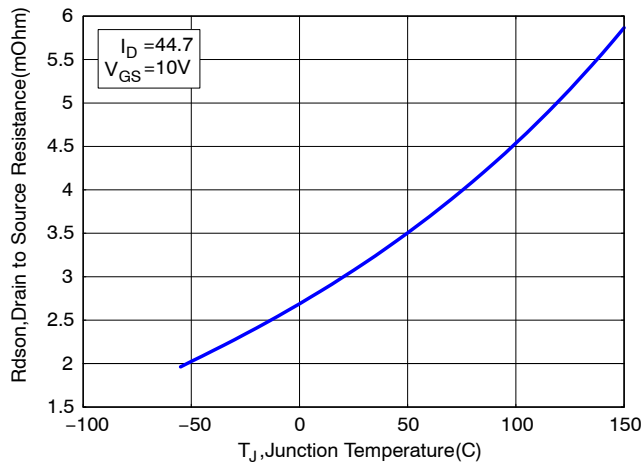


Figure 5. On-Resistance Variation with Temperature

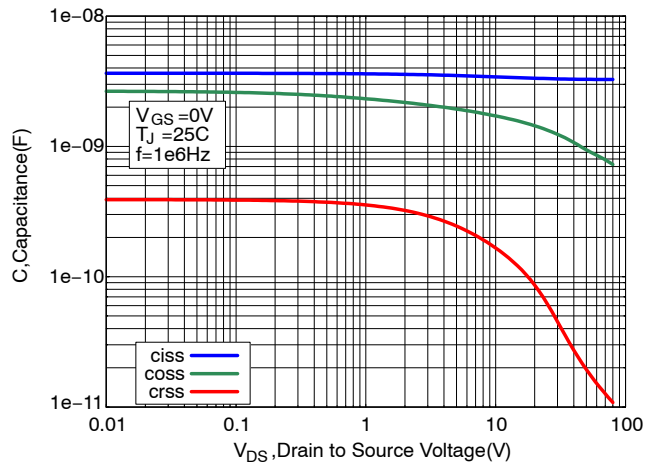


Figure 6. Capacitance Variation

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TYPICAL CHARACTERISTICS

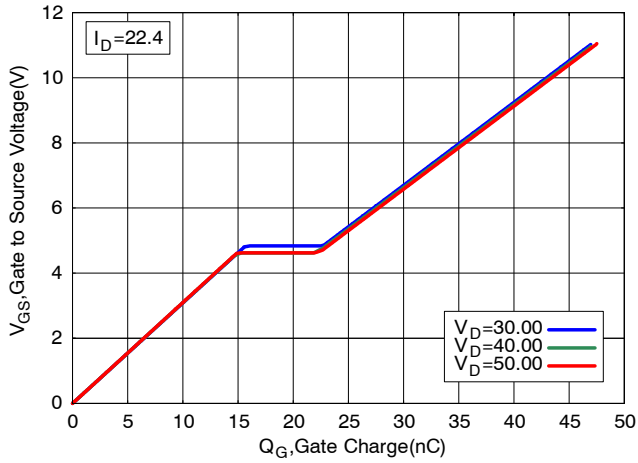


Figure 7. Gate-to-Source Voltage vs. Total Charge

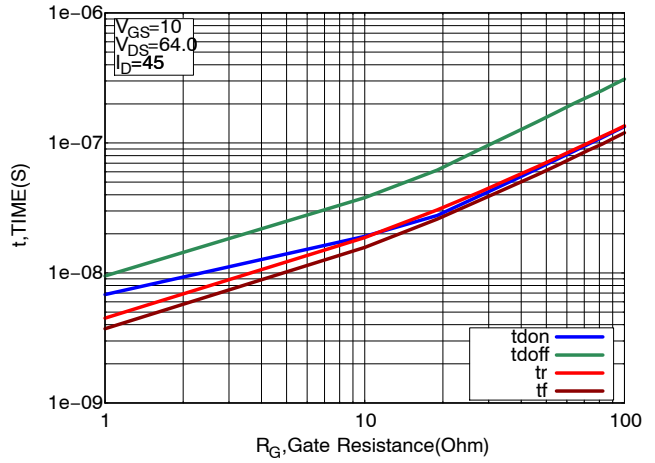


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

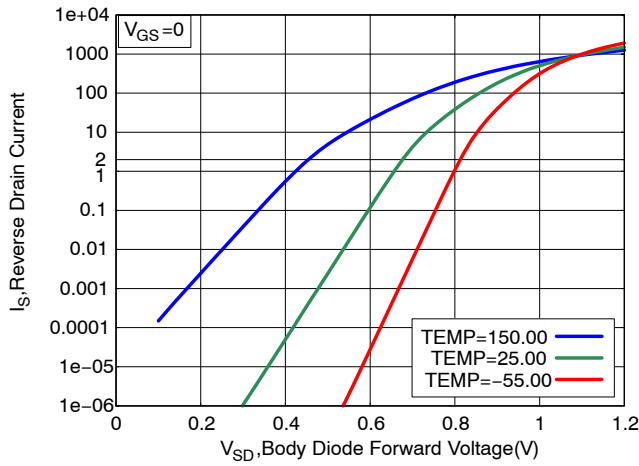


Figure 9. Diode Forward Voltage vs. Current

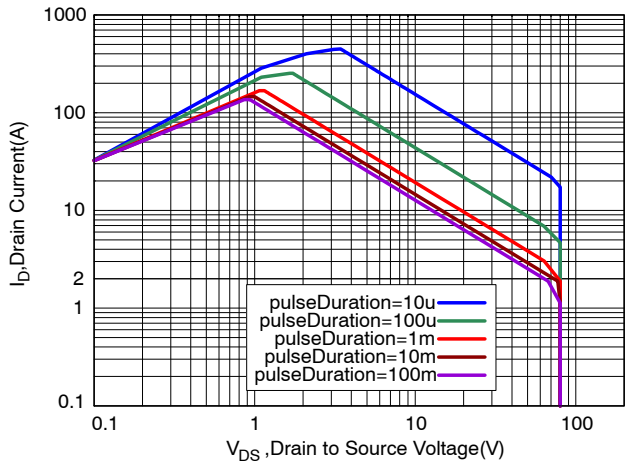


Figure 10. Maximum Rated Forward Biased Safe Operating Area

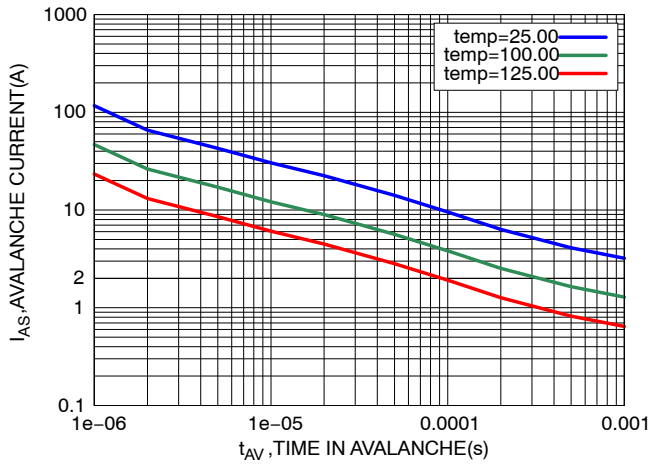


Figure 11. I_{PEAK} vs. Time in Avalanche

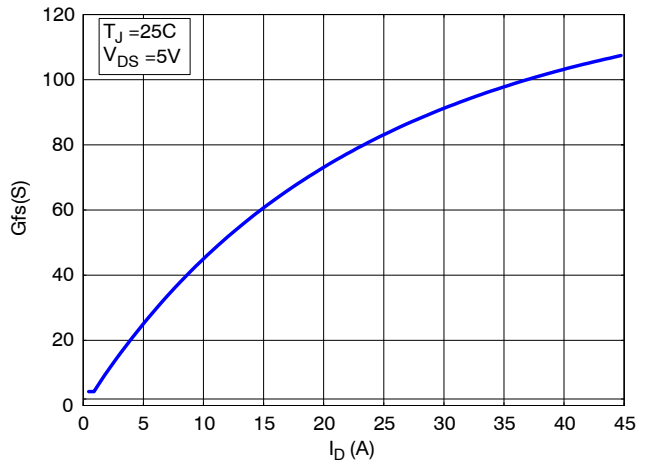


Figure 12. G_{FS} vs. I_D

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TYPICAL CHARACTERISTICS

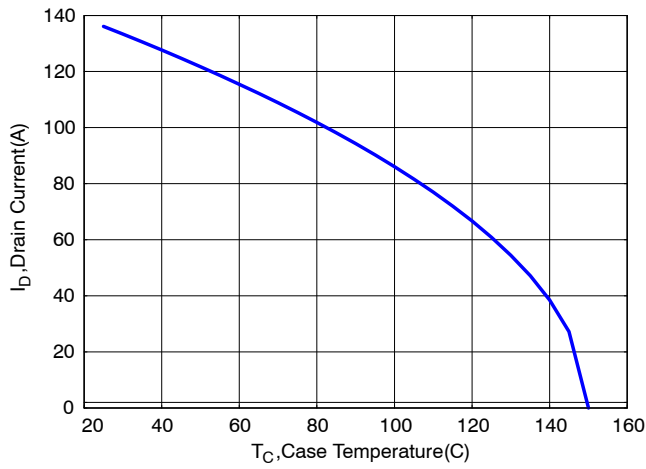


Figure 13. Maximum Current vs. Case Temperature

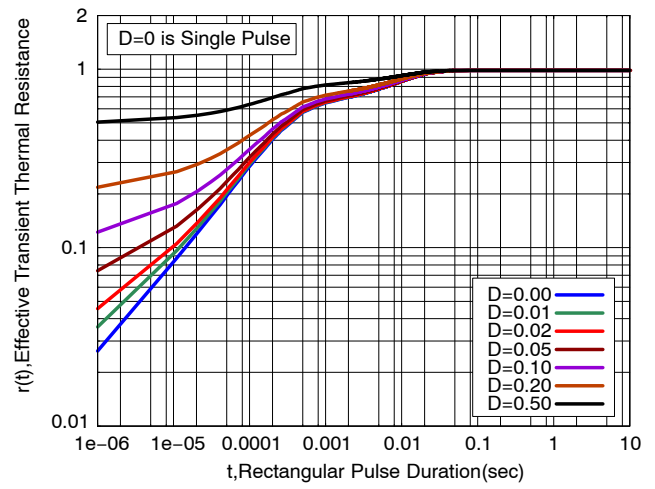


Figure 14. Thermal Response

MECHANICAL CASE OUTLINE

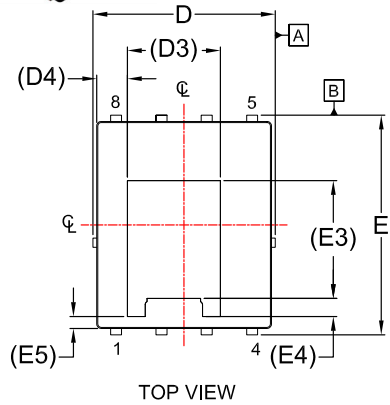
PACKAGE DIMENSIONS

ON Semiconductor®



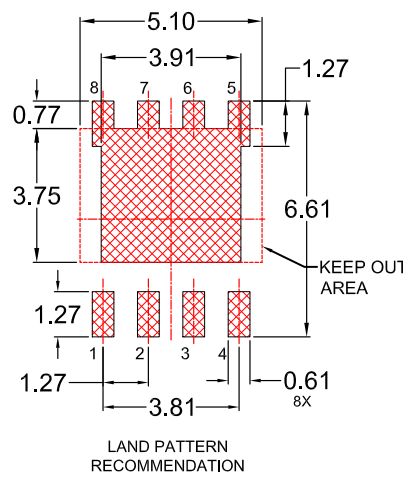
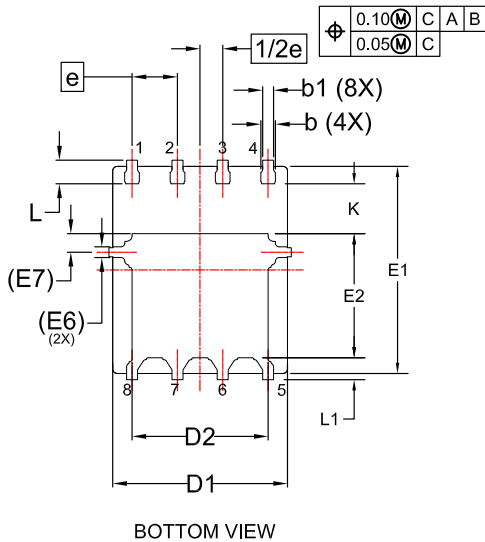
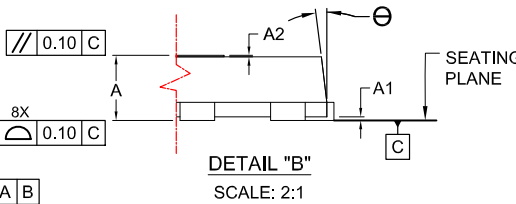
DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

DATE 25 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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