

# NTMFS4121N

## Power MOSFET

30 V, 29 A, Single N-Channel,  
SO-8 Flat Lead

### Features

- Low  $R_{DS(on)}$
- Optimized Gate Charge
- Low Inductance SO-8 Package
- These are Pb-Free Devices

### Applications

- Notebooks, Graphics Cards
- DC-DC Converters
- Synchronous Rectification

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	17	A
		$T_A = 85^\circ\text{C}$	12	
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$	29	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	2.2	W
		$t \leq 10$ s	6.6	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	11	A
		$T_A = 85^\circ\text{C}$	8.0	
		$T_A = 25^\circ\text{C}$	0.9	W
Power Dissipation (Note 2)				
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$	88	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	6.5	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_{PK} = 29$ A, $L = 1$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	430	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	56.2	$^\circ\text{C/W}$
Junction-to-Ambient - $t \leq 10$ s (Note 1)	$R_{\theta JA}$	19	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	141.1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

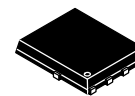
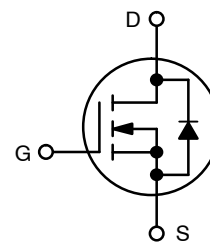
1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = 1.0 in sq).



ON Semiconductor®

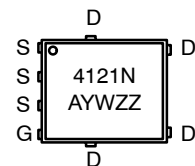
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ Max (Note 1)
30 V	4.0 m $\Omega$ @ 10 V	29 A
	5.5 m $\Omega$ @ 4.5 V	



SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



4121N = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4121NT1G	SO-8 FL (Pb-Free)	1500 Tape & Reel
NTMFS4121NT3G	SO-8 FL (Pb-Free)	5000 Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMFS4121N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		4.2	5.25	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 21\text{ A}$		5.5	7.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 24\text{ A}$		20		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 24\text{ V}$		2700		pF
Output Capacitance	$C_{OSS}$			480		
Reverse Transfer Capacitance	$C_{RSS}$			290		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 21\text{ A}$		24	40	nC
Threshold Gate Charge	$Q_{G(TH)}$			3.0		
Gate-to-Source Charge	$Q_{GS}$			7.3		
Gate-to-Drain Charge	$Q_{GD}$			10.2		
Gate Resistance	$R_G$			1.5		

## SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 1.0\text{ A}, R_L = 15\ \Omega, R_G = 3.0\ \Omega$		16		ns
Rise Time	$t_r$			29		
Turn-Off Delay Time	$t_{d(OFF)}$			32		
Fall Time	$t_f$			31		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 6.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 6.0\text{ A}$		34		ns	
Charge Time	$t_a$			18			
Discharge Time	$t_b$			16			
Reverse Recovery Charge	$Q_{RR}$			25.4			nC

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

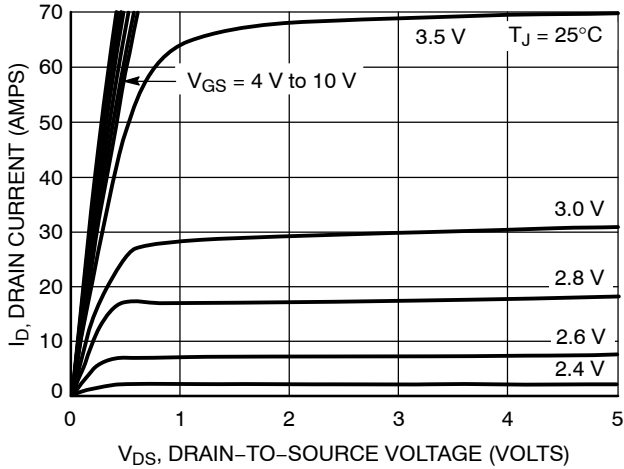


Figure 1. On-Region Characteristics

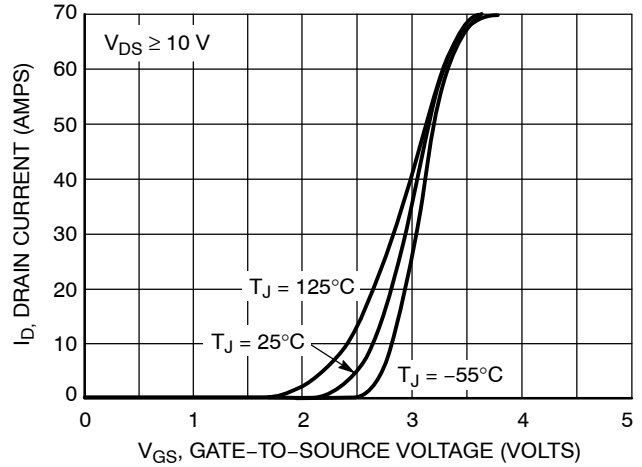


Figure 2. Transfer Characteristics

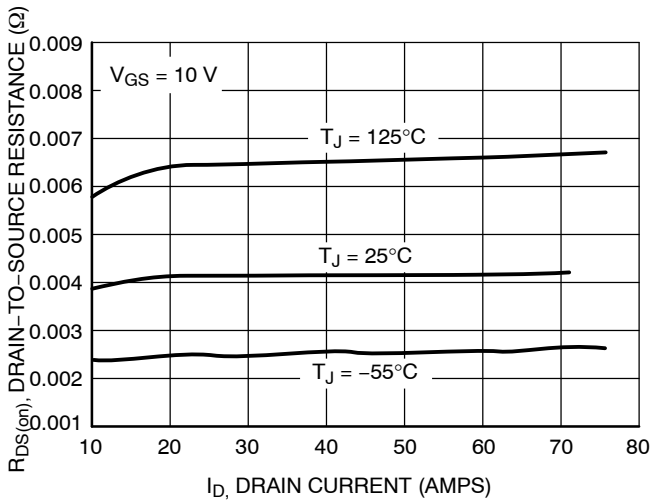


Figure 3. On-Resistance vs. Drain Current and Temperature

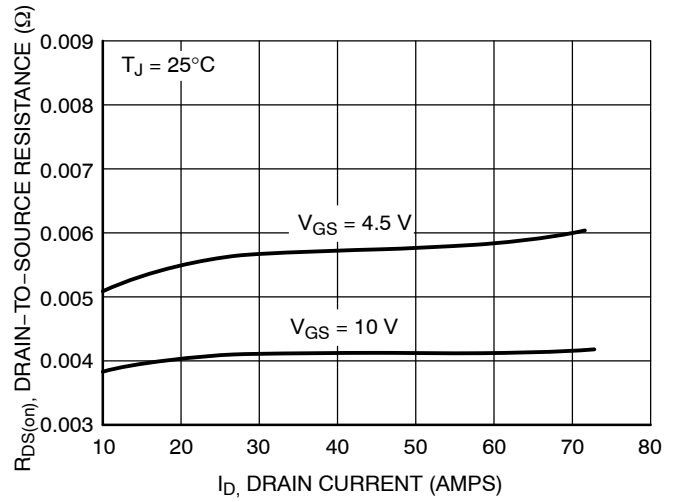


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

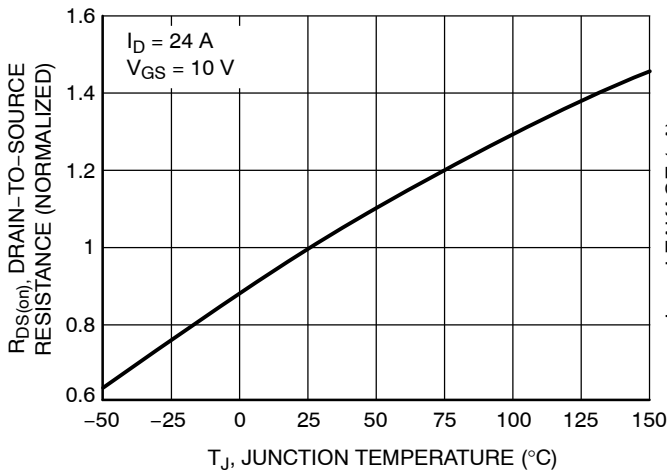


Figure 5. On-Resistance Variation with Temperature

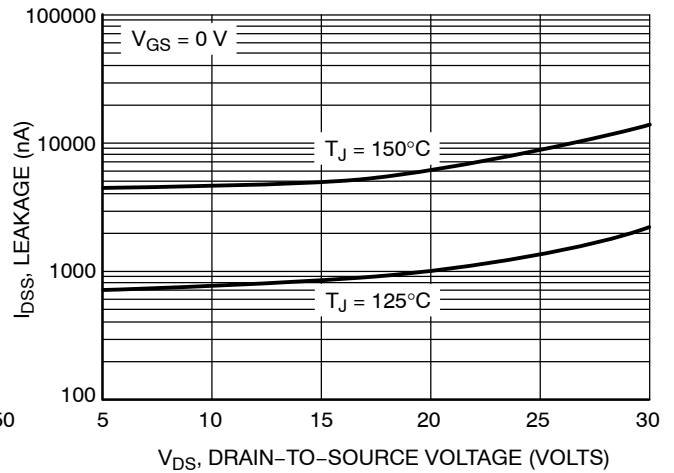


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL PERFORMANCE CURVES

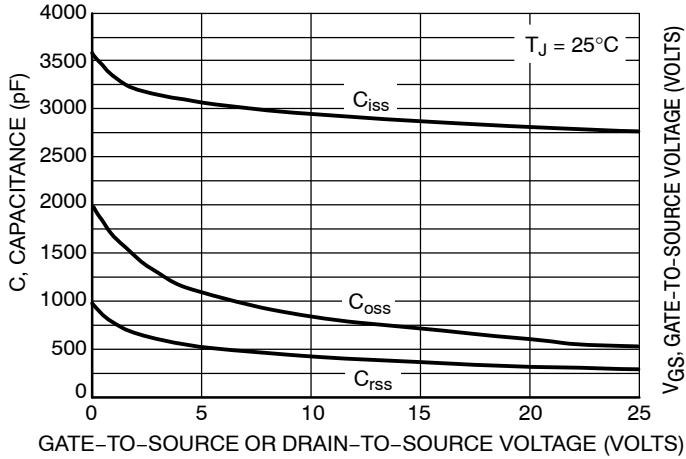


Figure 7. Capacitance Variation

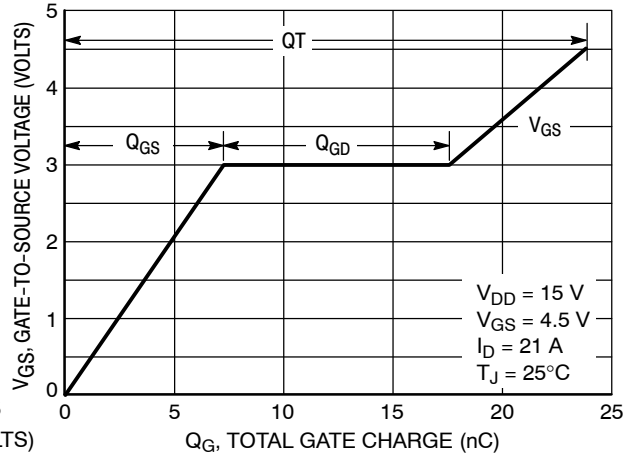


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

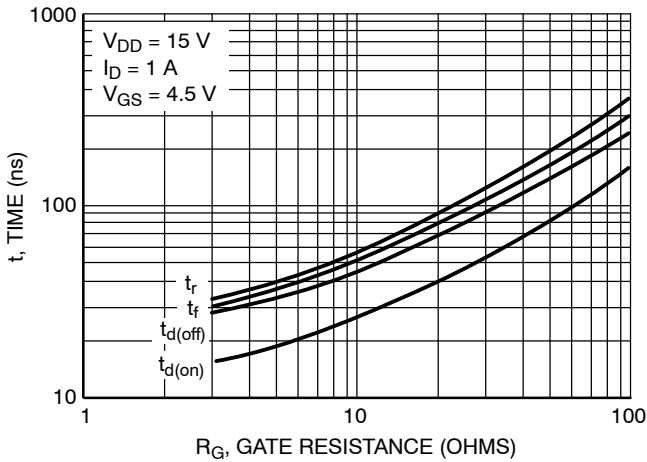


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

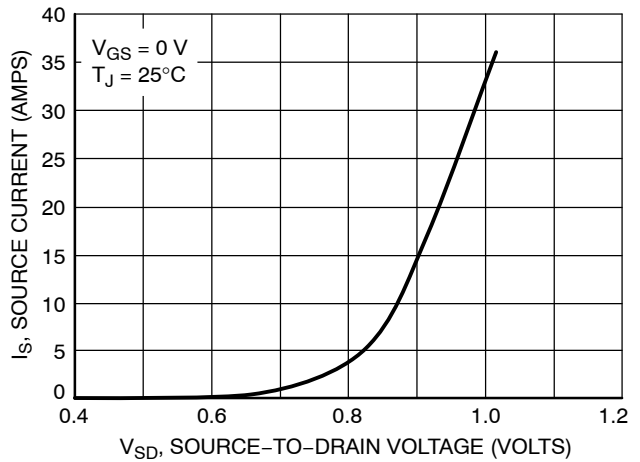


Figure 10. Diode Forward Voltage vs. Current

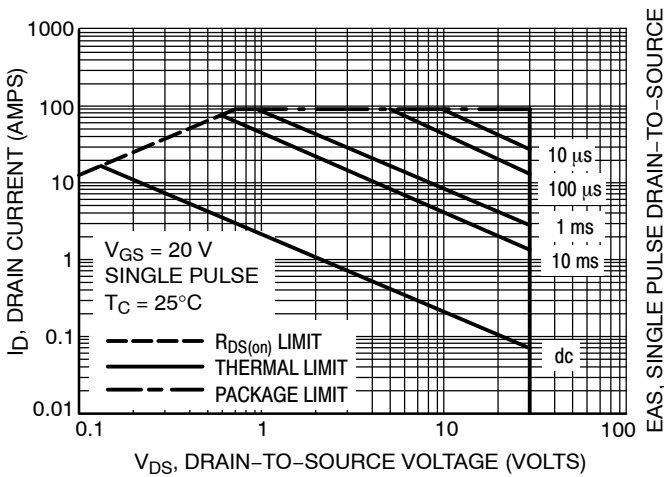


Figure 11. Maximum Rated Forward Biased Safe Operating Area

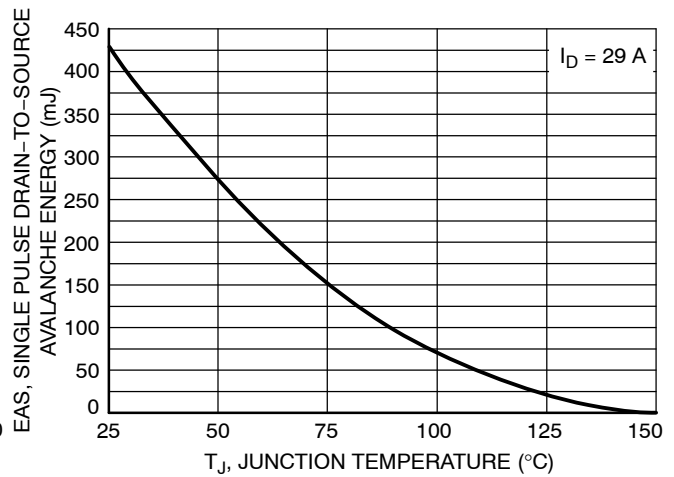


Figure 12. Maximum Avalanche Energy vs Starting Junction Temperature

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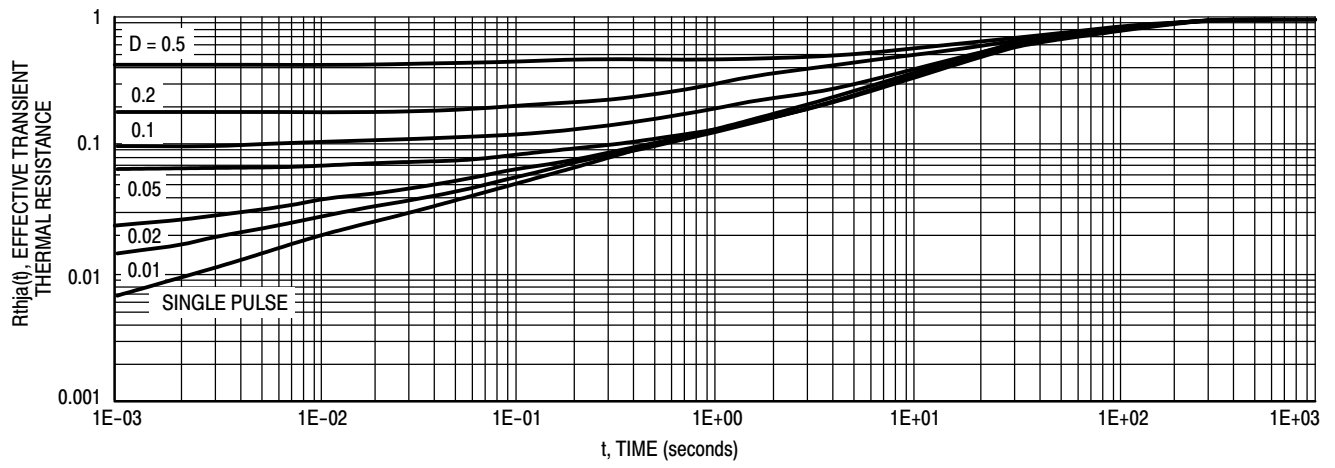


Figure 13. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:

- PIN 1. SOURCE
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN

STYLE 2:

- PIN 1. ANODE
- 2. ANODE
- 3. ANODE
- 4. NO CONNECT
- 5. CATHODE

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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