NTMFD4C20N

MOSFET – Power, Dual, N-Channel, SO8FL

30 V, High Side 18 A / Low Side 27 A

Features

- Co−Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC−DC Converters
- System Voltage Rails
- Point of Load

ON Semiconductor®

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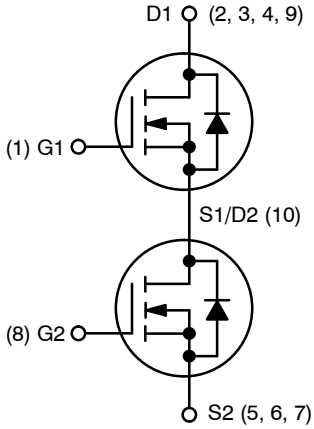
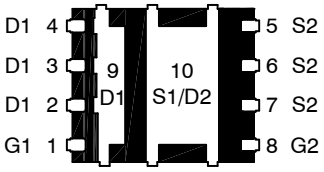
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1 Top FET 30 V	7.3 mΩ @ 10 V	18 A
	10.8 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	3.4 mΩ @ 10 V	27 A
	5.2 mΩ @ 4.5 V	

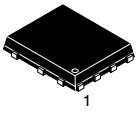


PIN CONNECTIONS

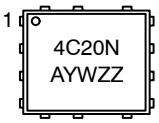


(Bottom View)

MARKING DIAGRAM



DFN8
CASE 506BX



4C20N	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter				Symbol	Value	Unit
Drain−to−Source Voltage			Q1	V_{DSS}	30	V
Drain−to−Source Voltage			Q2			
Gate−to−Source Voltage			Q1	V_{GS}	±20	V
Gate−to−Source Voltage			Q2			
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	Q1	I_D	12	A
		T_A = 85°C			8.6	
		T_A = 25°C	Q2		18	
		T_A = 85°C			13	
Power Dissipation RθJA (Note 1)		T_A = 25°C	Q1	P_D	1.88	W
			Q2		1.97	
Continuous Drain Current $R_{\theta JA} \le 10$ s (Note 1)		T_A = 25°C	Q1	I_D	18.2	A
		T_A = 85°C			13.1	
		T_A = 25°C	Q2		27.4	
		T_A = 85°C			19.8	
Power Dissipation $R_{\theta JA} \le 10$ s (Note 1)		T_A = 25°C	Q1	P_D	4.37	W
			Q2		4.6	
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	Q1	I_D	9.1	A
		T_A = 85°C			6.6	
		T_A = 25°C	Q2		13.7	
		T_A = 85°C			9.9	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25 °C	Q1	P_D	1.09	W
			Q2		1.15	
Pulsed Drain Current		TA = 25°C tp = 10 μs	Q1	I_{DM}	55	A
			Q2		82	
Operating Junction and Storage Temperature			Q1	T_J, T_{STG}	−55 to +150	°C
			Q2			
Source Current (Body Diode)			Q1	I_S	4.0	A
			Q2		4.2	
Drain to Source DV/DT				dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25C, V_{DD} = 50 V, V_{GS} = 10 V, L = 0.1 mH, R_G = 25 Ω)		I_L = 18 A_{pk}	Q1	EAS	16	mJ
		I_L = 29 A_{pk}	Q2	EAS	42	
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)				T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	FET	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 3)	Q1	$R_{\theta JA}$	66.5	°C/W
	Q2		63.3	
Junction−to−Ambient − Steady State (Note 4)	Q1	$R_{\theta JA}$	114.3	
	Q2		108.7	
Junction−to−Ambient − (t ≤ 10 s) (Note 3)	Q1	$R_{\theta JA}$	28.6	
	Q2		27.2	
Junction−to−Case − (Drain)	Q1	$R_{\theta JC}$	5.4	
	Q2		3.7	

3. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	Q1	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
	Q2		V_{GS} = 0 V, I_D = 1 mA		30			
Drain−to−Source Breakdown Voltage Temperature Coefficient	Q1	$V_{(BR)DSS}/T_J$				14.5		mV/°C
	Q2					12		
Zero Gate Voltage Drain Current	Q1	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1	μA
				T_J = 125°C			10	
	Q2		V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			10	
Gate−to−Source Leakage Current	Q1	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
	Q2						±100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	Q1	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.3		2.1	V
	Q2				1.3		2.1	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)}/T_J$				4.7		mV/°C
	Q2					5.1		
Drain−to−Source On Resistance	Q1	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10 A		5.8	7.3	mΩ
			V_{GS} = 4.5 V	I_D = 10 A		8.7	10.8	
	Q2		V_{GS} = 10 V	I_D = 20 A		2.7	3.4	
			V_{GS} = 4.5 V	I_D = 20 A		4.0	5.2	
Forward Transconductance	Q1	g_{FS}	V_{DS} = 1.5 V, I_D = 10 A			43		S
	Q2					68		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	Q1	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V		970		pF
	Q2				1950		
Output Capacitance	Q1	C_{OSS}			430		
	Q2				990		
Reverse Capacitance	Q1	C_{RSS}			125		
	Q2				50		
Total Gate Charge	Q1	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 10 A		9.3		nC
	Q2				13		
Threshold Gate Charge	Q1	$Q_{G(TH)}$			1.6		
	Q2				3.3		
Gate−to−Source Charge	Q1	Q_{GS}			3.3		
	Q2				6.0		
Gate−to−Drain Charge	Q1	Q_{GD}			4.2		
	Q2				3.0		
Total Gate Charge	Q1	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 10 A		19		nC
	Q2				29		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	Q1	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		9.0		ns
	Q2				11		
Rise Time	Q1	t_r			33		
	Q2				32		
Turn−Off Delay Time	Q1	$t_{d(OFF)}$			15		
	Q2				20		
Fall Time	Q1	t_f			5.0		
	Q2				5.0		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	Q1	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		6.0		ns
	Q2				8.0		
Rise Time	Q1	t_r			26		
	Q2				26		
Turn−Off Delay Time	Q1	$t_{d(OFF)}$			18		
	Q2				25		
Fall Time	Q1	t_f			4.0		
	Q2				4.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Voltage	Q1	V_{SD}	V_{GS} = 0 V, I_S = 3 A, T_J = 25°C		0.75	1.0	V
			V_{GS} = 0 V, I_S = 3 A, T_J = 125°C		0.62		
	Q2		V_{GS} = 0 V, I_S = 3 A, T_J = 25°C		0.45	0.70	
			V_{GS} = 0 V, I_S = 3 A, T_J = 125°C		0.37		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	Q1	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 30 A		23		ns
	Q2				38		
Charge Time	Q1	ta			11.6		
	Q2				18.6		
Discharge Time	Q1	tb			11.4		
	Q2				19.4		
Reverse Recovery Charge	Q1	Q_{RR}			10		nC
	Q2				25		
PACKAGE PARASITIC VALUES							
Source Inductance	Q1	L_S	T_A = 25°C		0.38		nH
	Q2				0.65		
Drain Inductance	Q1	L_D			0.054		nH
	Q2				0.007		
Gate Inductance	Q1	L_G			1.5		nH
	Q2				1.5		
Gate Resistance	Q1	R_G		0.3	1.0	2.0	Ω
	Q2			0.3	1.0	2.0	

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTMFD4C20NT1G	DFN8 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS – Q1

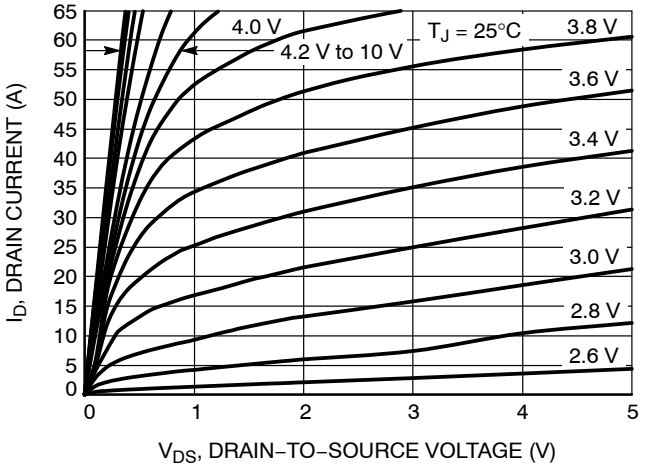


Figure 1. On−Region Characteristics

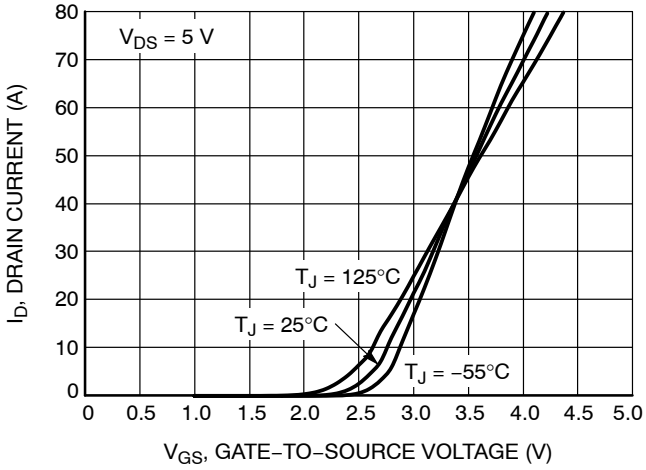


Figure 2. Transfer Characteristics

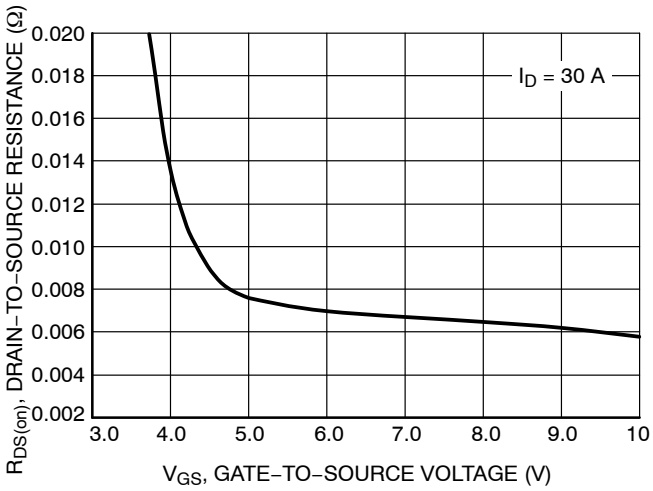


Figure 3. On−Resistance vs. V_{GS}

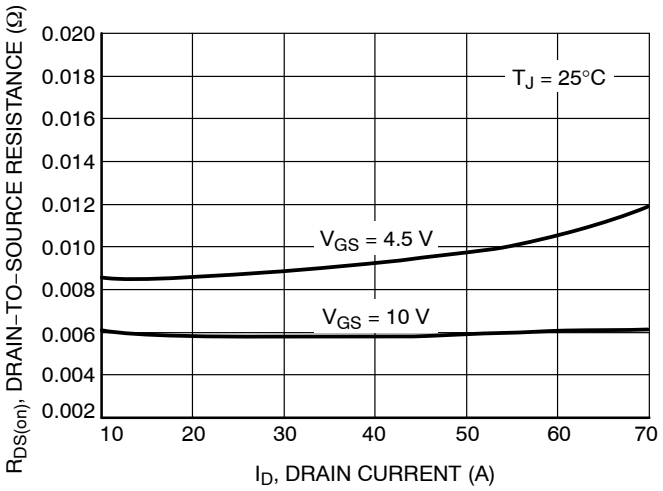


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

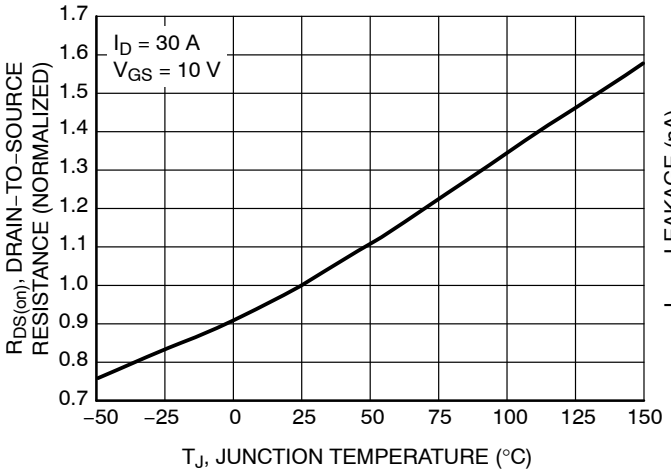


Figure 5. On−Resistance Variation with Temperature

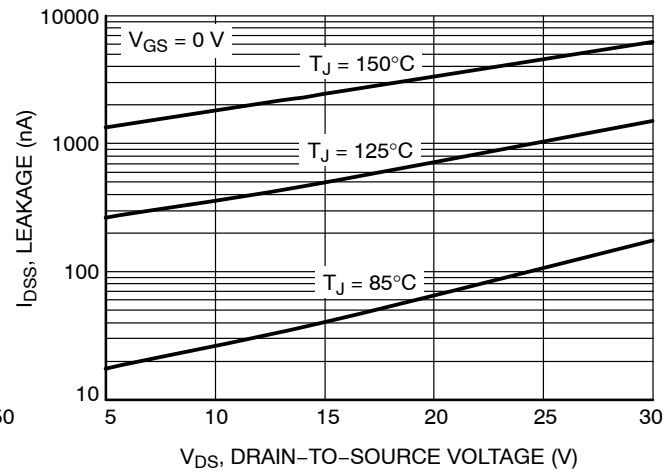


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q1

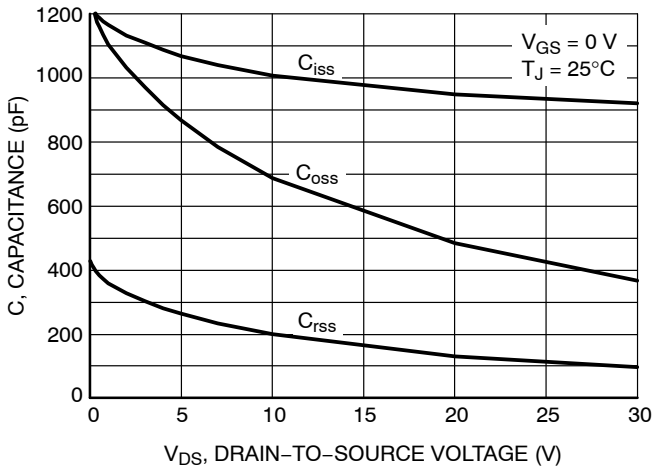


Figure 7. Capacitance Variation

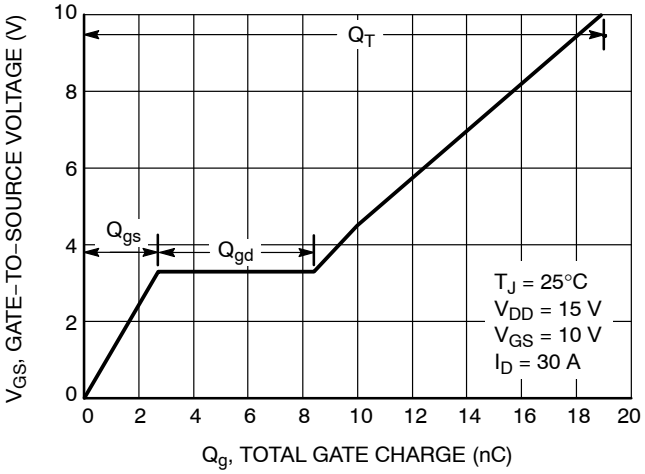


Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

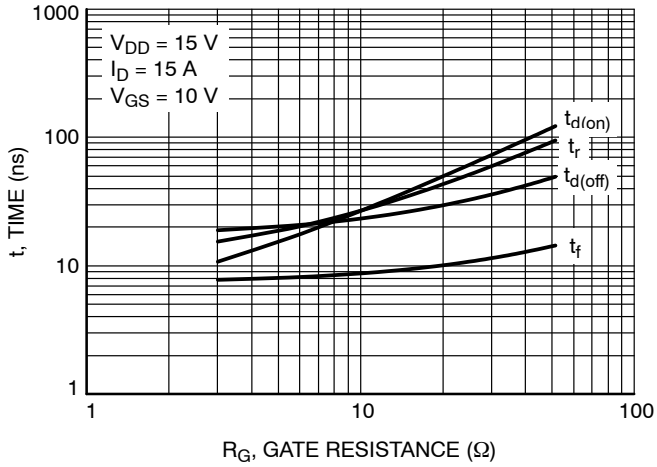


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

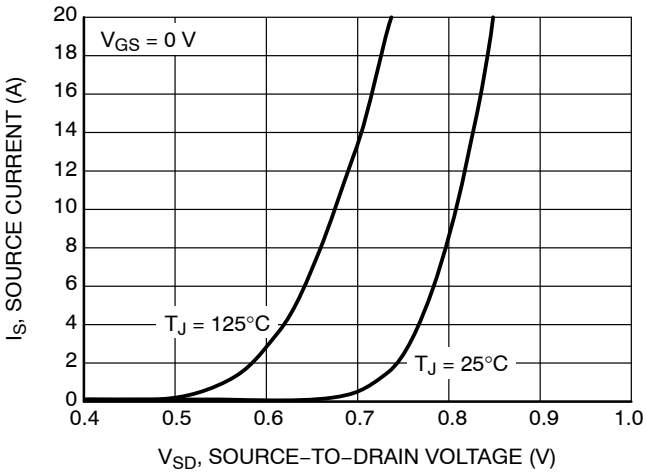


Figure 10. Diode Forward Voltage vs. Current

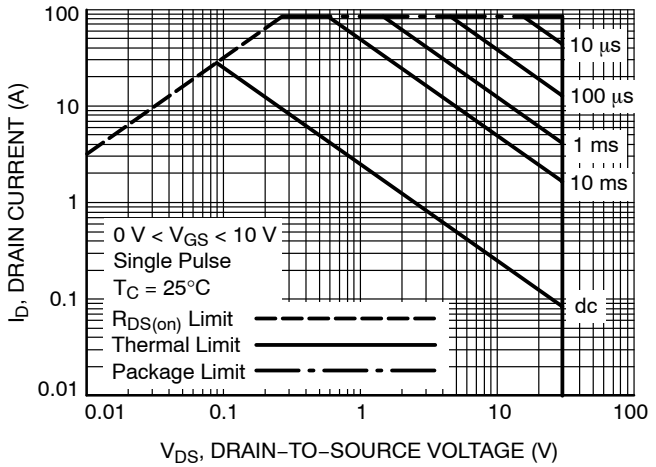


Figure 11. Maximum Rated Forward Biased Safe Operating Area

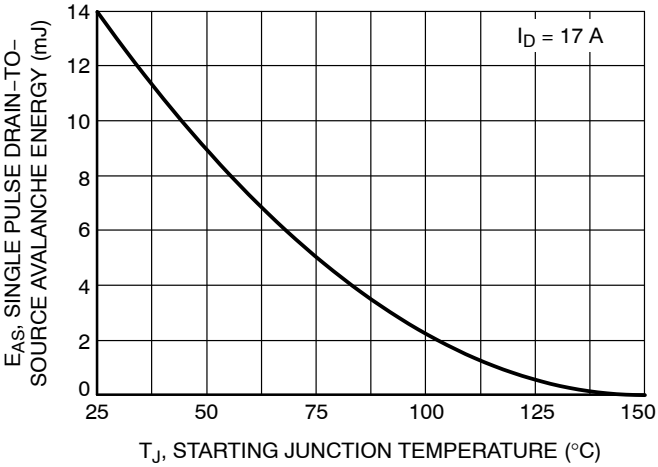


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS – Q1

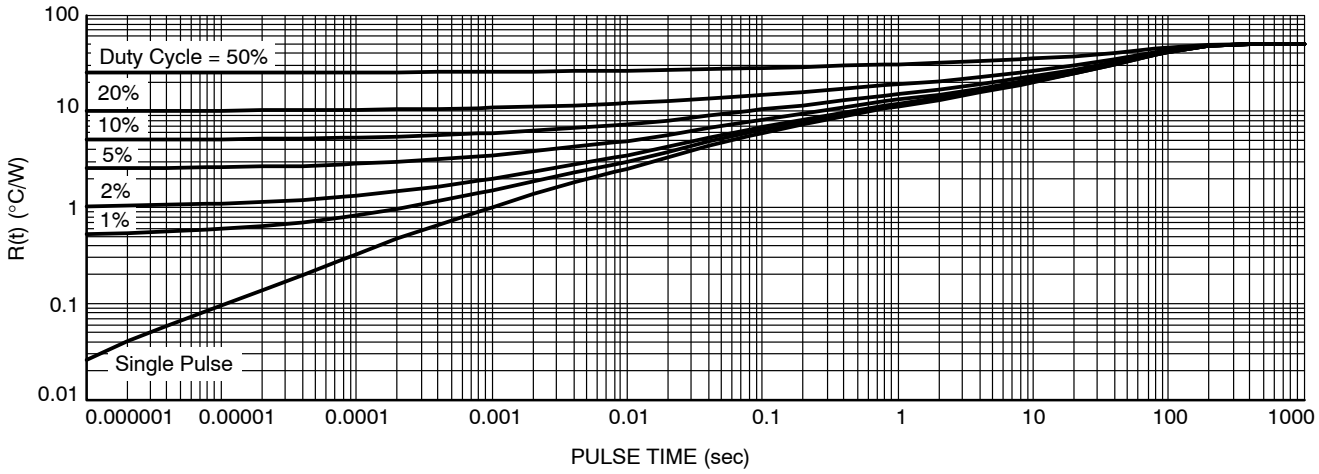


Figure 13. Thermal Response

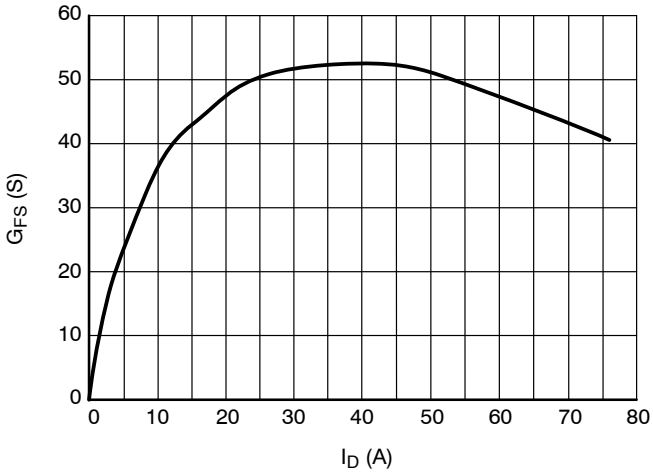


Figure 14. G_{FS} vs. I_D

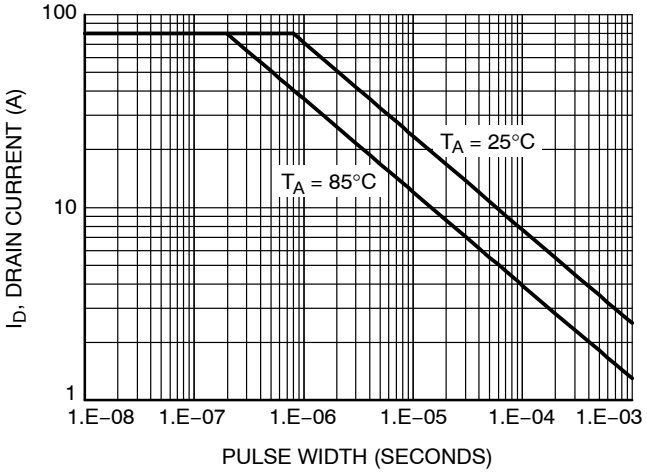


Figure 15. Avalanche Characteristics

TYPICAL CHARACTERISTICS – Q2

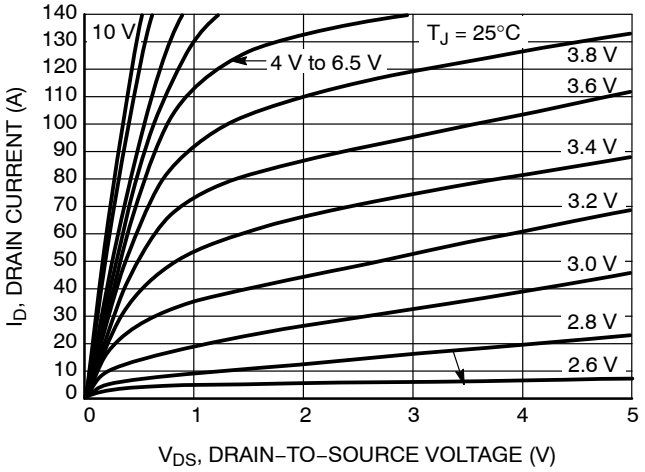


Figure 16. On−Region Characteristics

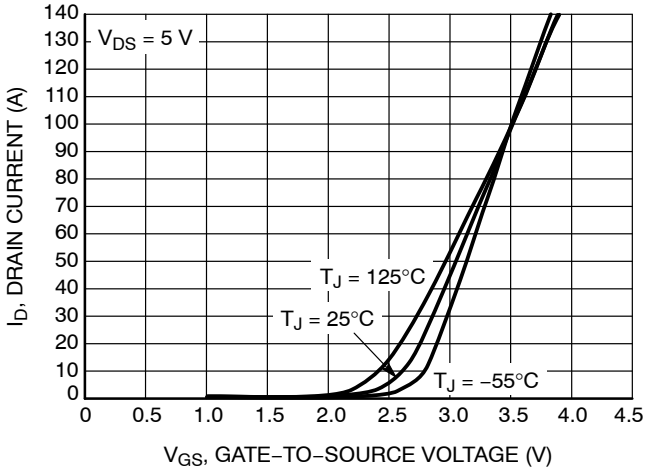


Figure 17. Transfer Characteristics

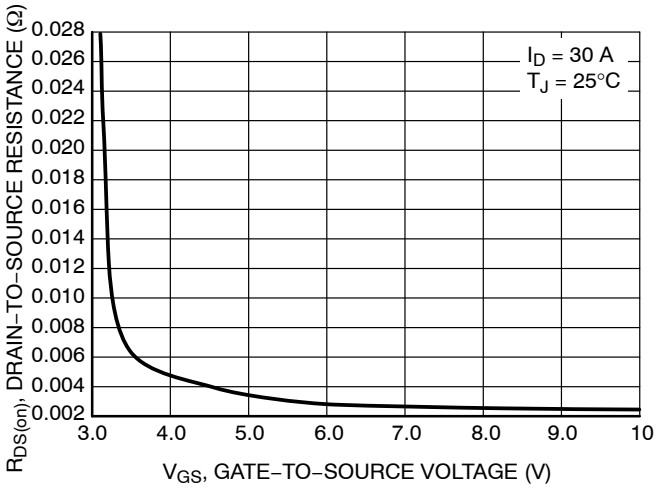


Figure 18. On−Resistance vs. V_{GS}

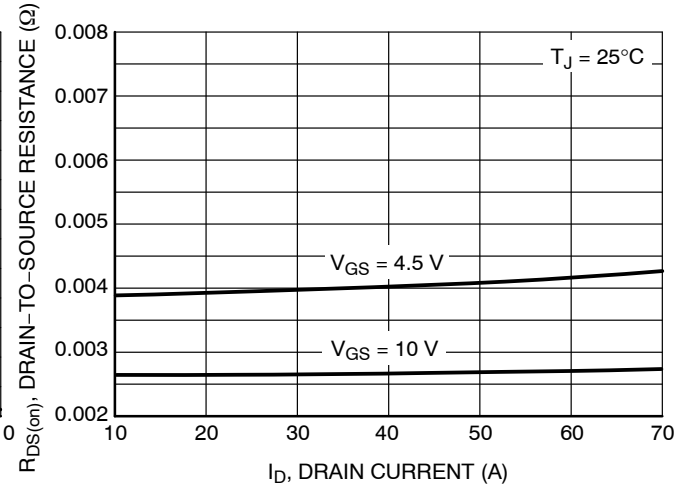


Figure 19. On−Resistance vs. Drain Current and Gate Voltage

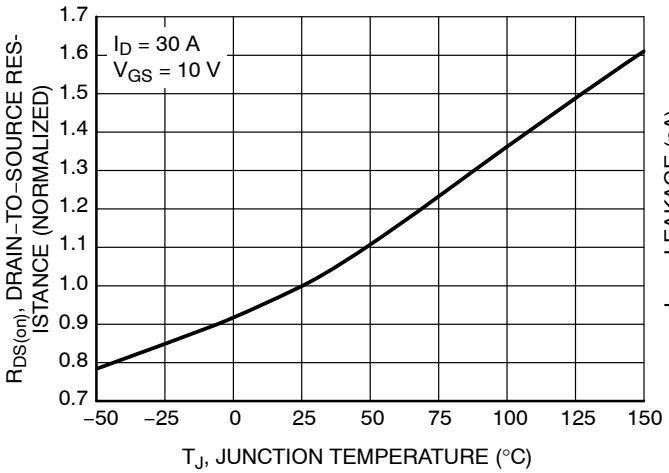


Figure 20. On−Resistance Variation with Temperature

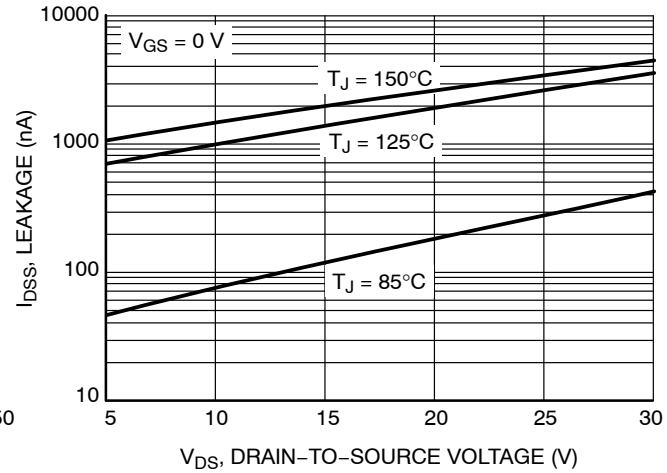


Figure 21. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

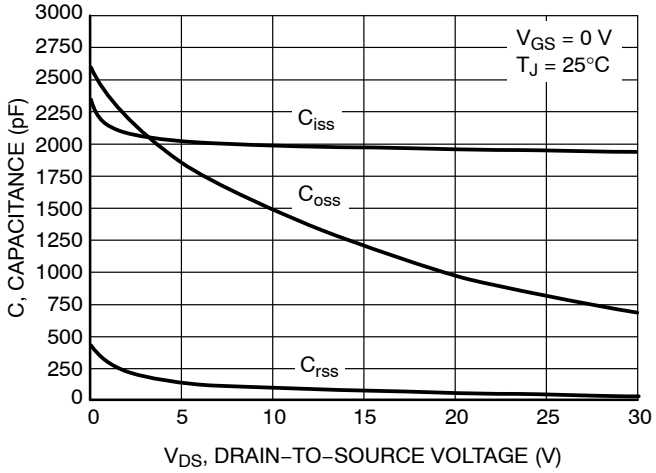


Figure 22. Capacitance Variation

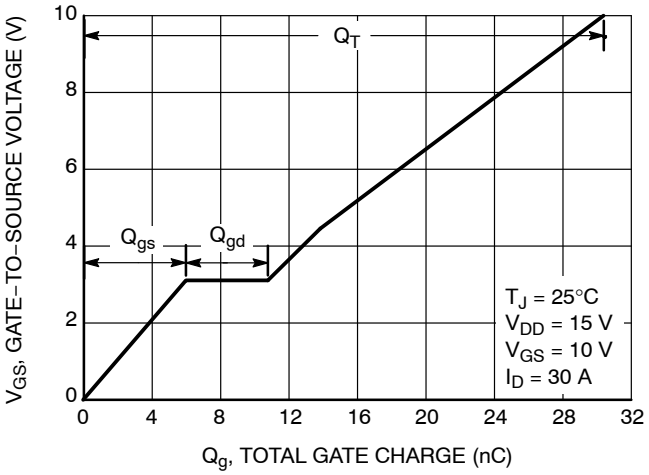


Figure 23. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

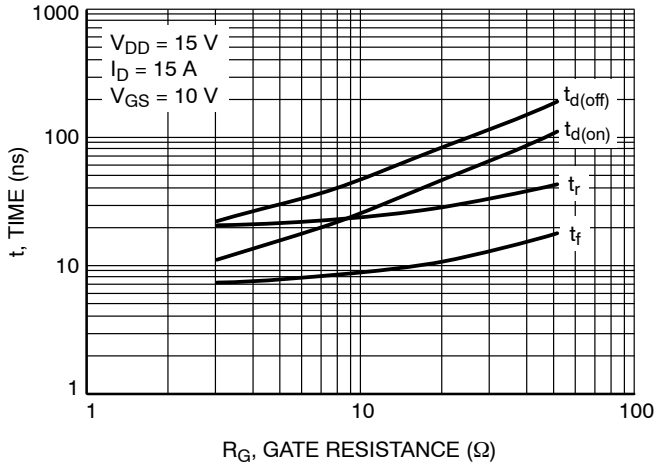


Figure 24. Resistive Switching Time Variation vs. Gate Resistance

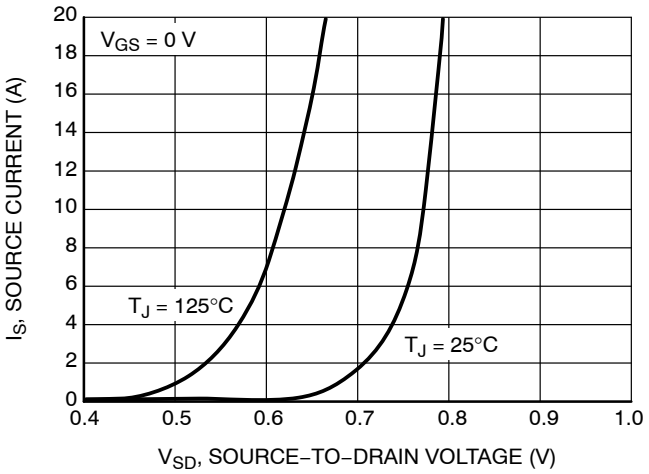


Figure 25. Diode Forward Voltage vs. Current

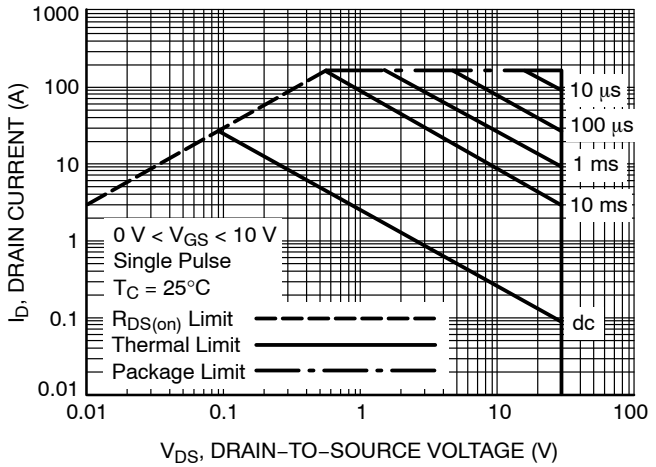


Figure 26. Maximum Rated Forward Biased Safe Operating Area

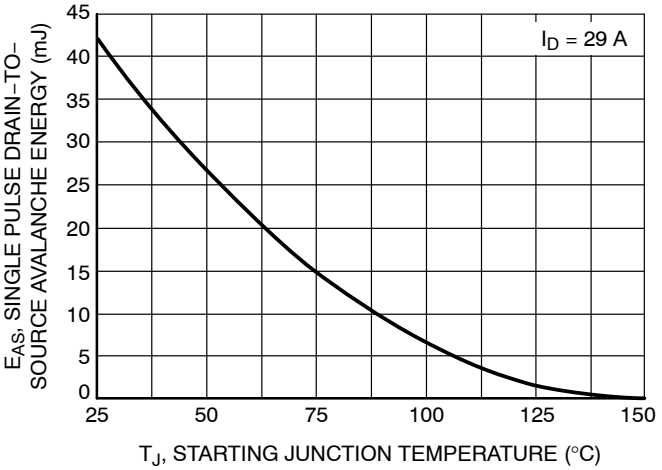


Figure 27. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS – Q2

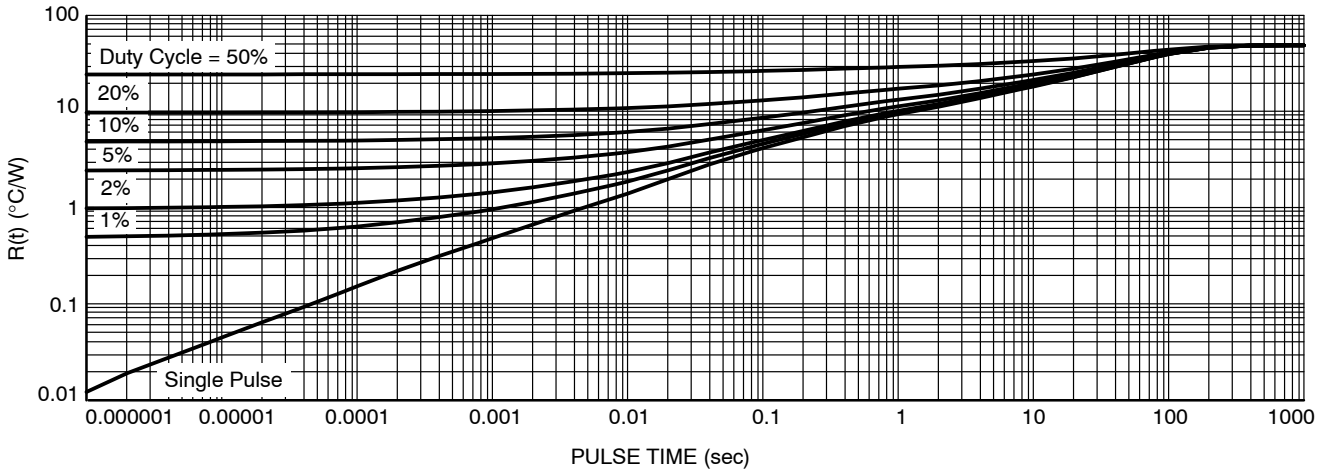


Figure 28. Thermal Response

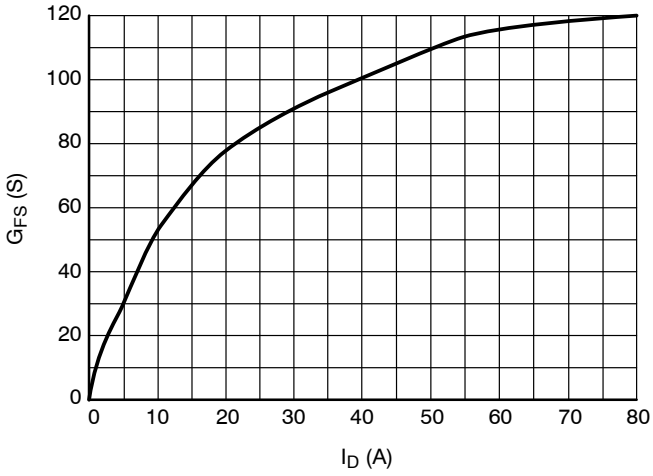


Figure 29. G_{FS} vs. I_D

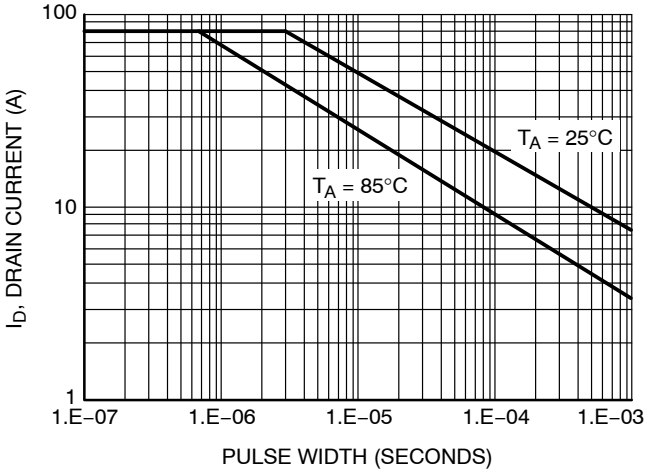


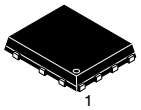
Figure 30. Avalanche Characteristics

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

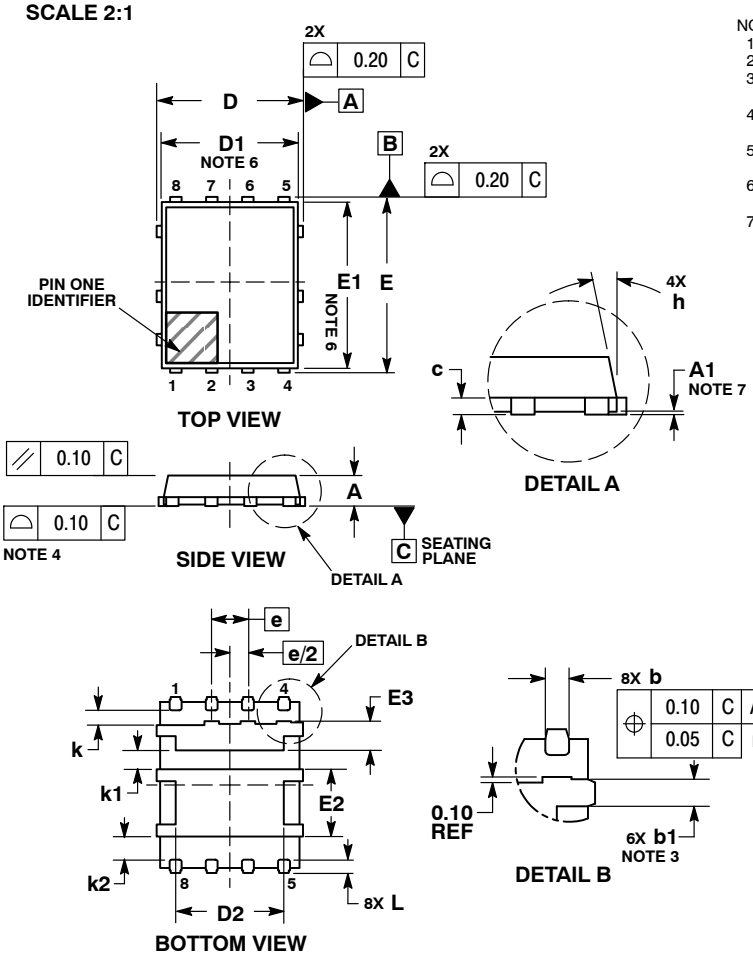
ON Semiconductor®

DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual−Asymmetrical)
CASE 506BX
ISSUE D

DATE 24 JUN 2014



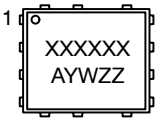
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS b AND L ARE MEASURED AT THE PACKAGE SURFACE
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
7. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.41	0.61
b1	0.41	0.61
c	0.23	0.33
D	5.00	5.30
D1	4.50	5.10
D2	3.50	4.22
E	6.00	6.30
E1	5.50	6.10
E2	2.27	2.67
E3	0.82	1.22
e	1.27 BSC	
h	---	12 °
k	0.39	0.59
k1	0.56	0.76
k2	0.73	0.93
L	0.35	0.55

GENERIC MARKING DIAGRAM*

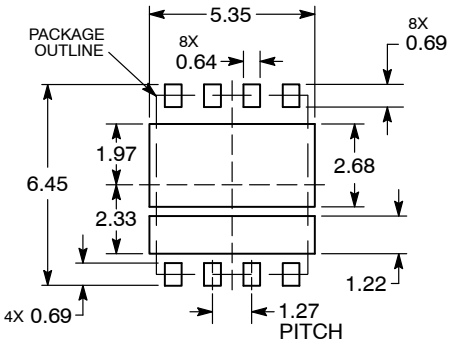


XXXXXX= Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.

STYLE 1:
PIN 1. GATE 1
2. DRAIN 1
3. DRAIN 1
4. DRAIN 1
5. SOURCE 2
6. SOURCE 2
7. SOURCE 2
8. GATE 2
9. DRAIN 1
10. SOURCE 1/DRAIN 2

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN8 5X6, 1.27P DUAL FLAG (SO8FL−DUAL−ASYMMETRICAL)**	**PAGE 1 OF 1**

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