

NTMFD0D9N02P1E

MOSFET – Power, Dual, N-Channel, Power Trench, Power Clip, Asymmetric

30 V / 25 V

Features

- Small Footprint (5x6mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Designed with Low R_g for Fast Switching Applications
- These are Pb-free, Halogen Free / BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Converters
- System Voltage Rails
- General Purpose Point of Load

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Sym- bol	Q1	Q2	Unit	
Drain-to-Source Voltage		V_{DS}	30	25	V	
Gate-to-Source Voltage		V_{GS}	+16V -12V	+16V -12V	V	
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	77	180	A
		$T_C = 85^\circ\text{C}$		56	130	
Power Dissipation $R_{\theta JC}$ (Note 3)		$T_A = 25^\circ\text{C}$	P_D	29.2	37.4	W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	21	44	A
		$T_A = 85^\circ\text{C}$		15	32	
Power Dissipation $R_{\theta JA}$ (Note 1, 3)		$T_A = 25^\circ\text{C}$	P_D	2.1	2.3	W
Continuous Drain Current $R_{\theta JA}$ (Note 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	14	30	A
		$T_A = 85^\circ\text{C}$		10	21	
Power Dissipation $R_{\theta JA}$ (Note 2, 3)		$T_A = 25^\circ\text{C}$	P_D	0.96	1.04	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM}	356	1023	A	
Single Pulse Drain-to-Source Avalanche Energy Q1: $I_L = 10 \text{ A}_{pk}$, $L = 3 \text{ mH}$ (Note 4) Q2: $I_L = 20 \text{ A}_{pk}$, $L = 3 \text{ mH}$ (Note 4)		E_{AS}	150	600	mJ	
Operating Junction and Storage Temperature		T_J , T_{stg}	-55 to 150		$^\circ\text{C}$	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T_L	260		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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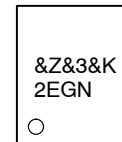
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FET	$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
Q1	30 V	3.0 m Ω @ 10 V	77 A
		3.8 m Ω @ 4.5 V	
Q2	25 V	0.72 m Ω @ 10 V	180 A
		0.95 m Ω @ 4.5 V	



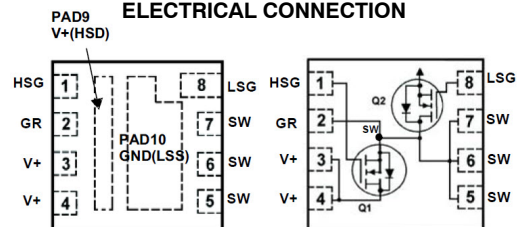
PQFN8
POWER CLIP
CASE 483AR

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = Numeric Date Code
- &K = Lot Code
- 2EGN = Specific Device Code

ELECTRICAL CONNECTION



ORDERING INFORMATION

Device	Package	Shipping†
NTMFD0D9N02P1E	PQFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFD0D9N02P1E

Table 1. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Q1 Max	Q2 Max	Units
Junction-to-Case – Steady State (Note 1, 3)	$R_{\theta JC}$	4.3	3.3	°C/W
Junction-to-Ambient – Steady State (Note 1, 3)	$R_{\theta JA}$	60	55	
Junction-to-Ambient – Steady State (Note 2, 3)	$R_{\theta JA}$	130	120	

- Surface-mounted on FR4 board using 1 in² pad size, 2 oz Cu pad.
- Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. RQCA is determined by the user's board design.
- Q1 100% UIS tested at L = 0.1 mH, I_{AS} = 21 A.
Q2 100% UIS tested at L = 0.1 mH, I_{AS} = 45 A.

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	Q1	30			V
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	Q2	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J	I _D = 1 mA, ref to 25°C	Q1		18		mV/°C
		I _D = 1 mA, ref to 25°C	Q2		16		
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C	Q1		10	μA
		V _{GS} = 0 V, V _{DS} = 20 V		Q2		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = +16 V / -12 V	Q1			±100	nA
		V _{DS} = 0 V, V _{GS} = +16 V / -12 V	Q2			±100	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 340 μA	Q1	1.2	1.6	2.0	V
		V _{GS} = V _{DS} , I _D = 1 mA	Q2	1.2	1.5	2.0	
Threshold Temperature Coefficient	V _{GS(TH)} / T _J	I _D = 340 μA, ref to 25°C	Q1		-4.4		mV/°C
		I _D = 1 mA, ref to 25°C	Q2		-5.1		
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	Q1		2.5	3.0	mΩ
		V _{GS} = 4.5 V, I _D = 18 A			3.0	3.8	
		V _{GS} = 10 V, I _D = 41 A	Q2		0.60	0.72	
		V _{GS} = 4.5 V, I _D = 37 A			0.75	0.95	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 20 A	Q1		147		
		V _{DS} = 5 V, I _D = 41 A	Q2		311		
Gate Resistance	R _G	T _A = 25°C	Q1		0.4		Ω
			Q2		0.4		

CHARGES & CAPACITANCES

Input Capacitance	C _{ISS}	Q1: V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz Q2: V _{GS} = 0 V, V _{DS} = 13 V, f = 1 MHz	Q1		1400		pF
			Q2		5050		
Output Capacitance	C _{OSS}		Q1		421		pF
			Q2		1355		
Reverse Capacitance	C _{RSS}		Q1		22		pF
			Q2		94		

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
- Switching characteristics are independent of operating junction temperatures

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Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit	
CHARGES & CAPACITANCES								
Total Gate Charge	$Q_{G(TOT)}$	Q1: $V_{GS} = 4.5\text{V}$, $V_{DS} = 15\text{V}$, $I_D = 20\text{A}$ Q2: $V_{GS} = 4.5\text{V}$, $V_{DS} = 13\text{V}$, $I_D = 41\text{A}$	Q1		9		nC	
			Q2		30			
Gate-to-Drain Charge	Q_{GD}		Q1		2		nC	
			Q2		6			
Gate-to-Source Charge	Q_{GS}		Q1		4		nC	
			Q2		13			
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 15\text{V}$, $I_D = 20\text{A}$	Q1		19		nC	
		$V_{GS} = 10\text{V}$, $V_{DS} = 13\text{V}$, $I_D = 41\text{A}$	Q2		67			
SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{V}$ (Note 6)								
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{V}$ Q1: $I_D = 20\text{A}$, $V_{DD} = 15\text{V}$, $R_G = 6\Omega$ Q2: $I_D = 41\text{A}$, $V_{DD} = 13\text{V}$, $R_G = 6\Omega$	Q1		8		ns	
			Q2		15			
Rise Time	$t_r(ON)$		Q1		2		ns	
			Q2		4			
Turn-Off Delay Time	$t_{d(OFF)}$		Q1		25		ns	
			Q2		70			
Fall Time	t_f		Q1		3		ns	
			Q2		10			
SOURCE-TO-DRAIN DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}		$V_{GS} = 0\text{V}$, $I_S = 20\text{A}$	$T_J = 25^\circ\text{C}$	Q1		0.8	1.2
		$T_J = 125^\circ\text{C}$				0.68		
		$V_{GS} = 0\text{V}$, $I_S = 41\text{A}$	$T_J = 25^\circ\text{C}$	Q2		0.8	1.2	
			$T_J = 125^\circ\text{C}$			0.64		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{V}$, Q1: $I_S = 20\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$ Q2: $I_S = 41\text{A}$, $di/dt = 300\text{A}/\mu\text{s}$	Q1		26		ns	
	Q2			48				
Reverse Recovery Charge	Q_{RR}		Q1		14		nC	
			Q2		79			

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

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TYPICAL CHARACTERISTICS (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

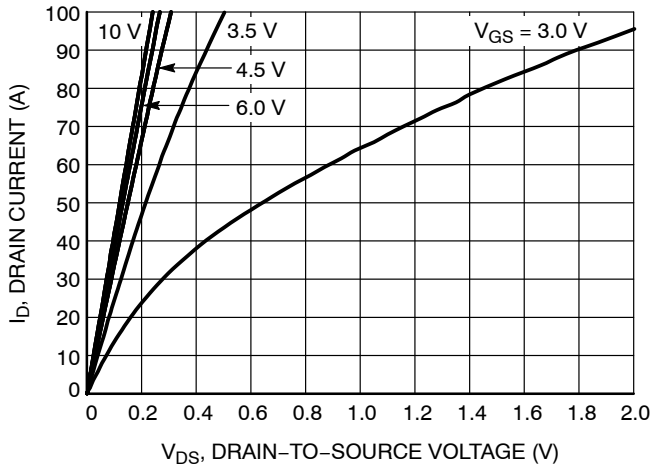


Figure 1. On-Region Characteristics

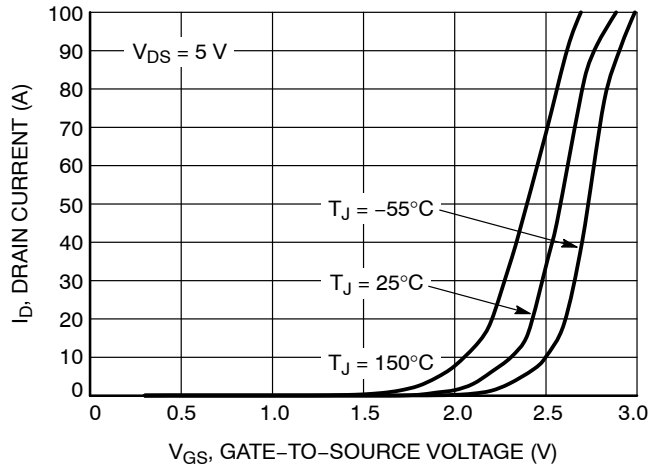


Figure 2. Transfer Characteristics

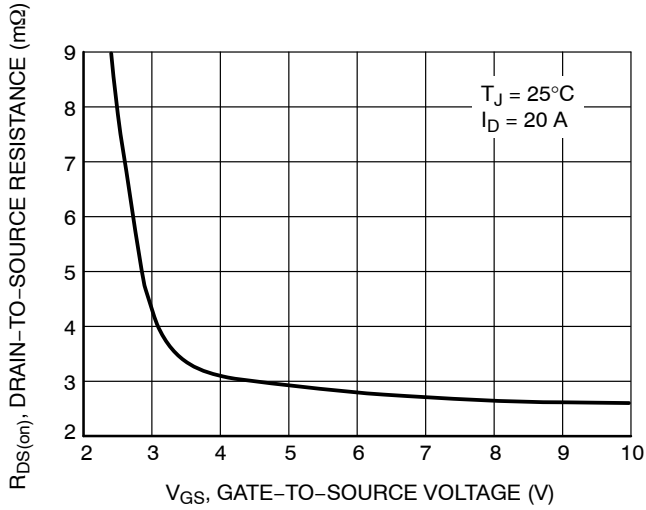


Figure 3. On-Resistance vs. Gate-to-Source Voltage

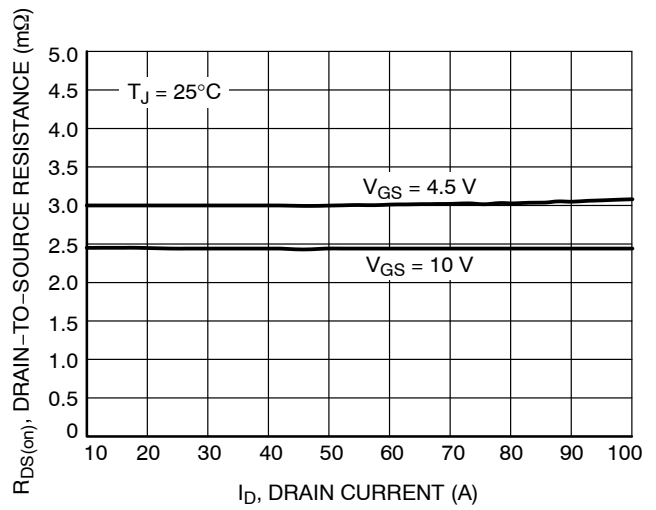


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

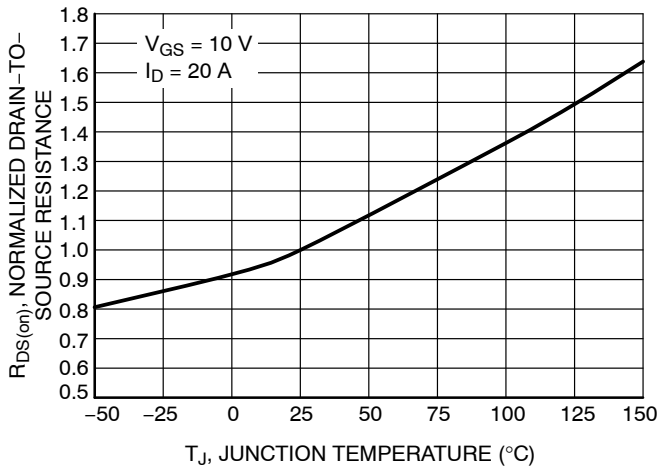


Figure 5. On-Resistance Variation with Temperature

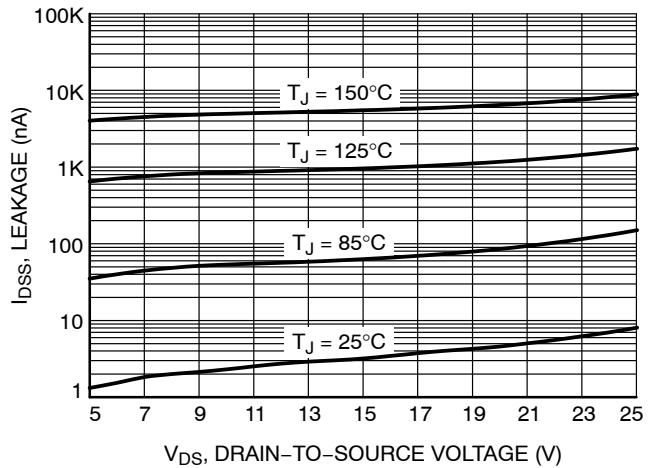


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

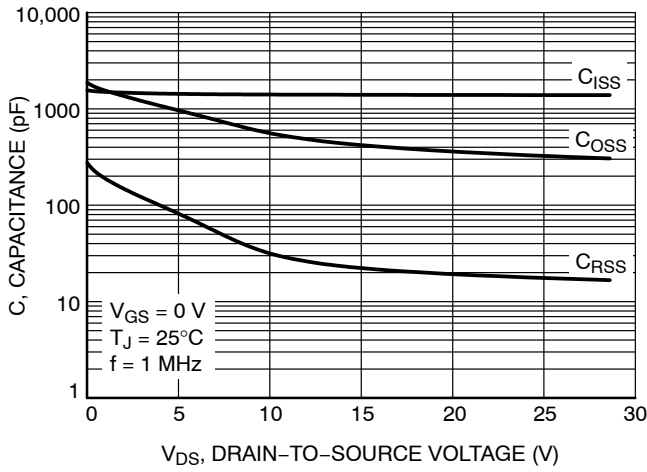


Figure 7. Capacitance Variation

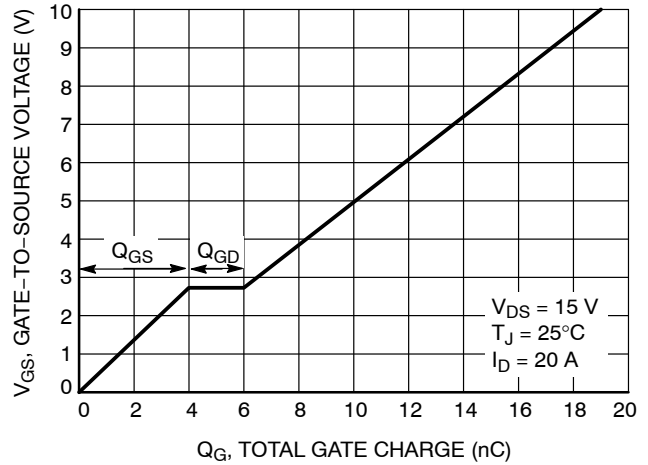


Figure 8. Gate-to-Source Voltage vs. Total Charge

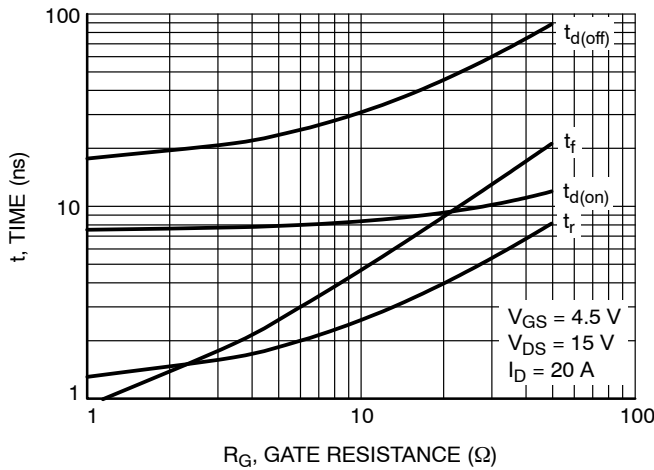


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

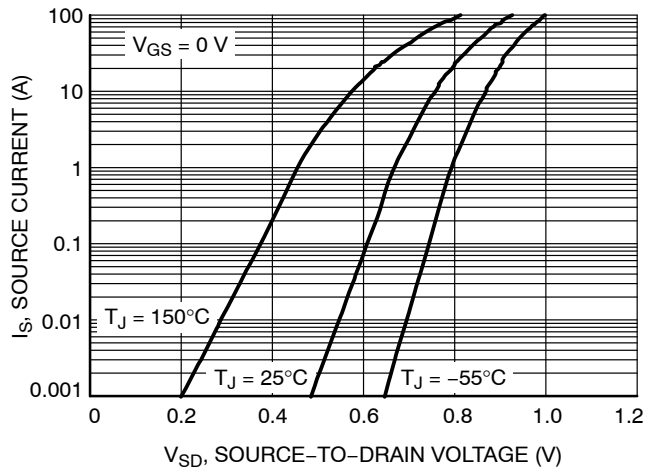


Figure 10. Diode Forward Voltage vs. Current

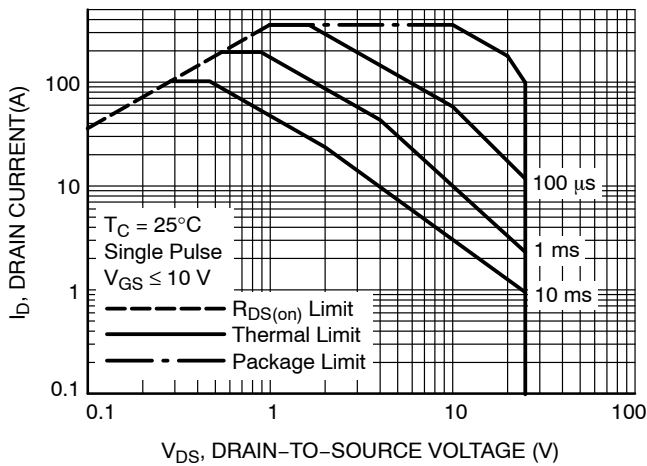


Figure 11. Maximum Rated Forward Biased Safe Operating Area

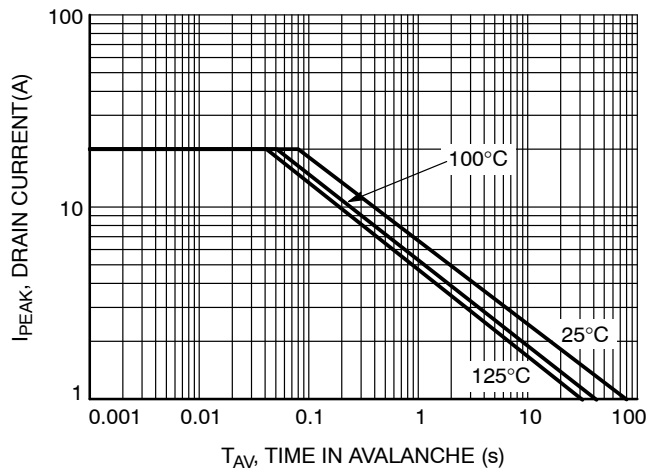


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

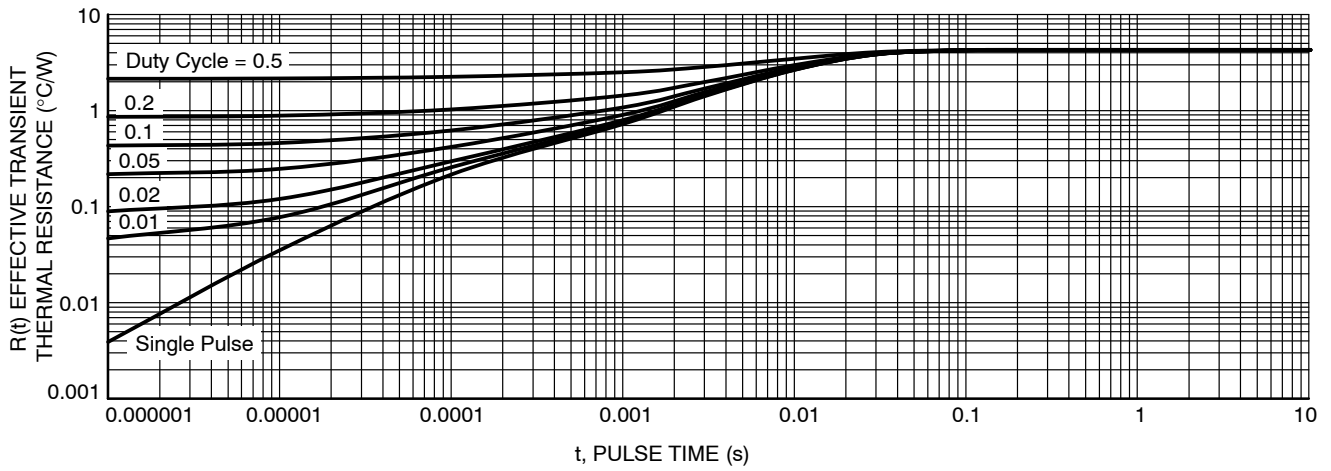


Figure 13. Thermal Response

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TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

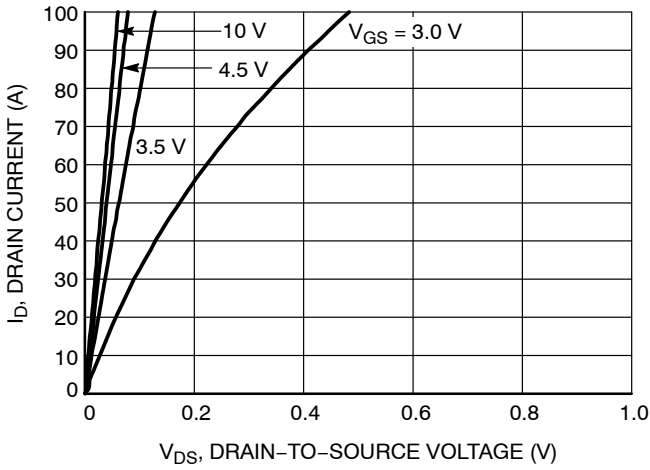


Figure 14. On-Region Characteristics

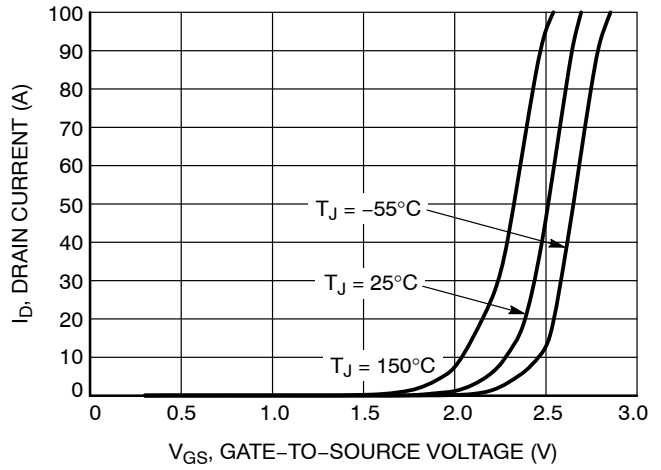


Figure 15. Transfer Characteristics

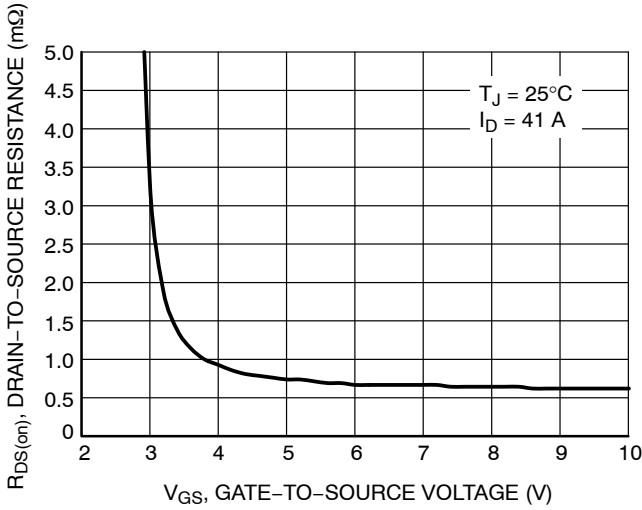


Figure 16. On-Resistance vs. Gate-to-Source Voltage

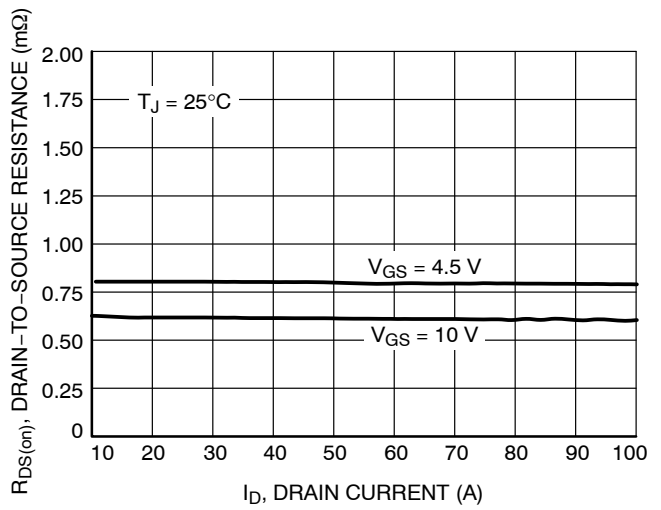


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

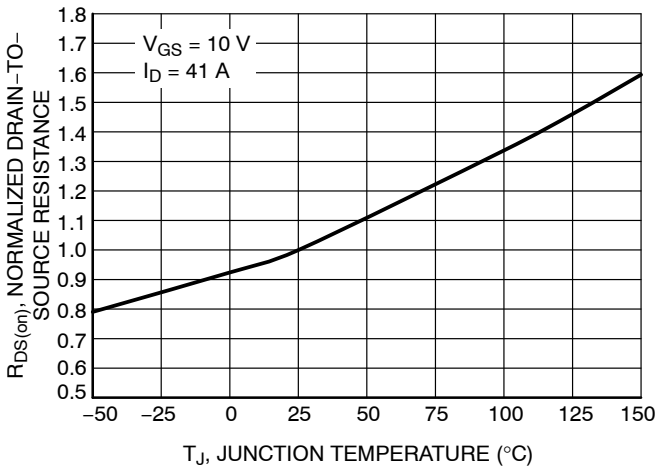


Figure 18. On-Resistance Variation with Temperature

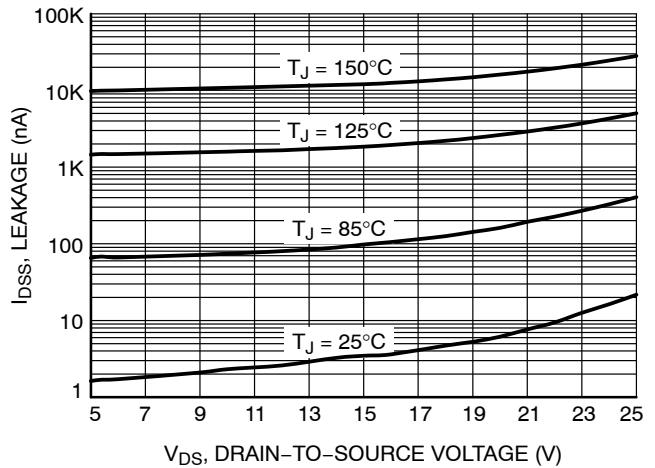


Figure 19. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

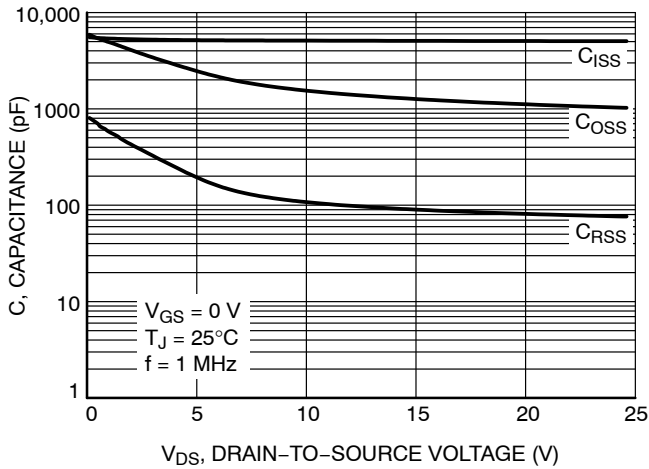


Figure 20. Capacitance Variation

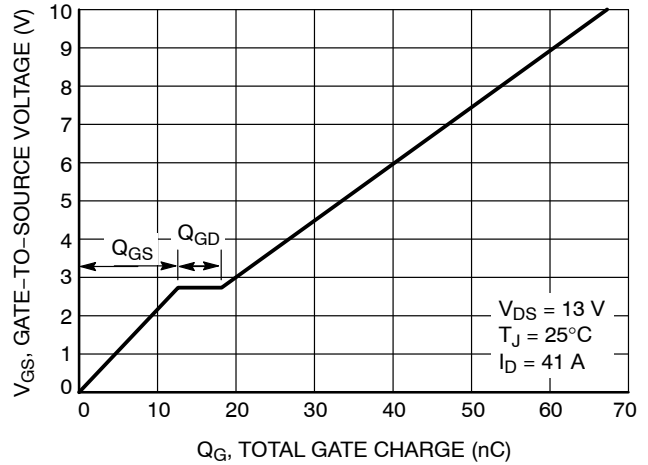


Figure 21. Gate-to-Source Voltage vs. Total Charge

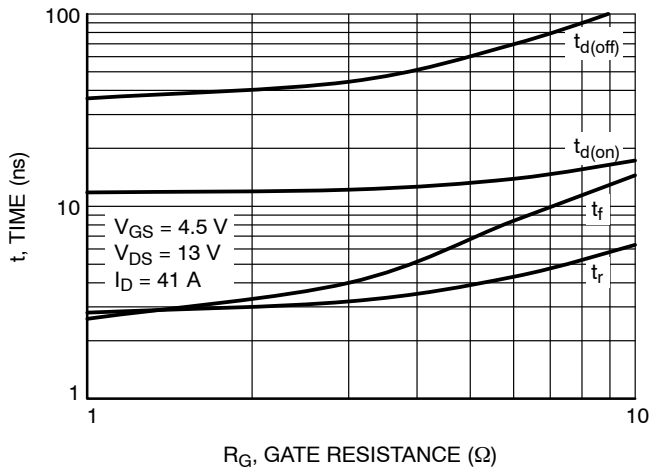


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

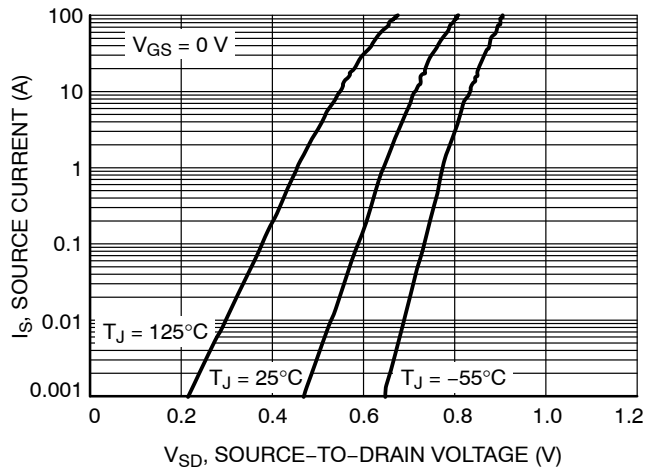


Figure 23. Diode Forward Voltage vs. Current

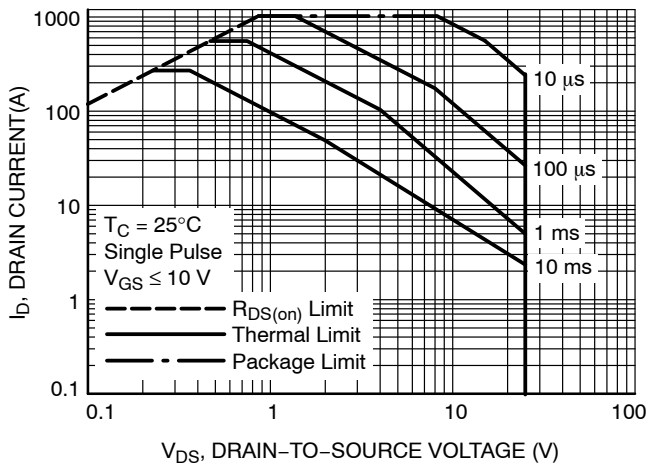


Figure 24. Maximum Rated Forward Biased Safe Operating Area

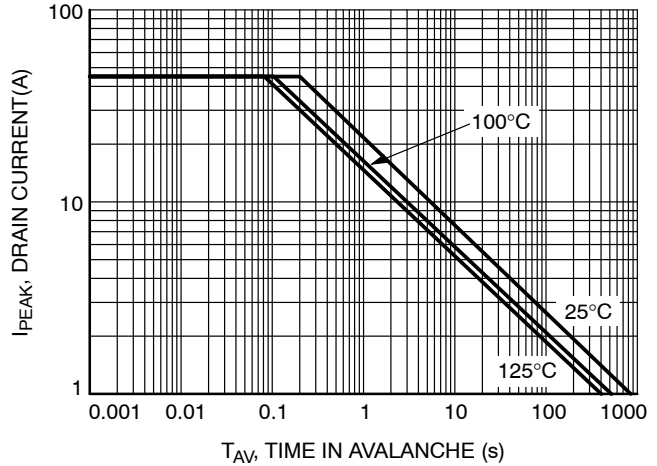


Figure 25. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

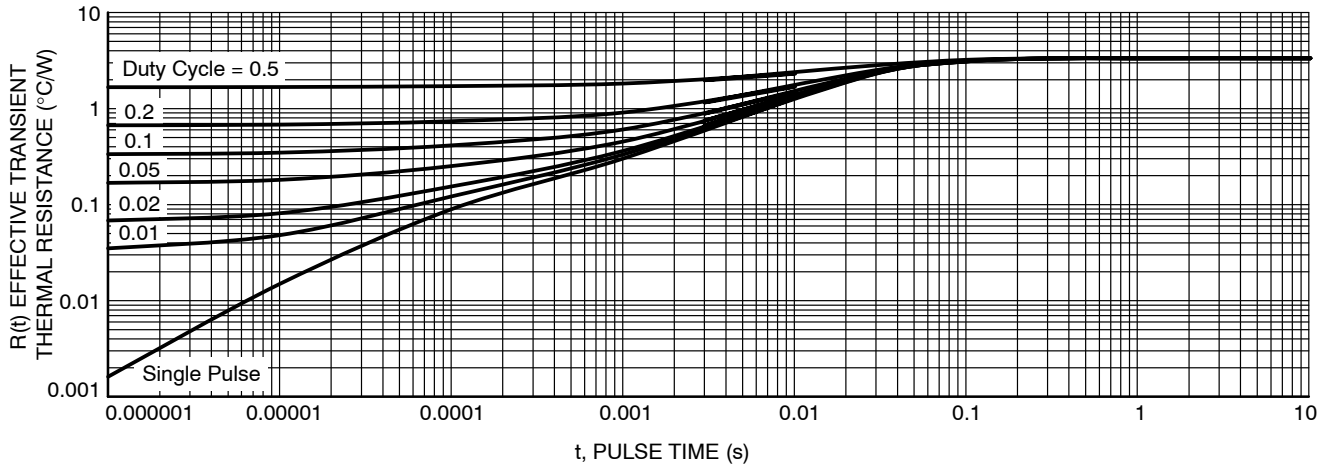
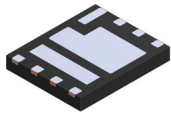


Figure 26. Thermal Response

MECHANICAL CASE OUTLINE

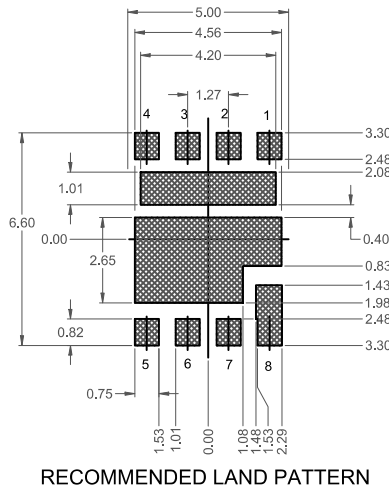
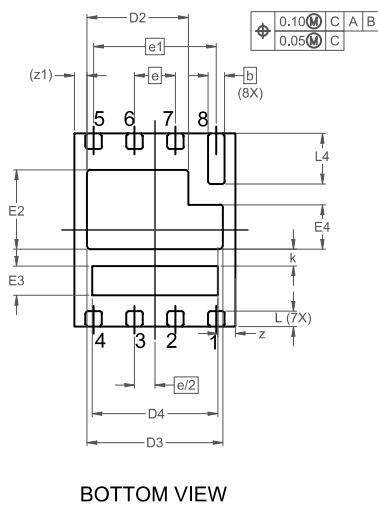
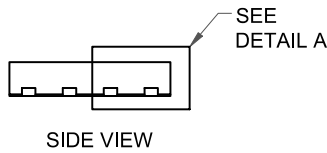
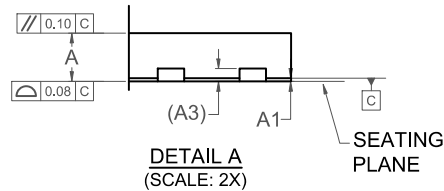
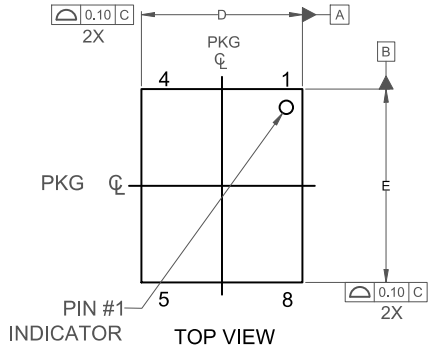
PACKAGE DIMENSIONS

ON Semiconductor®



PQFN8 5x6, 1.27P CASE 483AR ISSUE A

DATE 21 MAY 2021



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.42	0.52	0.62
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5x6, 1.27P	PAGE 1 OF 1

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