

NTLUS4195PZ

Power MOSFET

-30 V, -4.0 A, μ Cool™ Single P-Channel, ESD, 1.6x1.6x0.55 mm UDFN Package

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 1.6 x 1.6 x 0.55 mm for Board Space Saving
- Lowest $R_{DS(on)}$ in 1.6x1.6 Package
- ESD Protected
- This is a Halide Free Device
- This is a Pb-Free Device

Applications

- High Side Load Switch
- PA Switch and Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		V_{DSS}	-30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-3.0	A
			$T_A = 85^\circ\text{C}$	-2.3	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	-4.0		
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	1.5	W
			$t \leq 5$ s	$T_A = 25^\circ\text{C}$	
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-2.0	A
			$T_A = 85^\circ\text{C}$	-1.5	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	P_D	0.6	W
Pulsed Drain Current		$t_p = 10 \mu\text{s}$	I_{DM}	-17	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150		$^\circ\text{C}$
Source Current (Body Diode) (Note 2)		I_S	-1.0		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260		$^\circ\text{C}$
Gate-to-Source ESD Rating (HBM) per JESD22-A114F		ESD	Class 1B		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

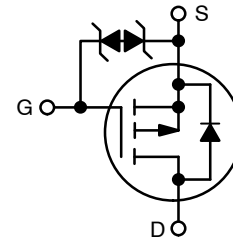


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MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-30 V	90 m Ω @ -10 V	-3.0 A
	155 m Ω @ -4.5 V	-2.0 A

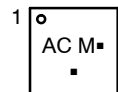


P-Channel MOSFET



UDFN6
CASE 517AU
 μ COOL™

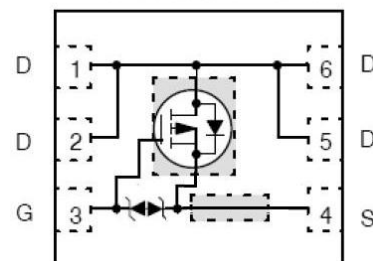
MARKING DIAGRAM



AC = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	85	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	55	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	200	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$, ref to 25°C		28		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -30\text{ V}$			-1.0	μA
					-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			10	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-1.0		-3.0	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$			3.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -3.0\text{ A}$		75	90	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -2.0\text{ A}$		120	155	
Forward Transconductance	g_{FS}	$V_{DS} = -5.0\text{ V}, I_D = -0.2\text{ A}$		1.3		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -15\text{ V}$		250		pF
Output Capacitance	C_{OSS}			60		
Reverse Transfer Capacitance	C_{RSS}			40		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V}; I_D = -3.0\text{ A}$		3.2	5.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.2		
Gate-to-Source Charge	Q_{GS}			1.0		
Gate-to-Drain Charge	Q_{GD}			1.5		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -15\text{ V}, I_D = -3.0\text{ A}, R_G = 1\ \Omega$		30		ns
Rise Time	t_r			95		
Turn-Off Delay Time	$t_{d(OFF)}$			50		
Fall Time	t_f			70		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	VSD	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 85^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -1.0\text{ A}$			11		ns
Charge Time	t_a				7.5		
Discharge Time	t_b				3.5		
Reverse Recovery Charge	Q_{RR}				5.0		nC

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 1 oz. Cu.
- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

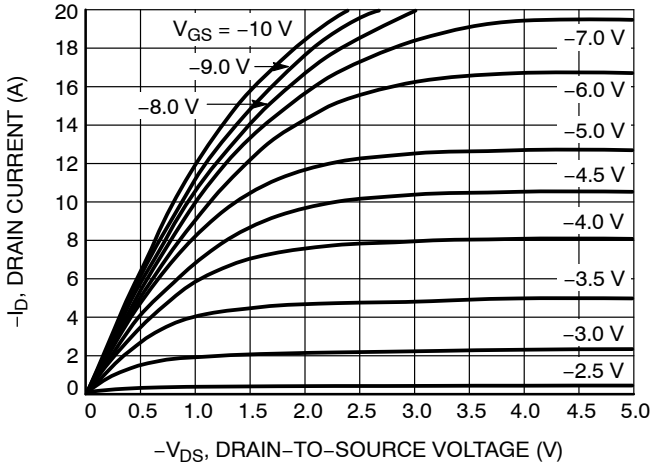


Figure 1. On-Region Characteristics

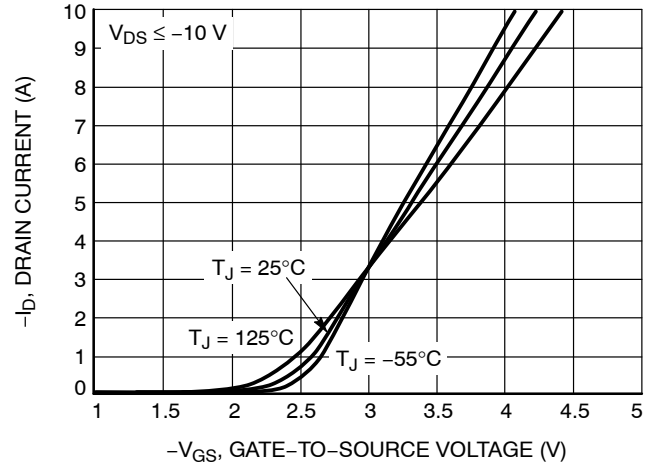


Figure 2. Transfer Characteristics

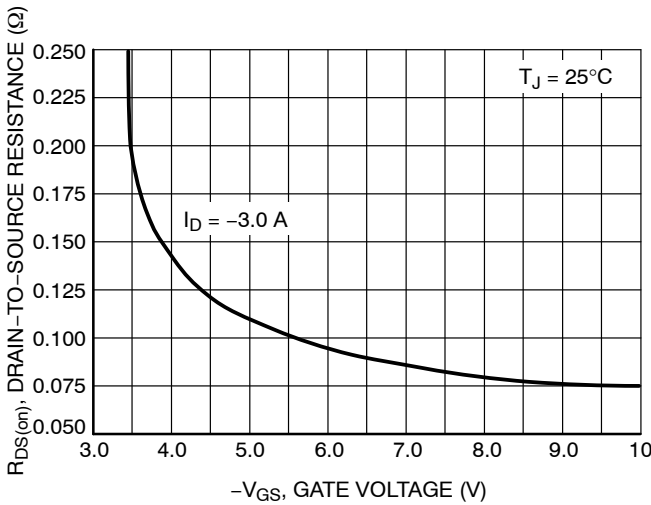


Figure 3. On-Resistance vs. Gate-to-Source Voltage

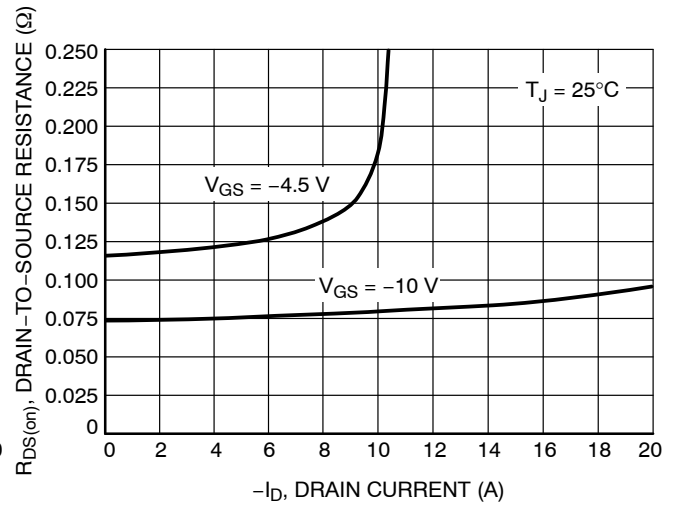


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

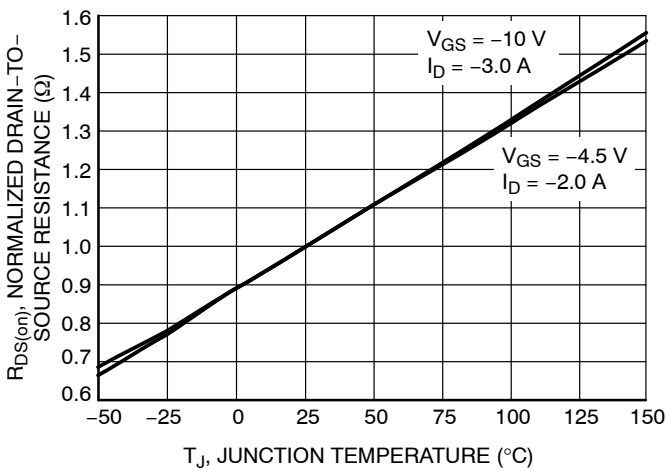


Figure 5. On-Resistance Variation with Temperature

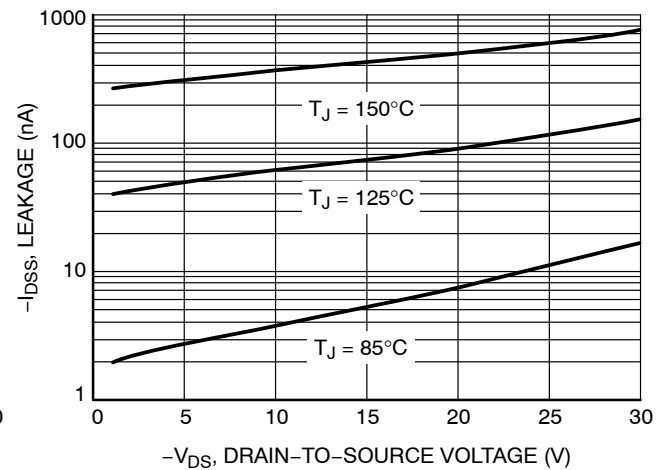


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

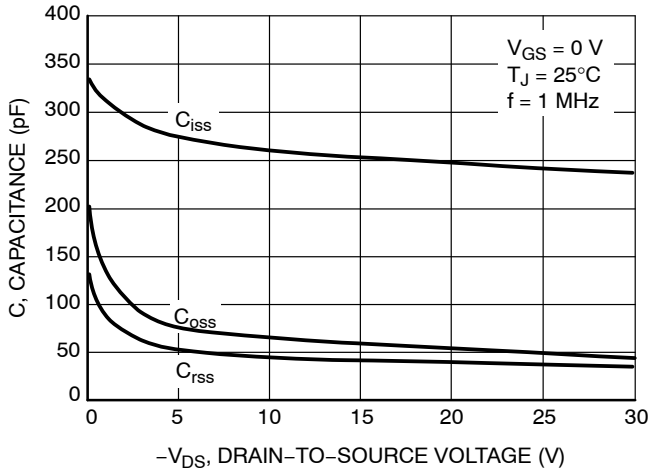


Figure 7. Capacitance Variation

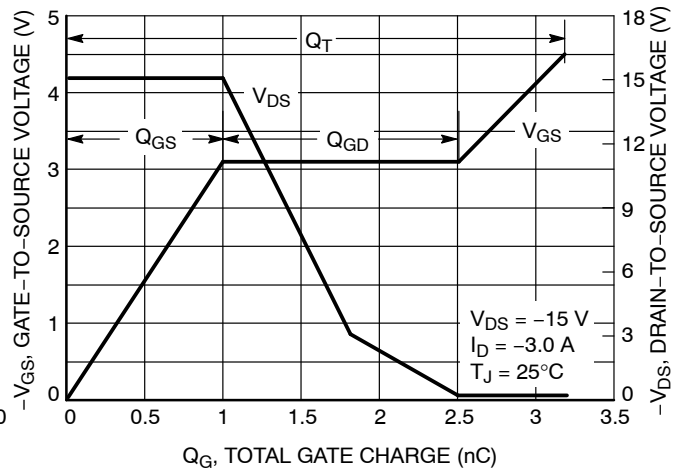


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

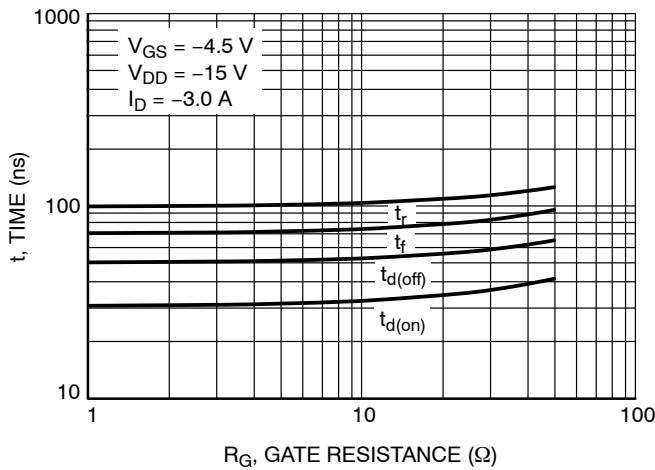


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

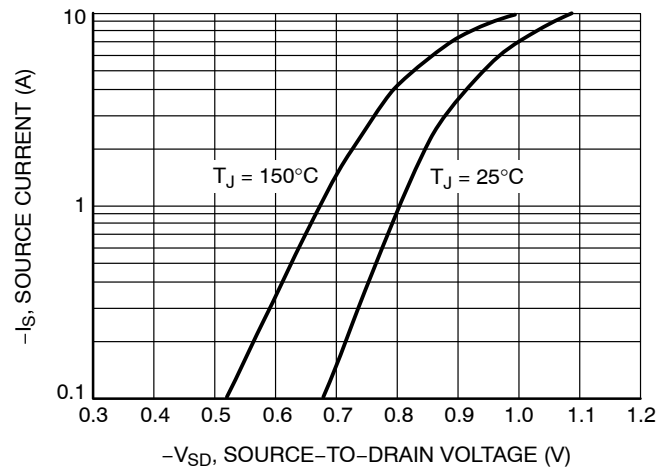


Figure 10. Diode Forward Voltage vs. Current

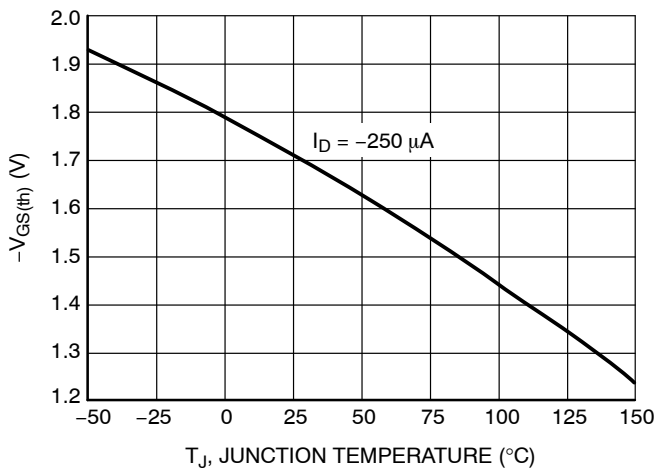


Figure 11. Threshold Voltage

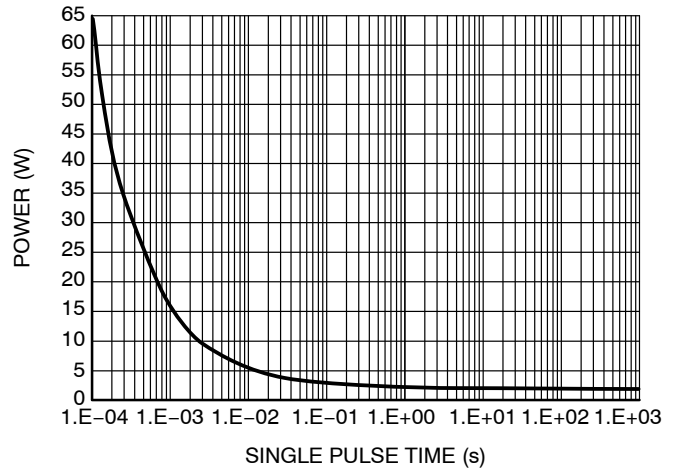


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

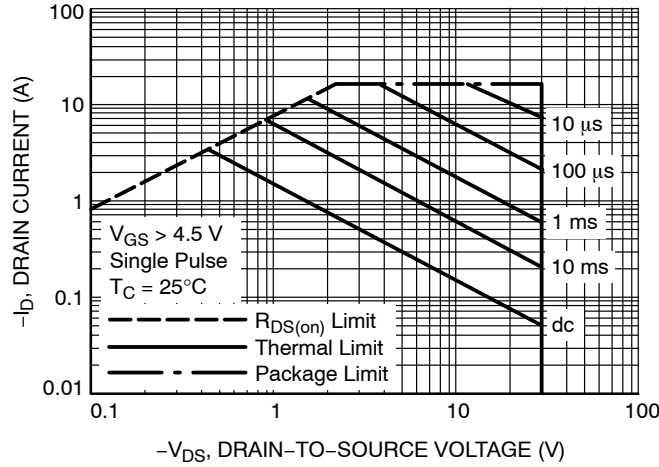


Figure 13. Maximum Rated Forward Biased Safe Operating Area

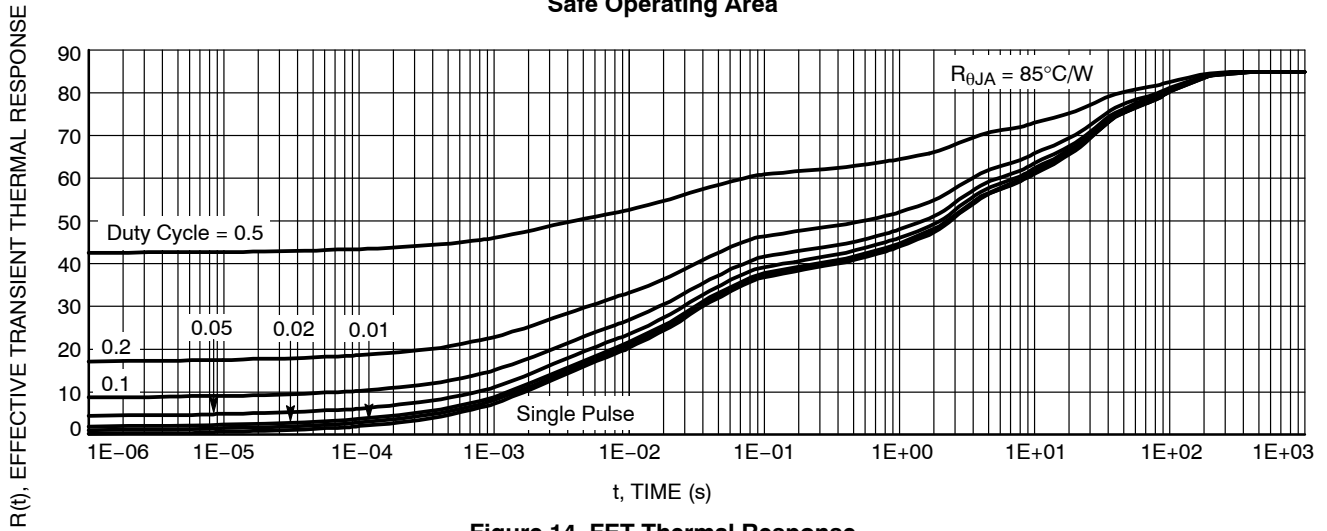


Figure 14. FET Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLUS4195PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS4195PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

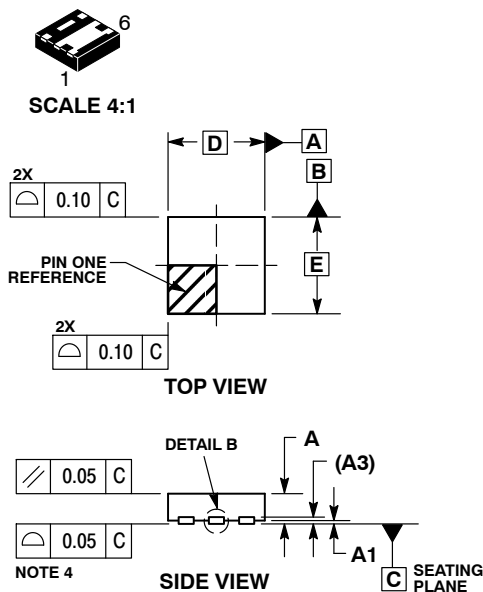
PACKAGE DIMENSIONS

ON Semiconductor®



UDFN6 1.6x1.6, 0.5P CASE 517AU-01 ISSUE O

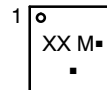
DATE 16 OCT 2008



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D1	0.62	0.72
D2	0.15	0.25
E2	0.57	0.67
F	0.55	BSC
G	0.25	BSC
L	0.20	0.30
L1	---	0.15

GENERIC MARKING DIAGRAM*

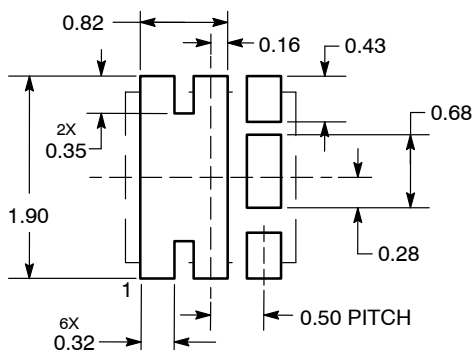
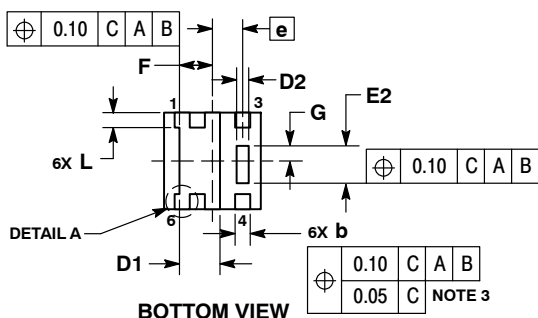


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "▪", may or may not be present.



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN6, 1.6X1.6, 0.5P	PAGE 1 OF 1

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