

# NTLUS3A40PZ

## MOSFET – Power, Single, P-Channel, ESD, $\mu$ Cool, UDFN, 2.0x2.0x0.55 mm -20 V, -9.4 A



ON Semiconductor®

<http://onsemi.com>

### Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- Lowest RDS(on) in 2.0x2.0 Package
- ESD Protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- High Side Load Switch
- PA Switch and Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

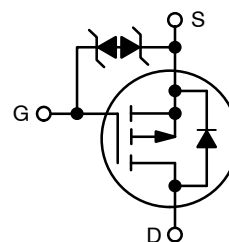
### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		V <sub>DSS</sub>	-20	V	
Gate-to-Source Voltage		V <sub>GS</sub>	±8.0	V	
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	-6.4	A
			T <sub>A</sub> = 85°C	-4.6	
	t ≤ 5 s	T <sub>A</sub> = 25°C	-9.4		
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.7	W
	t ≤ 5 s	T <sub>A</sub> = 25°C		3.8	
Continuous Drain Current (Note 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	-4.0	A
		T <sub>A</sub> = 85°C		-2.9	
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.7	W
Pulsed Drain Current		t <sub>p</sub> = 10 μs	I <sub>DM</sub>	-30	A
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>STG</sub>	-55 to 150		°C
Source Current (Body Diode) (Note 2)		I <sub>S</sub>	-1.0		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260		°C
ESD Rating (HBM) per JESD22-A114F		ESD	>2000		V

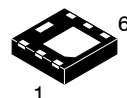
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

MOSFET		
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
-20 V	29 mΩ @ -4.5 V	-9.4 A
	39 mΩ @ -2.5 V	
	60 mΩ @ -1.8 V	
	120 mΩ @ -1.5 V	

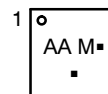


P-Channel MOSFET



UDFN6  
CASE 517BG  
 $\mu$ COOL™

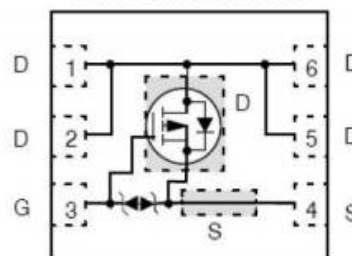
### MARKING DIAGRAM



AA = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NTLUS3A40PZ

2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 2 oz. Cu.

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	R <sub>θJA</sub>	72	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)	R <sub>θJA</sub>	33	
Junction-to-Ambient – Steady State min Pad (Note 4)	R <sub>θJA</sub>	189	

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
-----------	--------	----------------	-----	-----	-----	-------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA, ref to 25°C		-5.0		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -20 V			-1.0	μA
			T <sub>J</sub> = 25°C			
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8.0 V			±10	μA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.4		-1.0	V
Negative Threshold Temp. Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.4 A		23	29	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -4.8 A		31	39	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -2.5 A		43	60	
		V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -1.5 A		60	120	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -4.0 A		18		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = -15 V		2600		pF
Output Capacitance	C <sub>OSS</sub>			200		
Reverse Transfer Capacitance	C <sub>RSS</sub>			190		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -15 V; I <sub>D</sub> = -4.0 A		29		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.4		
Gate-to-Source Charge	Q <sub>GS</sub>			3.7		
Gate-to-Drain Charge	Q <sub>GD</sub>			8.1		

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 6)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -4.0 A, R <sub>G</sub> = 1 Ω		9.0		ns
Rise Time	t <sub>r</sub>			18		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			126		
Fall Time	t <sub>f</sub>			71		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	VSD	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.0 A	T <sub>J</sub> = 25°C	0.65	1.0	V
			T <sub>J</sub> = 125°C	0.55		

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).  
 4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 2 oz. Cu.  
 5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.  
 6. Switching characteristics are independent of operating junction temperatures.

# NTLUS3A40PZ

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
-----------	--------	----------------	-----	-----	-----	-------

### DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}$ , $dis/dt = 100\text{ A}/\mu\text{s}$ , $I_S = -1.0\text{ A}$		25		ns
Charge Time	$t_a$			10		
Discharge Time	$t_b$			15		
Reverse Recovery Charge	$Q_{RR}$			13.6		nC

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 2 oz. Cu.
- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

# NTLUS3A40PZ

## TYPICAL CHARACTERISTICS

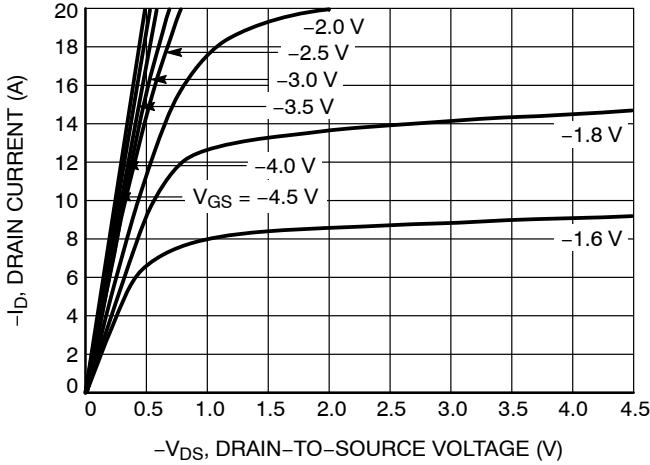


Figure 1. On-Region Characteristics

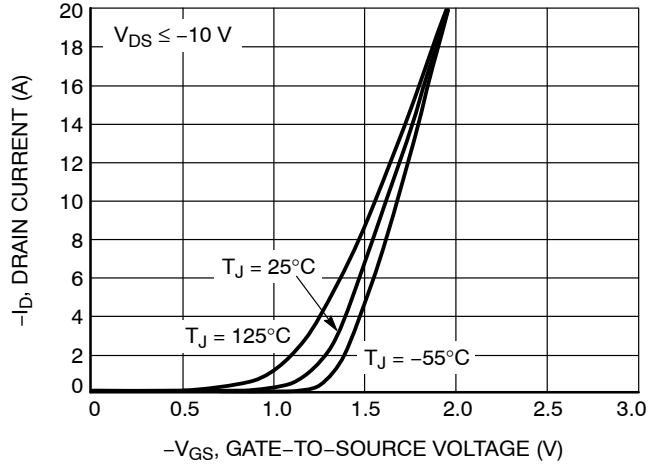


Figure 2. Transfer Characteristics

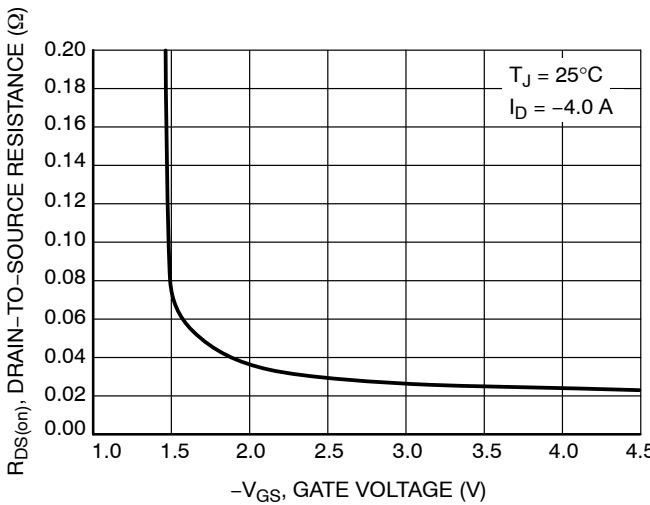


Figure 3. On-Resistance vs. Gate-to-Source Voltage

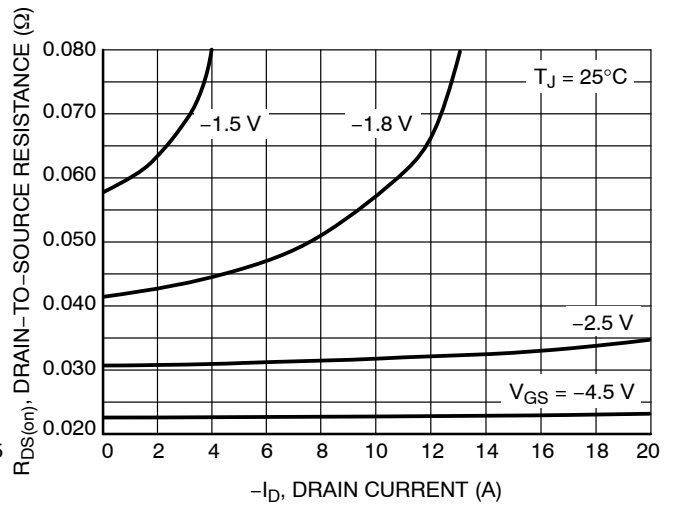


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

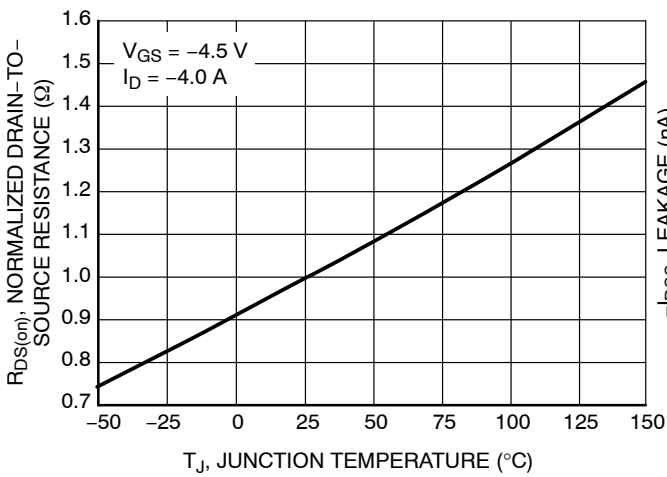


Figure 5. On-Resistance Variation with Temperature

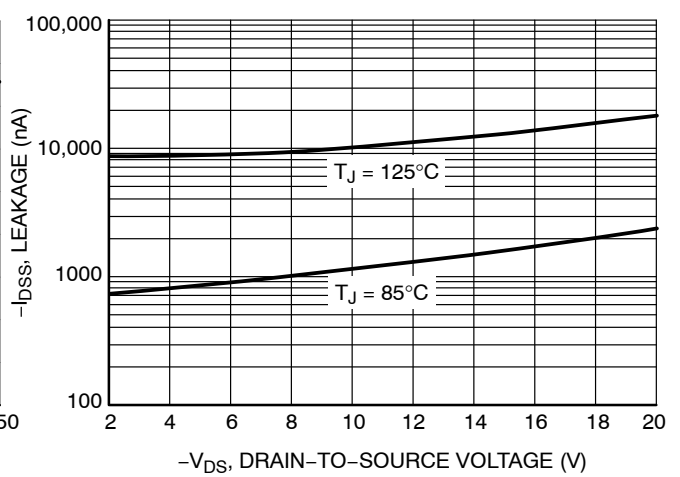


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTLUS3A40PZ

## TYPICAL CHARACTERISTICS

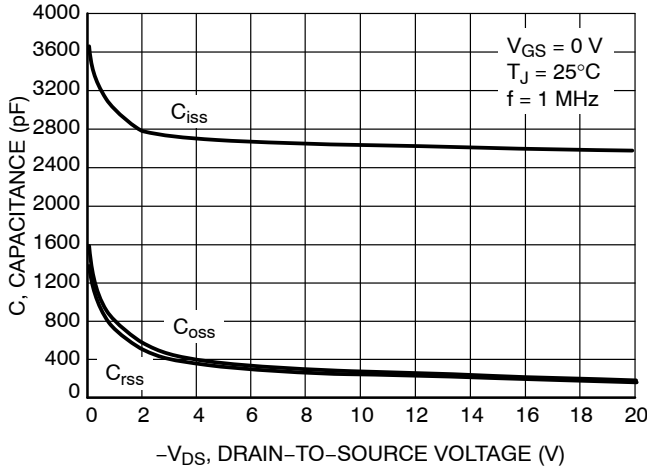


Figure 7. Capacitance Variation

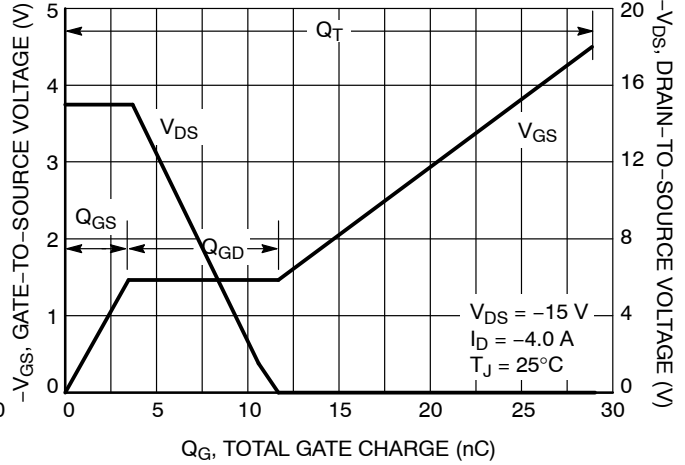


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

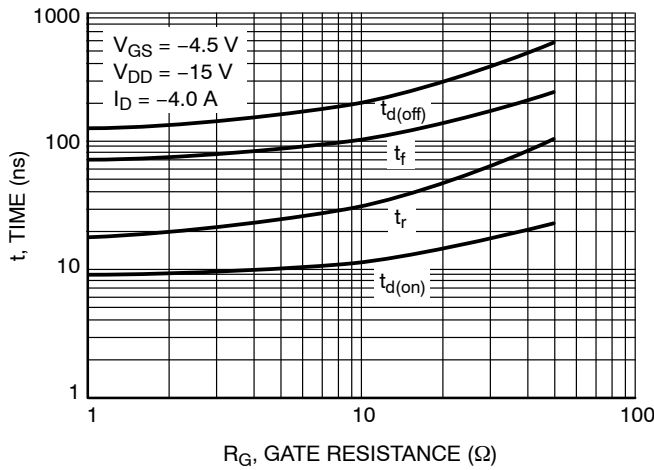


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

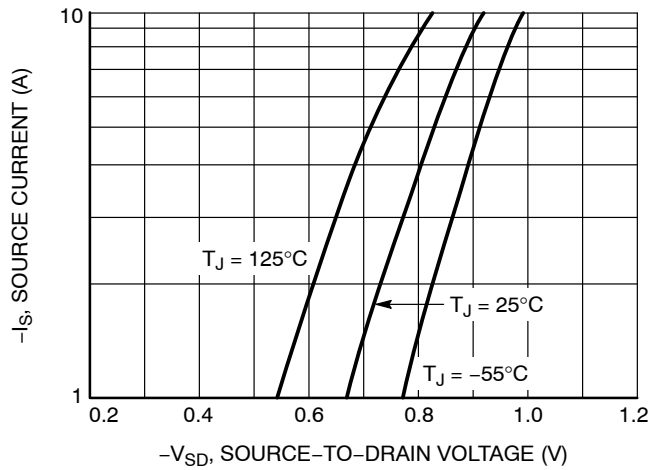


Figure 10. Diode Forward Voltage vs. Current

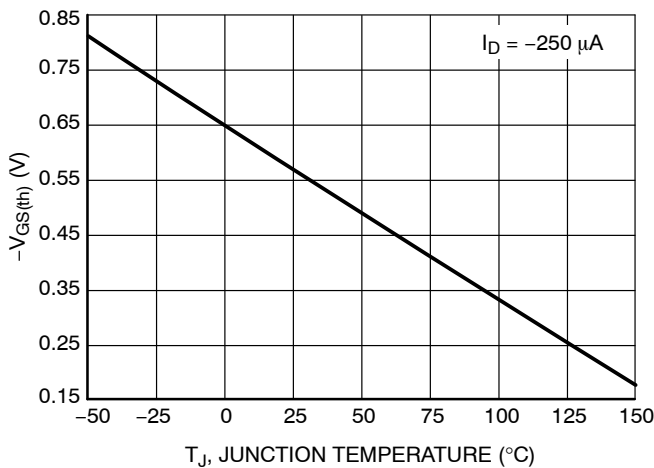


Figure 11. Threshold Voltage

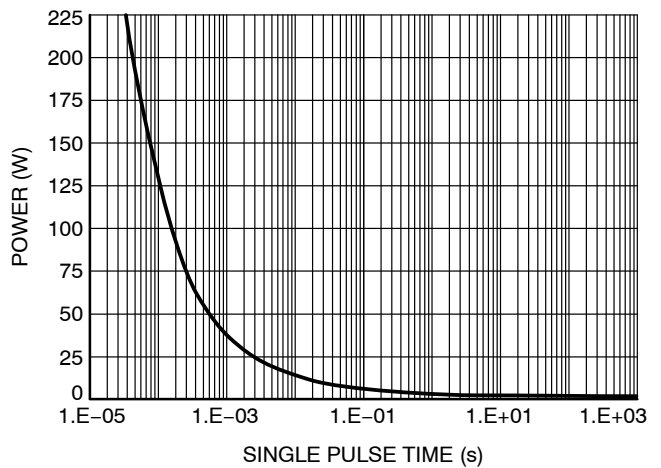
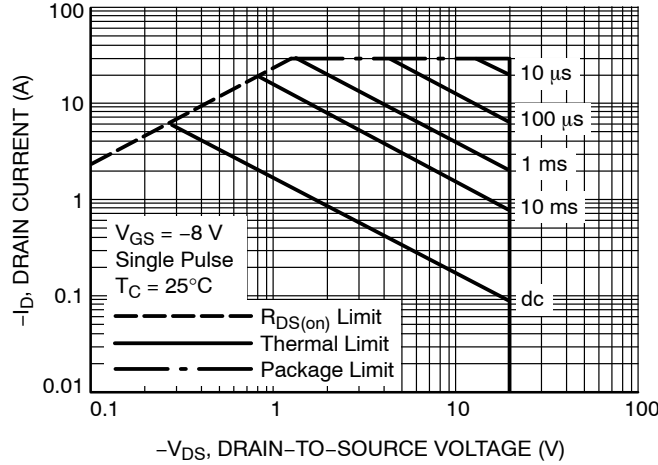


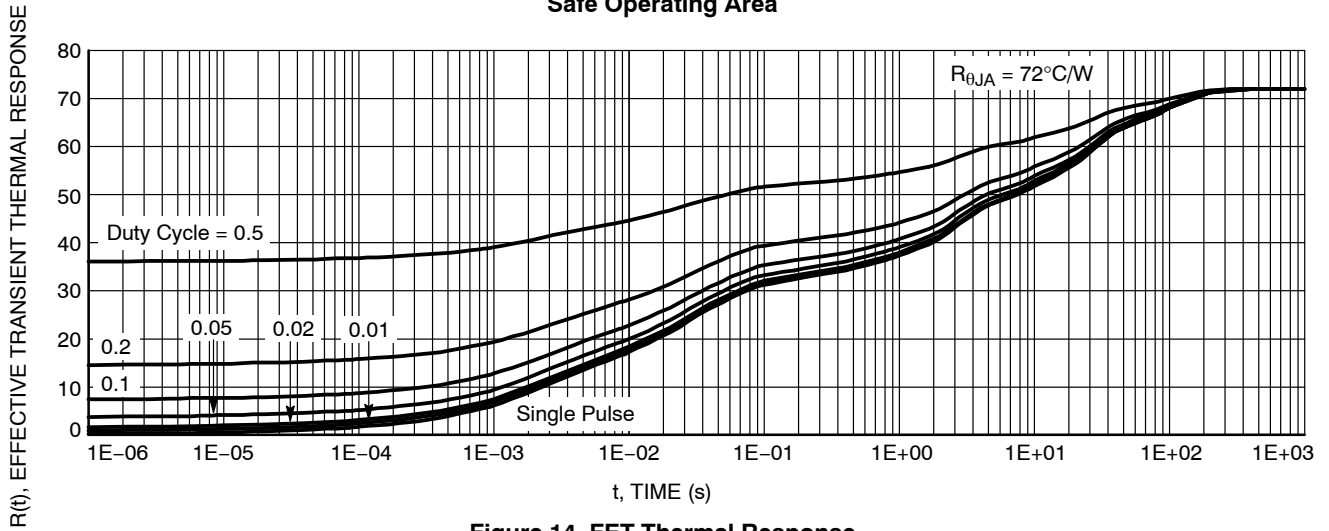
Figure 12. Single Pulse Maximum Power Dissipation

# NTLUS3A40PZ

## TYPICAL CHARACTERISTICS



**Figure 13. Maximum Rated Forward Biased Safe Operating Area**



**Figure 14. FET Thermal Response**

### DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLUS3A40PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS3A40PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

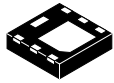
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

μCool is a trademark of Semiconductor Components Industries, LLC (SCILLC).

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

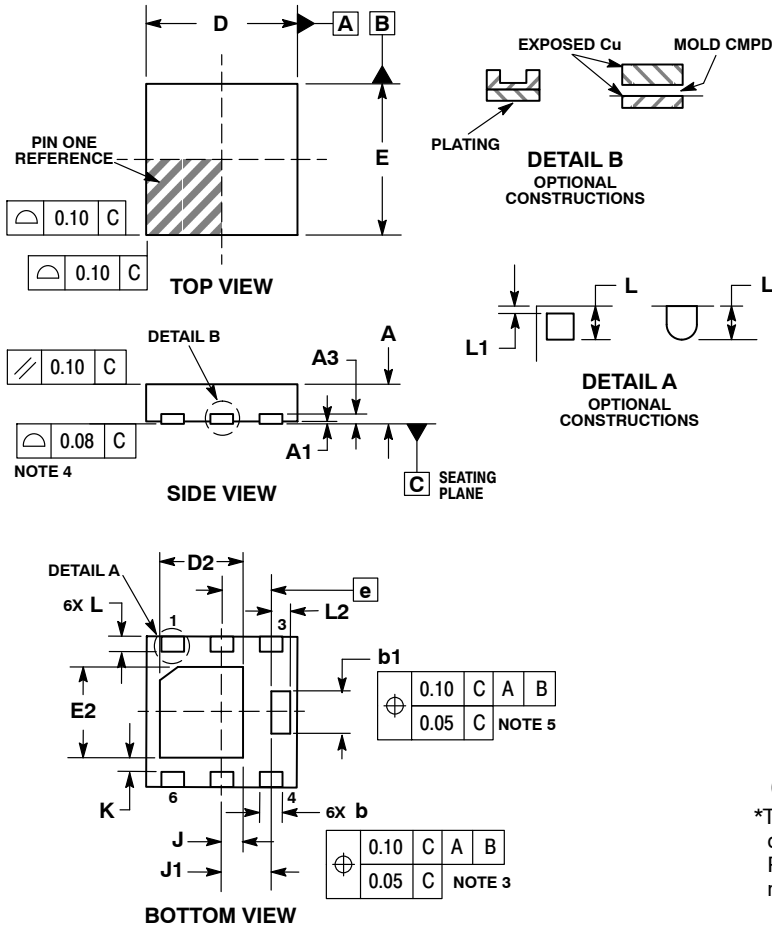
ON Semiconductor®



SCALE 4:1

UDFN6 2x2, 0.65P  
CASE 517BG-01  
ISSUE A

DATE 04 FEB 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
1. CENTER TERMINAL LEAD IS OPTIONAL. CENTER TERMINAL IS CONNECTED TO TERMINAL LEAD # 4.
2. LEADS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
J	0.27 BSC	
J1	0.65 BSC	
L	0.20	0.30
L1	---	0.10
L2	0.20	0.30

**GENERIC MARKING DIAGRAM\***

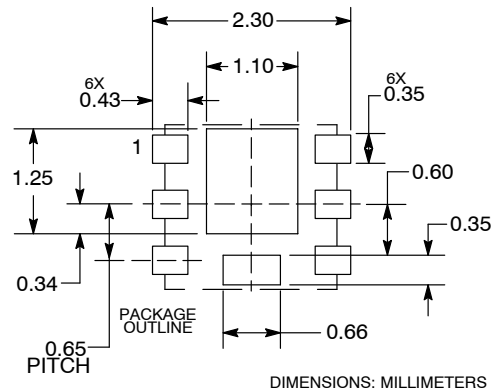


XX = Specific Device Code  
M = Date Code

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**RECOMMENDED MOUNTING FOOTPRINT**



<b>DOCUMENT NUMBER:</b>	<b>98AON48158E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>UDFN6 2X2, 0.65P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)