

NTHD4N02F

Power MOSFET and Schottky Diode

20 V, 3.9 A, N-Channel, with 3.7 A Schottky Barrier Diode, ChipFET™

Features

- Leadless SMD Package Featuring a MOSFET and Schottky Diode
- 40% Smaller than TSOP-6 Package with Better Thermals
- Super Low Gate Charge MOSFET
- Ultra Low V_F Schottky
- Pb-Free Package is Available

Applications

- Fast Switching, low Gate Charge for DC-to-DC Buck and Boost Converters
- Li-Ion Battery Applications in Cell Phones, PDAs, DSCs, and Media Players
- Load Side Switching

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	20	V
Gate-to-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	Steady State	$T_J = 25^\circ\text{C}$	I_D 2.9
		$T_J = 85^\circ\text{C}$	2.1
		$t \leq 5 \text{ s}$, $T_J = 25^\circ\text{C}$	3.9
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM} 12	A
Power Dissipation	Steady State	$T_J = 25^\circ\text{C}$	P_D 0.91
		$T_J = 85^\circ\text{C}$	0.36
		$t \leq 5 \text{ s}$, $T_J = 25^\circ\text{C}$	2.1
Continuous Source Current (Body Diode)	I_S	2.6	A
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

SCHOTTKY DIODE MAXIMUM RATINGS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak Repetitive Reverse Voltage	V_{RRM}	20	V
DC Blocking Voltage	V_R	20	V
Average Rectified Forward Current	Steady State	$T_J = 25^\circ\text{C}$	I_F 2.2
		$t \leq 5 \text{ s}$	3.7

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



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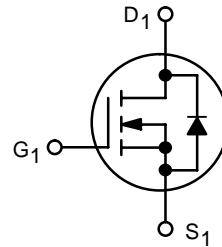
<http://onsemi.com>

MOSFET

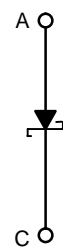
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	60 m Ω @ 4.5 V	3.9 A
	80 m Ω @ 2.5 V	

SCHOTTKY DIODE

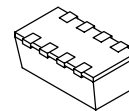
V_R MAX	V_F TYP	I_F MAX
20 V	0.35 V	3.7 A



N-Channel MOSFET

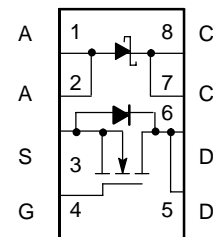


SCHOTTKY DIODE

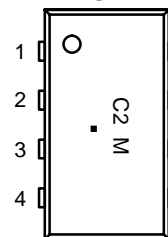


ChipFET™
CASE 1206A
STYLE 3

PIN CONNECTIONS



MARKING DIAGRAM



C2 = Specific Device Code
M = Month Code
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4N02FT1	ChipFET	3000/Tape & Reel
NTHD4N02FT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD4N02F

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	110	°C/W
Junction-to-Ambient – $t \leq 5$ s	$R_{\theta JA}$	60	°C/W

1. Surface Mounted on FR4 Board using 1 in sq. pad size (Cu area = 1.27 in sq. [1 oz] including traces).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ μA	20	28		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V $V_{DS} = 16$ V	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 85^\circ\text{C}$		5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μA	0.6		1.2	V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5$, $I_D = 2.9$ A		0.058	0.080	Ω
		$V_{GS} = 2.5$, $I_D = 2.3$ A		0.077	0.115	
Forward Transconductance	g_{FS}	$V_{DS} = 10$ V, $I_D = 2.9$ A		6.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = 10$ V		180	300	pF
Output Capacitance	C_{OSS}			80	130	
Reverse Transfer Capacitance	C_{RSS}			30	50	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 10$ V, $I_D = 2.9$ A		2.6	4.0	nC
Gate-to-Source Charge	Q_{GS}			0.6		
Gate-to-Drain Charge	Q_{GD}			0.7		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DD} = 16$ V, $I_D = 2.9$ A, $R_G = 2.5$ Ω		5.0	10	ns
Rise Time	t_r			9.0	18	
Turn-Off Delay Time	$t_{d(OFF)}$			10	20	
Fall Time	t_f			3.0	6.0	

DRAIN-SOURCE DIODE CHARACTERISTICS (Note 2)

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = 2.6$ A		0.8	1.15	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $I_S = 2.6$ A, $di_S/dt = 100$ A/ μs		12.5		ns
Charge Time	t_a			9.0		
Discharge Time	t_b			3.5		
Reverse Recovery Charge	Q_{RR}			6.0		

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Maximum Instantaneous Forward Voltage	V_F	$I_F = 0.1$ A			0.31	V
		$I_F = 1.0$ A			0.365	
Maximum Instantaneous Reverse Current	I_R	$V_R = 10$ V			0.75	mA
		$V_R = 20$ V			2.5	
Non-Repetitive Peak Surge Current	I_{FSM}	Halfwave, Single Pulse, 60 Hz			23	A

2. Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL MOSFET PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

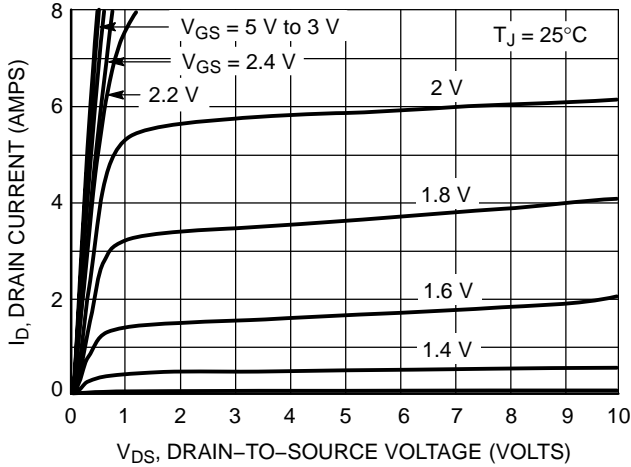


Figure 1. On-Region Characteristics

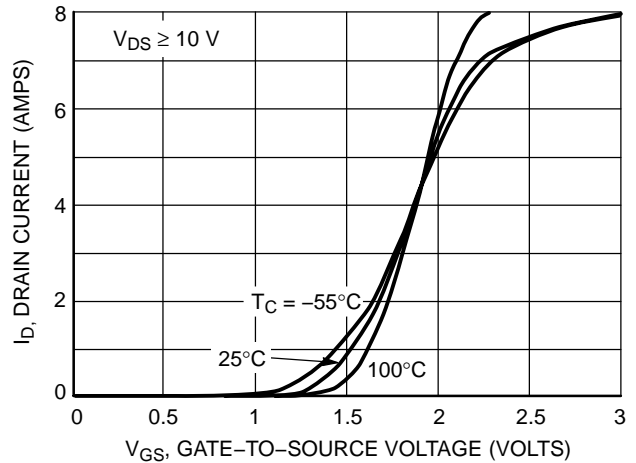


Figure 2. Transfer Characteristics

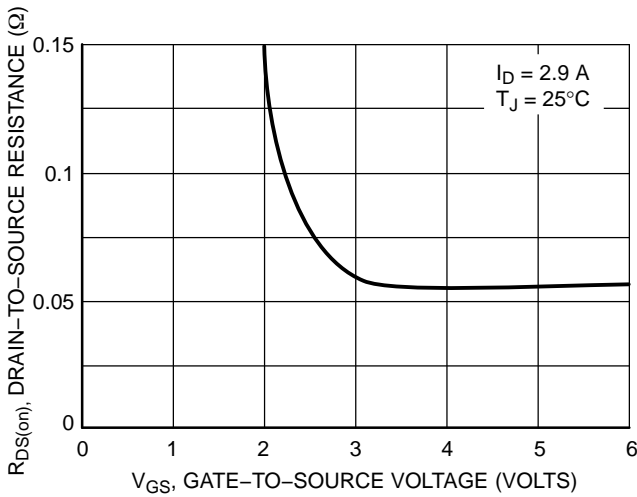


Figure 3. On-Resistance vs. Gate-to-Source Voltage

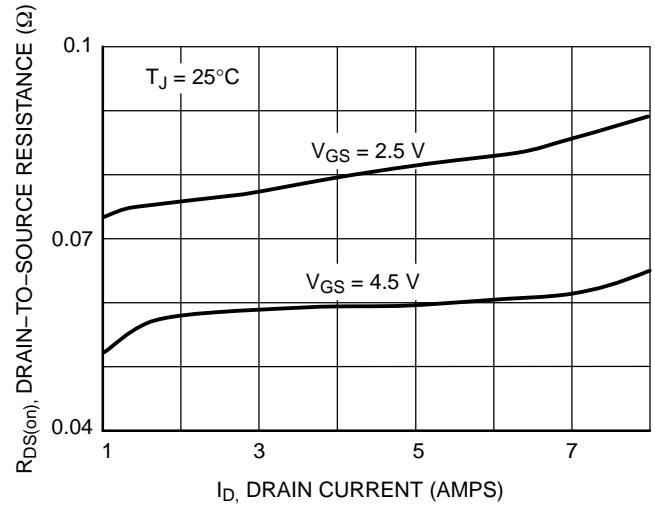


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

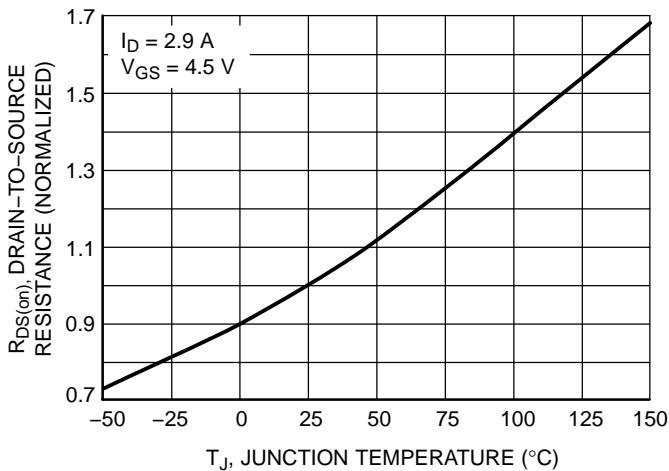


Figure 5. On-Resistance Variation with Temperature

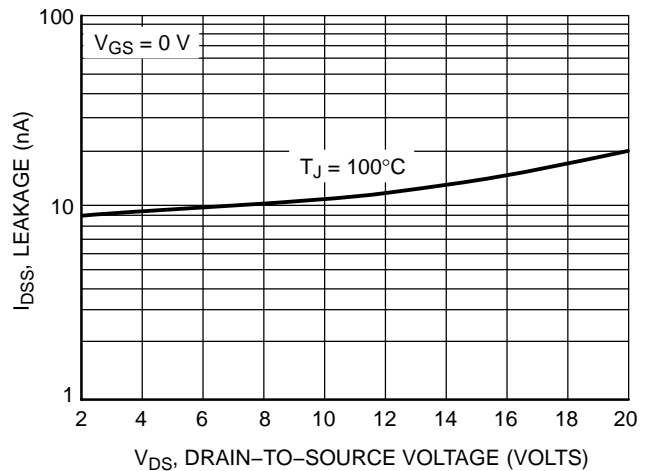


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL MOSFET PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

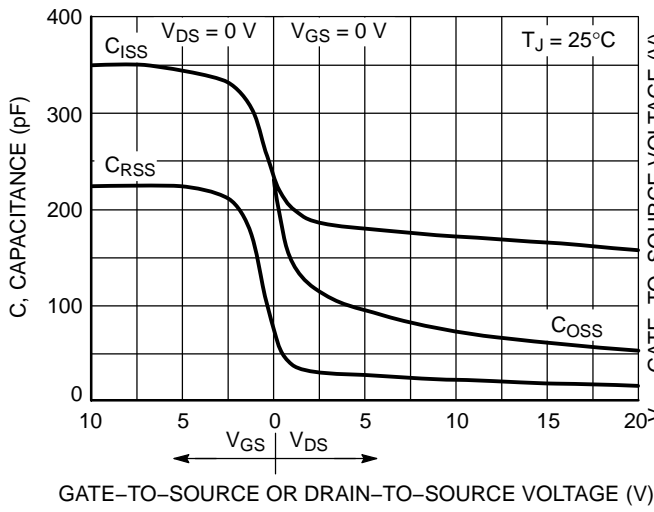


Figure 7. Capacitance Variation

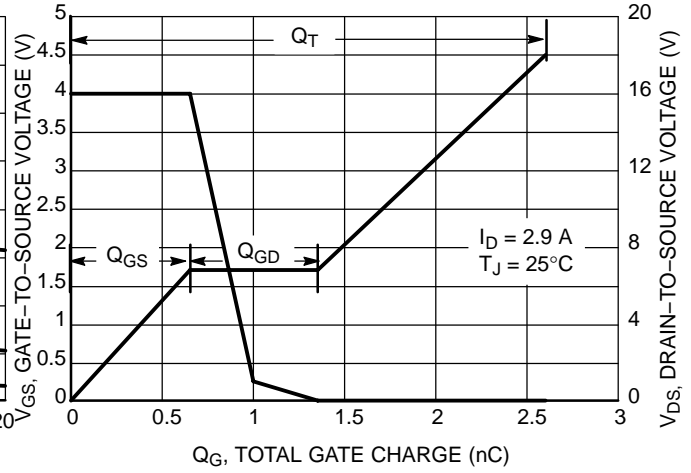


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

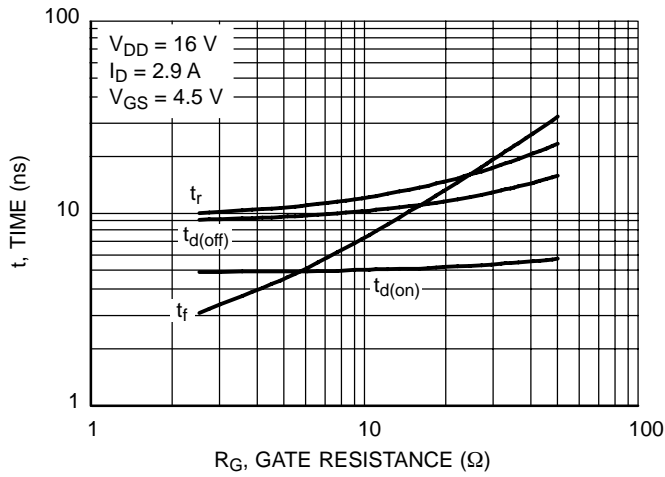


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

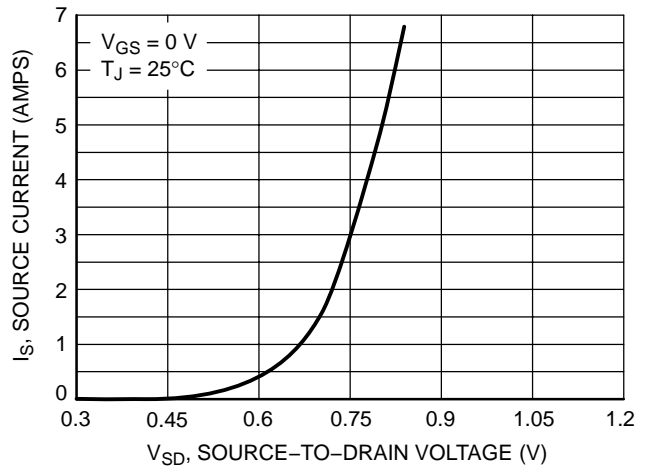


Figure 10. Diode Forward Voltage vs. Current

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TYPICAL SCHOTTKY PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

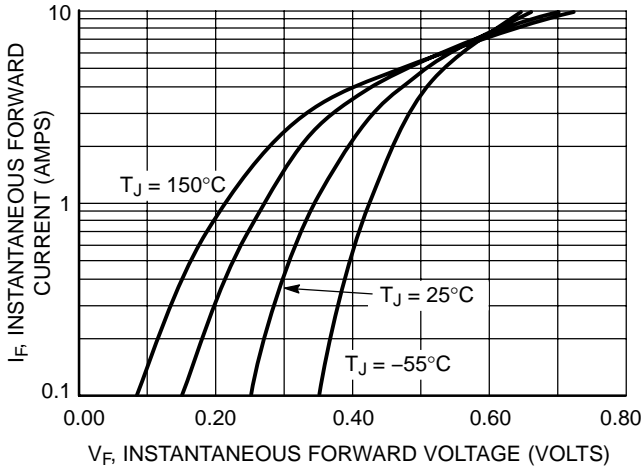


Figure 11. Typical Forward Voltage

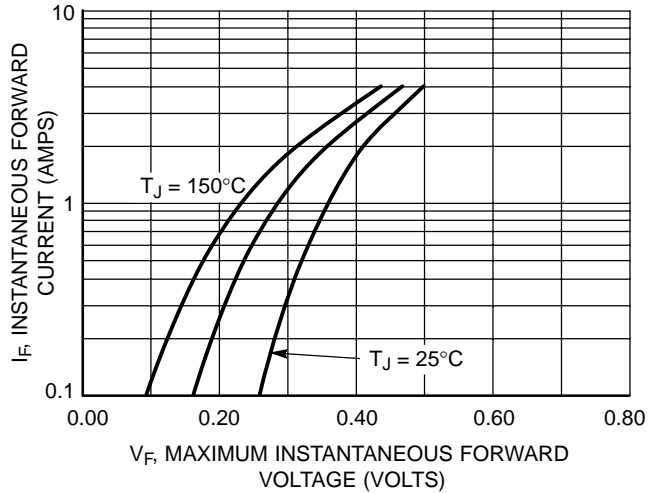


Figure 12. Maximum Forward Voltage

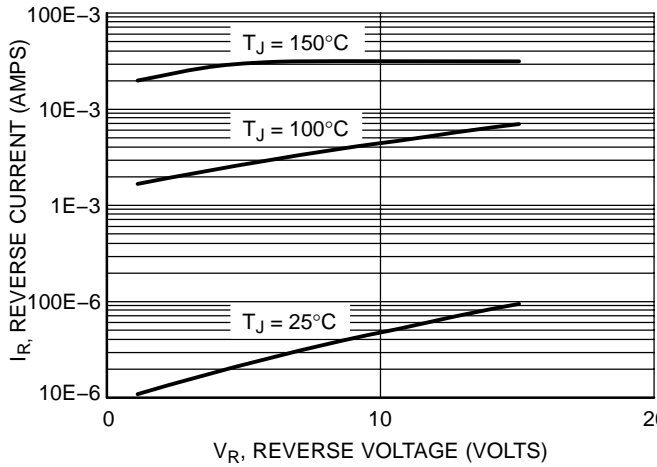


Figure 13. Typical Reverse Current

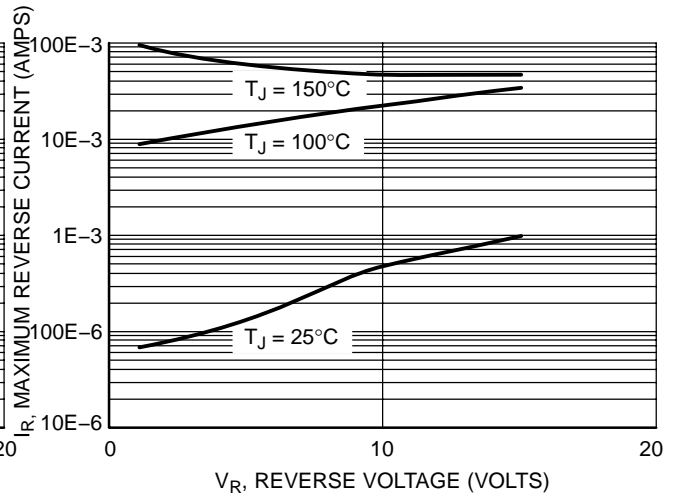


Figure 14. Maximum Reverse Current

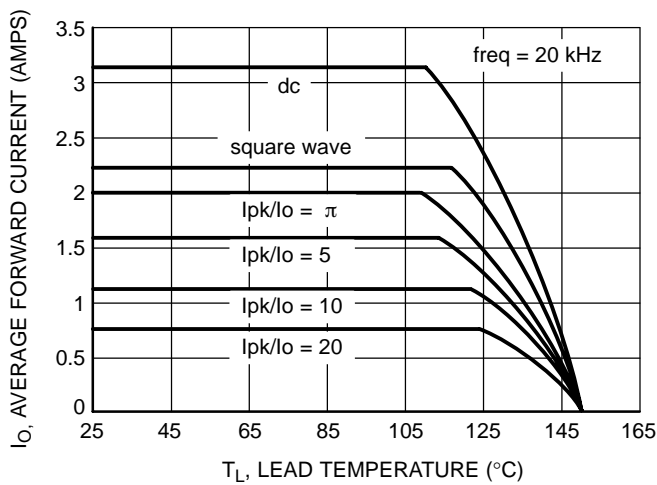


Figure 15. Current Derating

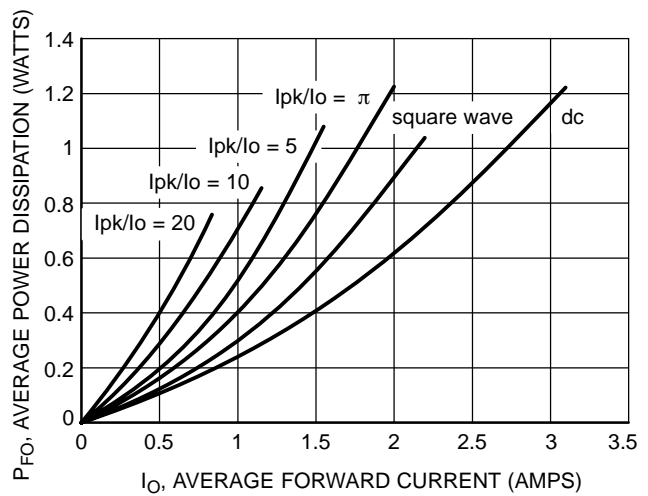


Figure 16. Forward Power Dissipation

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™ CASE1206A-03 ISSUE K

DATE 19 MAY 2009



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

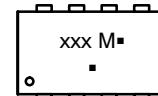
- | | | | | | |
|---|---|---|--|---|---|
| STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN | STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1 | STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE | STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR | STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE | STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN |
|---|---|---|--|---|---|

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
 - M = Month Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

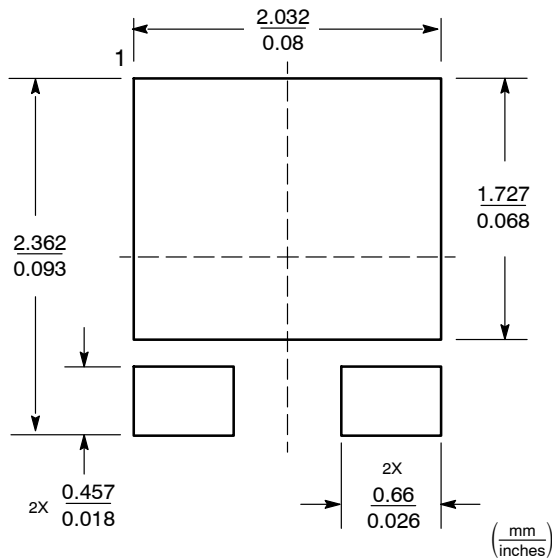
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

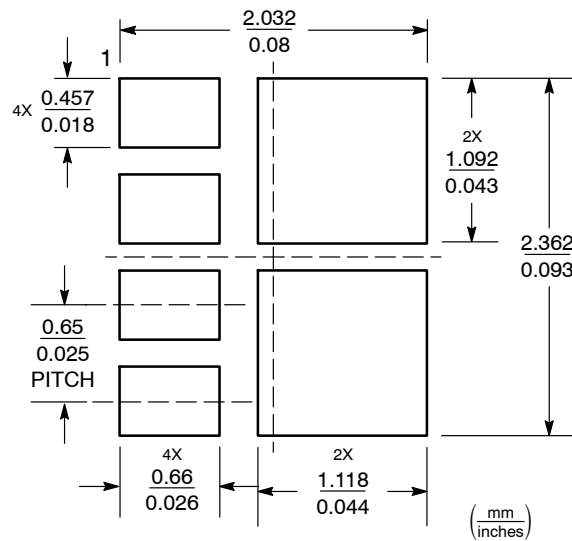
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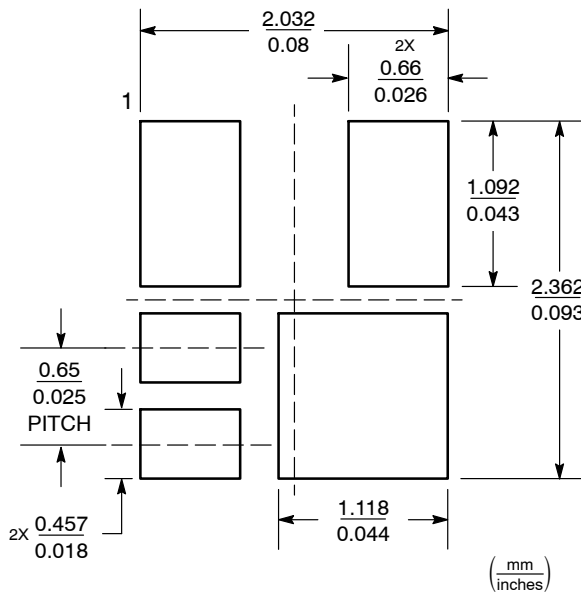
ADDITIONAL SOLDERING FOOTPRINTS*



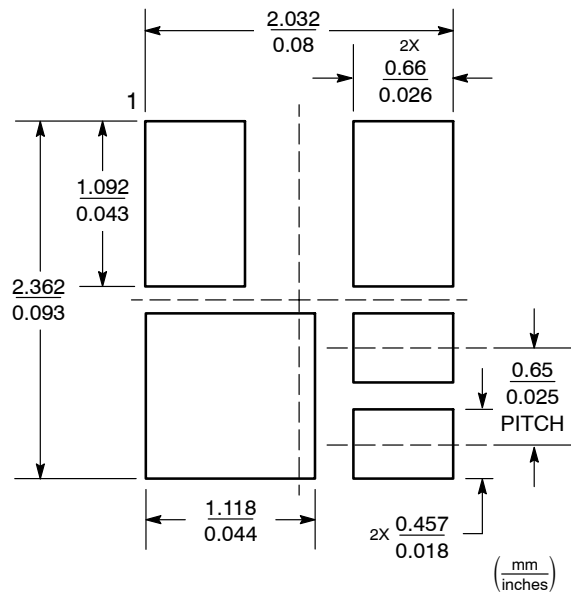
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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