

NTHD3102C

MOSFET – Power, Complementary, ChipFET 20 V, +5.5 A /-4.2 A

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- This is a Pb-Free Device

Applications

- DC-DC Conversion Circuits
- Load/Power Switching
- Single or Dual Cell Li-Ion Battery Supplied Devices
- Ideal for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V _{DSS}	20	V	
Gate-to-Source Voltage	N-Ch	±8.0	V	
	P-Ch	±8.0	V	
N-Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D 4.0	A
		T _A = 85°C	2.9	
	t ≤ 5 s	T _A = 25°C	5.5	
P-Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D 3.1	A
		T _A = 85°C	2.2	
	t ≤ 5 s	T _A = 25°C	4.2	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D 1.1	W
		t ≤ 5 s	2.1	
Gate-to-Source ESD Rating – (Human Body Model, Method 3015)	ESD	100	V	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

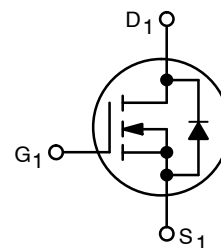
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu. area = 1.127 in sq [1 oz] including traces).



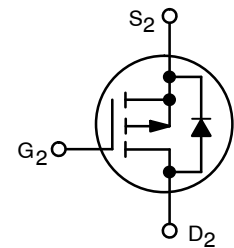
ON Semiconductor®

<http://onsemi.com>

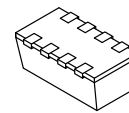
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX (Note 1)
N-Channel 20 V	29 mΩ @ 4.5 V	5.5 A
	37 mΩ @ 2.5 V	
	48 mΩ @ 1.8 V	
P-Channel -20 V	64 mΩ @ 4.5 V	-4.2 A
	83 mΩ @ 2.5 V	
	105 mΩ @ 1.8 V	



N-Channel MOSFET

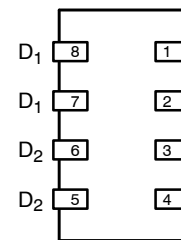


P-Channel MOSFET



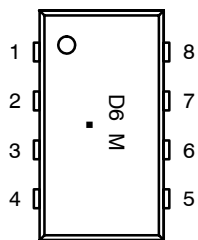
ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



(Bottom View)

MARKING DIAGRAM



(Top View)

- D6 = Specific Device Code
- M = Date Code
- = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NTHD3102C

MAXIMUM RATINGS (continued) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
N-Channel Continuous Drain Current (Note 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	3.0	A
		$T_A = 85^\circ\text{C}$		2.2	
P-Channel Continuous Drain Current (Note 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	2.3	A
		$T_A = 85^\circ\text{C}$		1.7	
Power Dissipation (Note 3)		$T_A = 25^\circ\text{C}$	P_D	0.6	W
Pulsed Drain Current	N-Ch	$t_p = 10 \mu\text{s}$	I_{DM}	16	A
	P-Ch			12.6	
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	1.7	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5 \text{ s}$ (Note 2)		60	
Junction-to-Ambient – Steady State (Note 3)		195	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4)	$V_{(BR)DSS}$	N	$V_{GS} = 0 \text{ V}$	$I_D = 250 \mu\text{A}$	20		V
		P		$I_D = -250 \mu\text{A}$	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N			20.2		mV/ $^\circ\text{C}$
		P			16.2		
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0 \text{ V}, V_{DS} = 16 \text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
		P	$V_{GS} = 0 \text{ V}, V_{DS} = -16 \text{ V}$			-1.0	
		N	$V_{GS} = 0 \text{ V}, V_{DS} = 16 \text{ V}$	$T_J = 85^\circ\text{C}$		5.0	
		P	$V_{GS} = 0 \text{ V}, V_{DS} = -16 \text{ V}$			-5.0	
Gate-to-Source Leakage Current	I_{GSS}	N	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8.0 \text{ V}$			± 100	nA
		P	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8.0 \text{ V}$			± 100	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
3. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq).
4. Switching characteristics are independent of operating junction temperatures.

NTHD3102C

ELECTRICAL CHARACTERISTICS (continued) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250 \mu\text{A}$	0.4	1.2	V
		P		$I_D = -250 \mu\text{A}$	-0.4	-1.2	
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5 \text{ V}, I_D = 4.4 \text{ A}$		29	45	m Ω
		P	$V_{GS} = -4.5 \text{ V}, I_D = -3.2 \text{ A}$		64	80	
		N	$V_{GS} = 2.5 \text{ V}, I_D = 4.1 \text{ A}$		37	50	
		P	$V_{GS} = -2.5 \text{ V}, I_D = -2.5 \text{ A}$		83	110	
		N	$V_{GS} = 1.8 \text{ V}, I_D = 1.9 \text{ A}$		48	70	
		P	$V_{GS} = -1.8 \text{ V}, I_D = -0.6 \text{ A}$		105	150	
Forward Transconductance	g_{FS}	N	$V_{DS} = 10 \text{ V}, I_D = 4.4 \text{ A}$		7.7		S
		P	$V_{DS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		5.9		

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	N	$f = 1.0 \text{ MHz}, V_{GS} = 0 \text{ V}$	$V_{DS} = 10 \text{ V}$		510	pF
		P		$V_{DS} = -10 \text{ V}$		650	
Output Capacitance	C_{OSS}	N		$V_{DS} = 10 \text{ V}$		100	
		P		$V_{DS} = -10 \text{ V}$		100	
Reverse Transfer Capacitance	C_{RSS}	N		$V_{DS} = 10 \text{ V}$		50	
		P		$V_{DS} = -10 \text{ V}$		50	
Total Gate Charge	$Q_{G(TOT)}$	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 4.4 \text{ A}$		5.8	7.9	nC
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		6.6	8.9	
Threshold Gate Charge	$Q_{G(TH)}$	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 4.4 \text{ A}$		0.96		
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		0.98		
Gate-to-Source Charge	Q_{GS}	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 4.4 \text{ A}$		1.2		
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		1.4		
Gate-to-Drain Charge	Q_{GD}	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 4.4 \text{ A}$		1.56		
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		1.64		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5 \text{ V}, V_{DD} = 10 \text{ V}, I_D = 4.4 \text{ A}, R_G = 2.5 \Omega$		7.2	ns
Rise Time	t_r				15.9	
Turn-Off Delay Time	$t_{d(OFF)}$				15.7	
Fall Time	t_f				4.6	
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5 \text{ V}, V_{DD} = -10 \text{ V}, I_D = -3.2 \text{ A}, R_G = 2.5 \Omega$		6.4	
Rise Time	t_r				16.9	
Turn-Off Delay Time	$t_{d(OFF)}$				16.4	
Fall Time	t_f				15.0	

5. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

NTHD3102C

ELECTRICAL CHARACTERISTICS (continued) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	$I_S = 1.7\text{ A}$	0.68	1.2	V
		P		$I_S = -1.7\text{ A}$	-0.7	-1.2	
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0\text{ V},$ $dI_S / dt = 100\text{ A}/\mu\text{s}$	$I_S = 1.7\text{ A}$	13.5		ns
		P		$I_S = -1.7\text{ A}$	12.6		
Charge Time	t_a	N		$I_S = 1.7\text{ A}$	8.6		
		P		$I_S = -1.7\text{ A}$	8.4		
Discharge Time	t_b	N		$I_S = 1.7\text{ A}$	4.9		
		P		$I_S = -1.7\text{ A}$	4.2		
Reverse Recovery Charge	Q_{RR}	N		$I_S = 1.7\text{ A}$	7.0		nC
		P		$I_S = -1.7\text{ A}$	6.0		

NTHD3102C

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

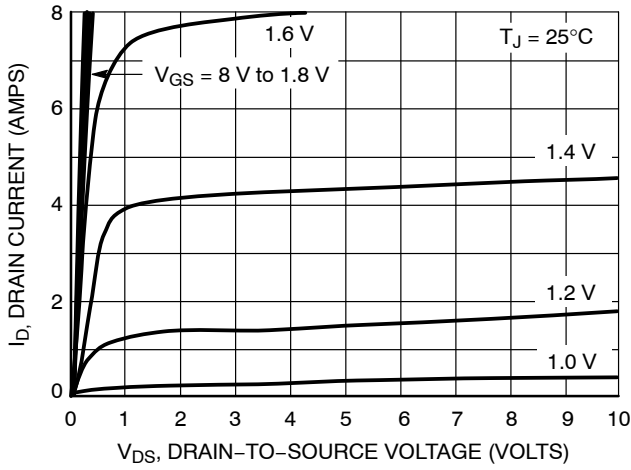


Figure 1. On-Region Characteristics

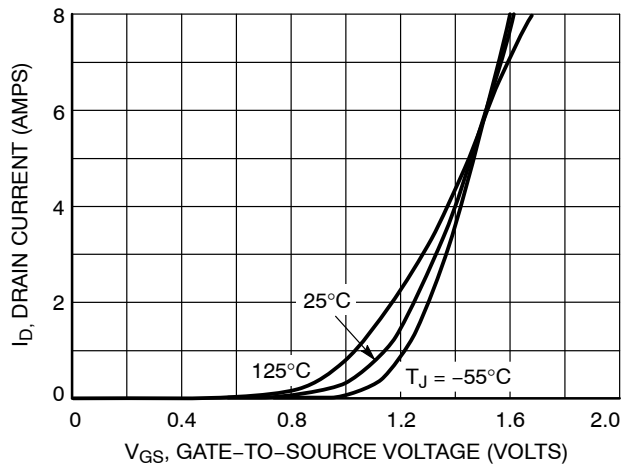


Figure 2. Transfer Characteristics

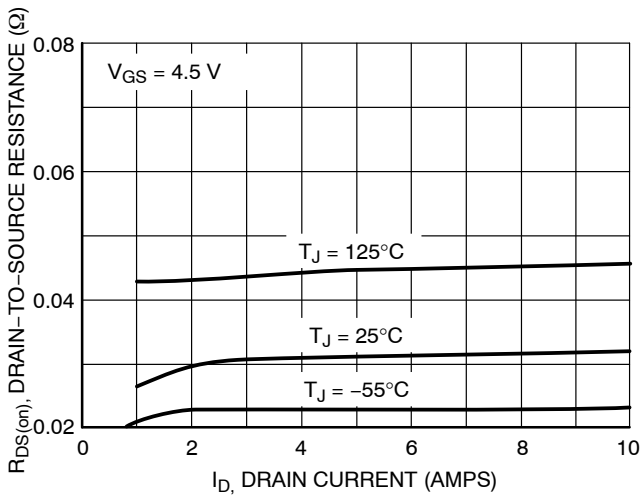


Figure 3. On-Resistance vs. Drain Current

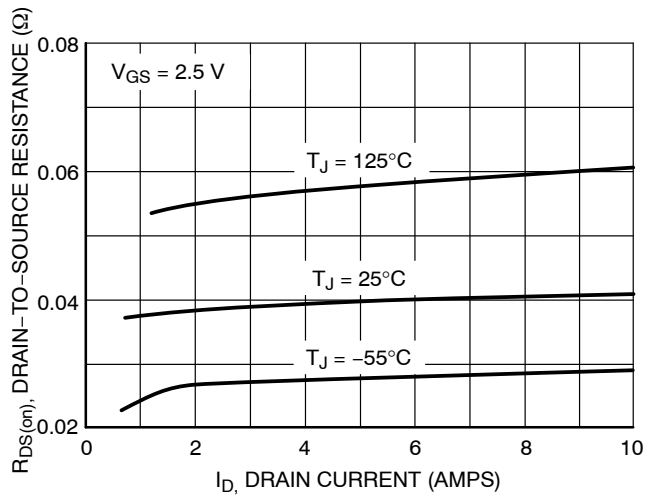


Figure 4. On-Resistance vs. Drain Current and Temperature

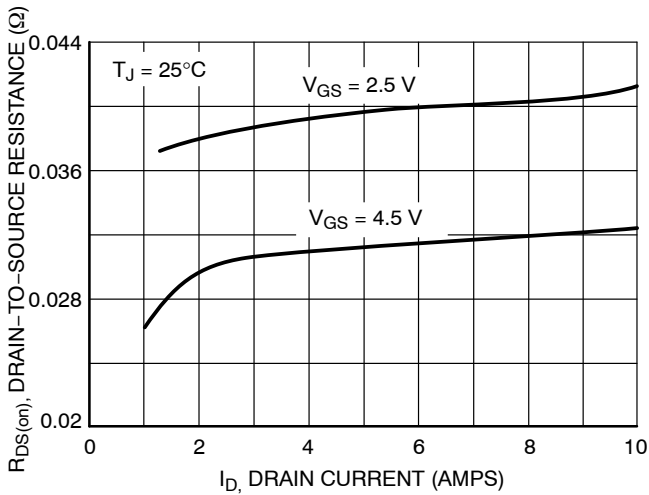


Figure 5. On-Resistance vs. Drain Current

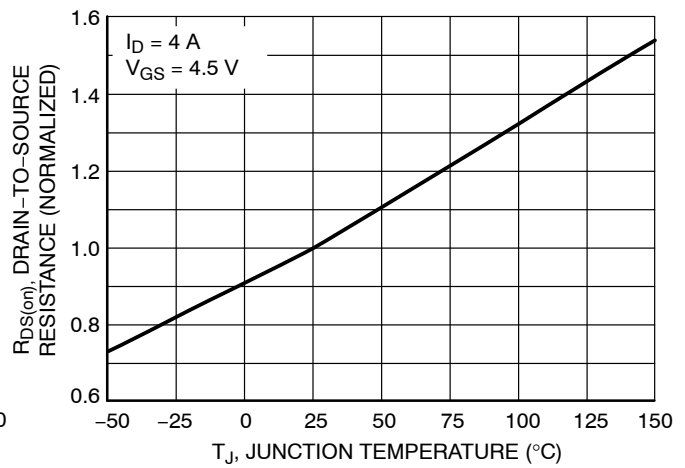


Figure 6. On-Resistance Variation with Temperature

NTHD3102C

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

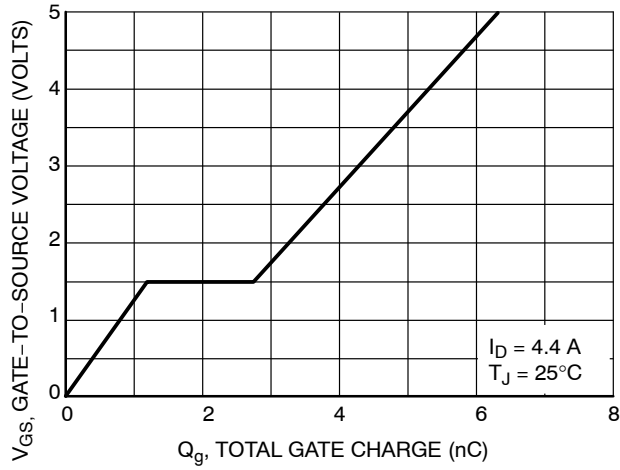


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

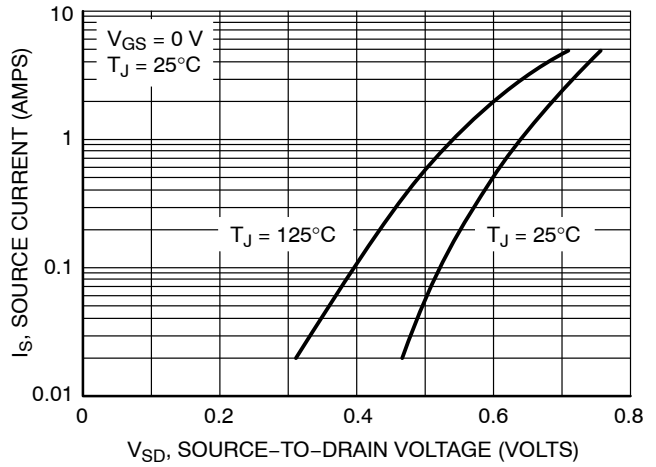


Figure 8. Diode Forward Voltage vs. Current

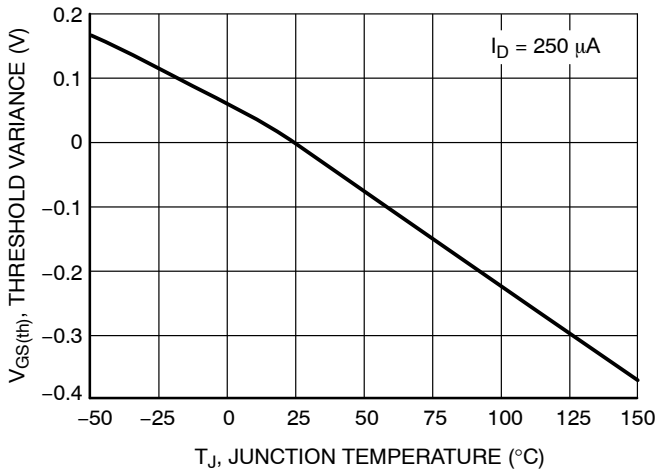


Figure 9. Threshold Voltage

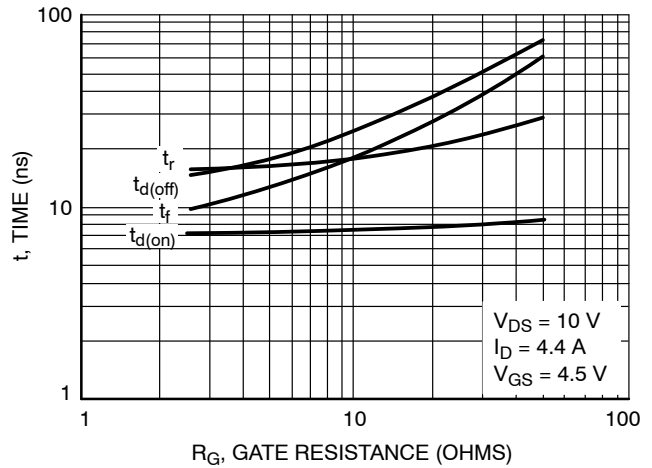


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

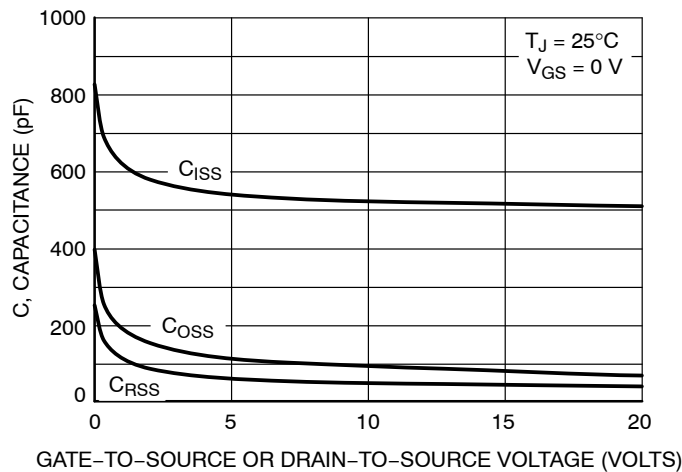


Figure 11. Capacitance Variation

NTHD3102C

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

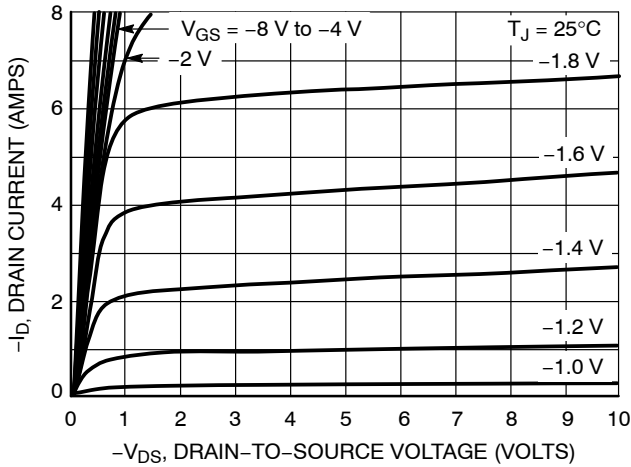


Figure 12. On-Region Characteristics

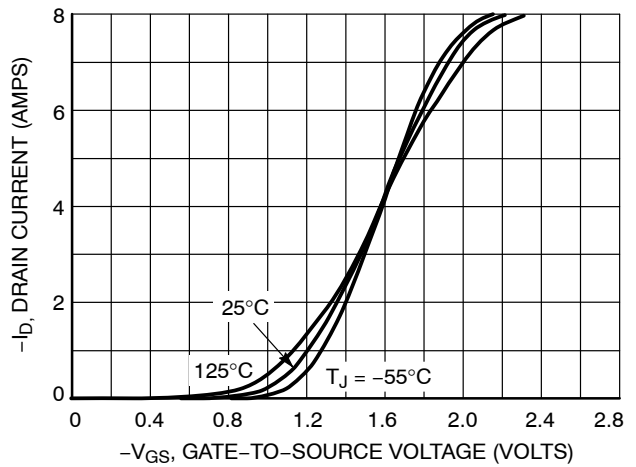


Figure 13. Transfer Characteristics

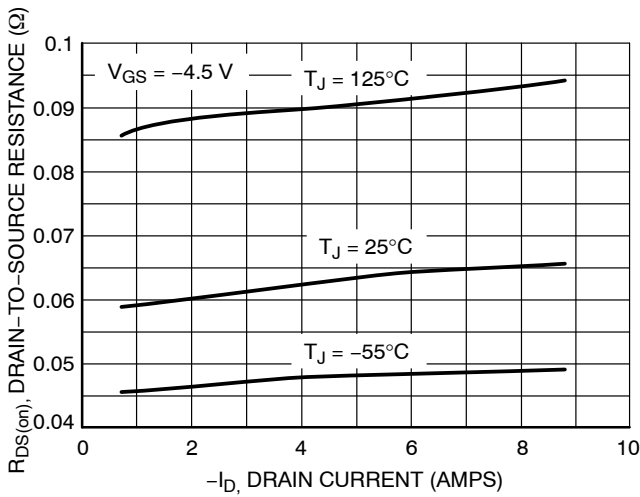


Figure 14. On-Resistance vs. Drain Current

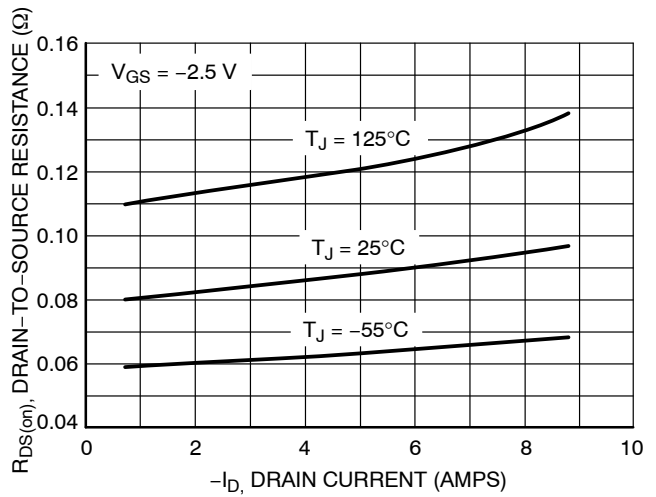


Figure 15. On-Resistance vs. Drain Current and Temperature

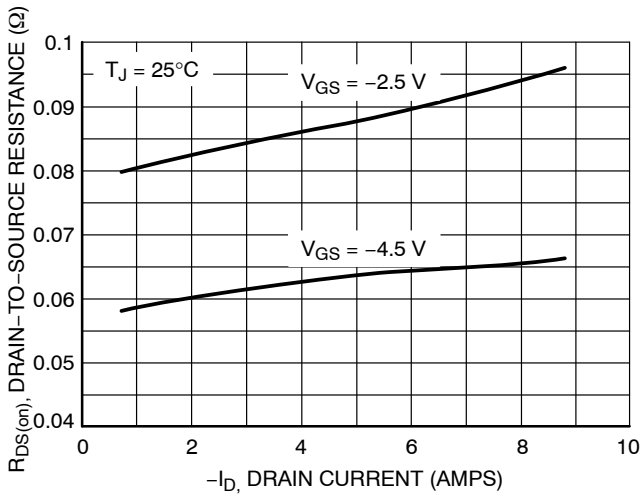


Figure 16. On-Resistance vs. Drain Current

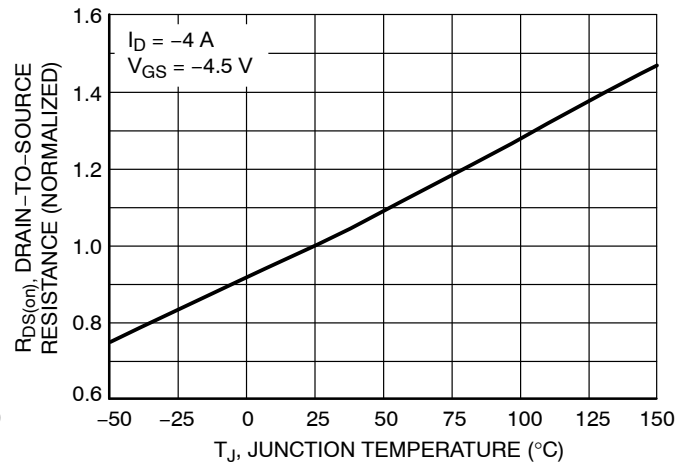


Figure 17. On-Resistance Variation with Temperature

NTHD3102C

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

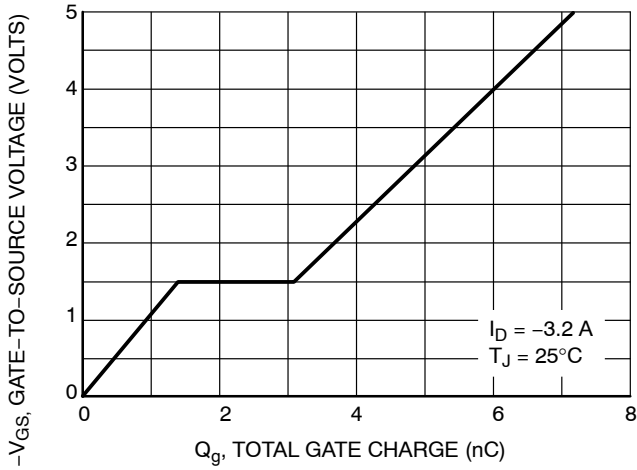


Figure 18. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

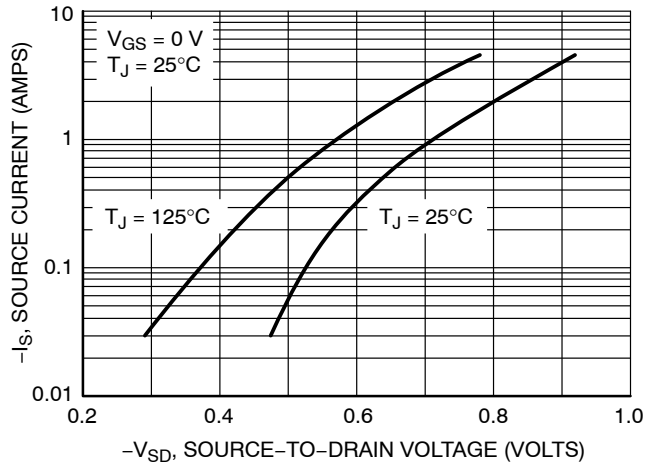


Figure 19. Diode Forward Voltage vs. Current

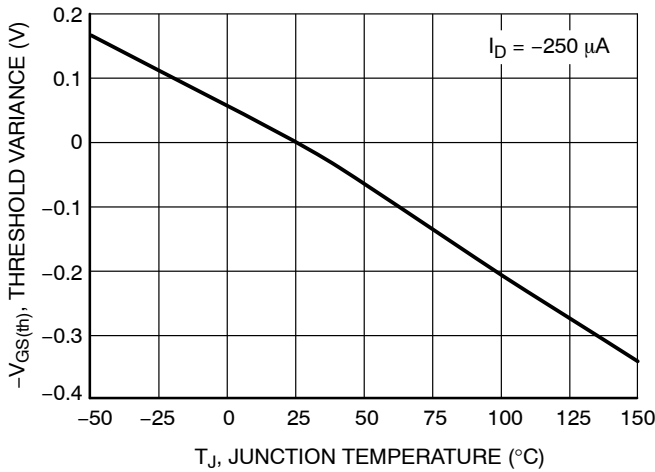


Figure 20. Threshold Voltage

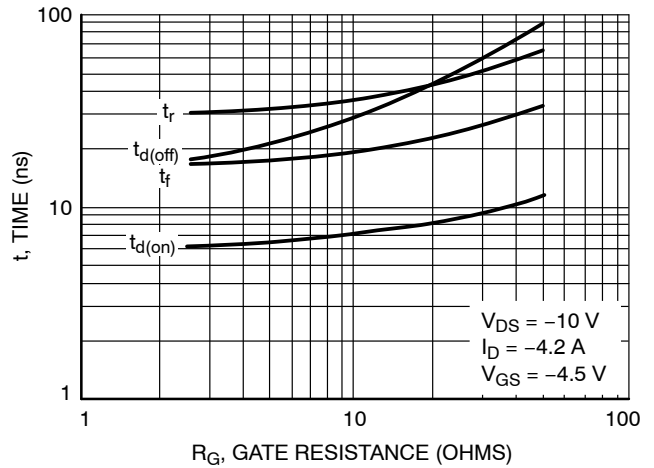


Figure 21. Resistive Switching Time Variation vs. Gate Resistance

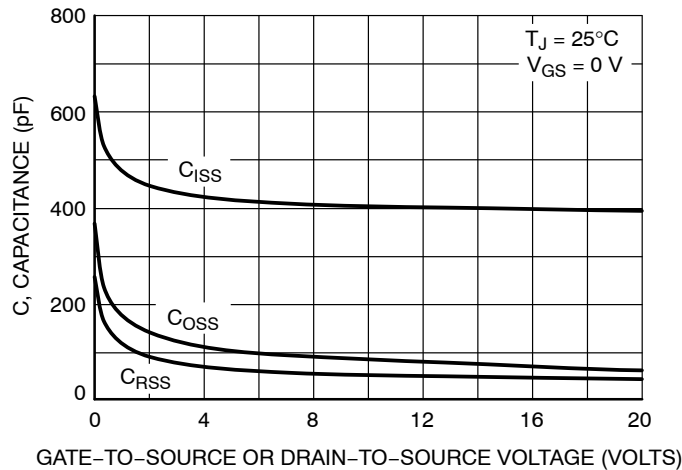


Figure 22. Capacitance Variation

NTHD3102C

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

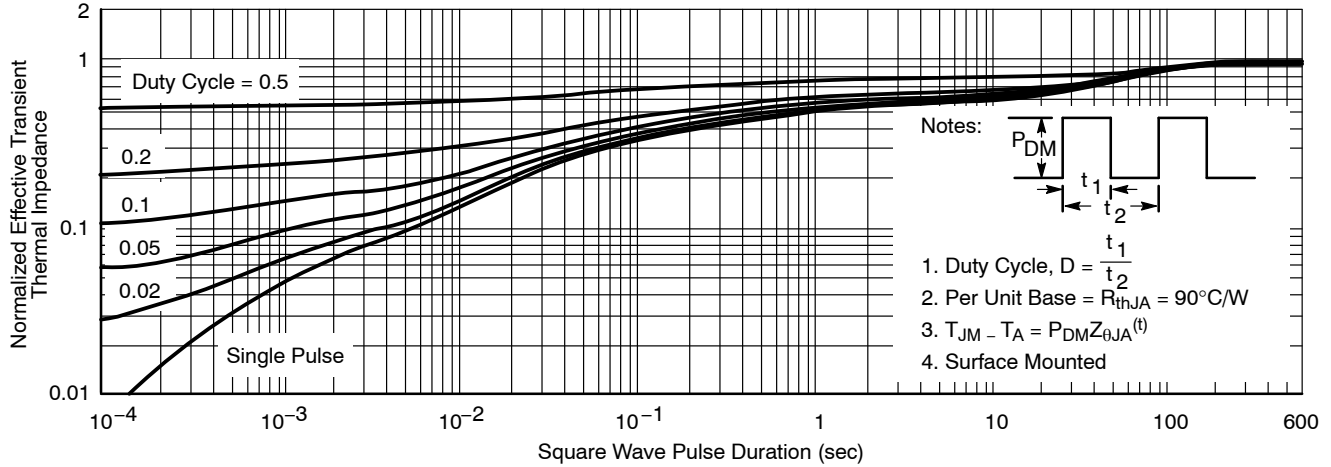


Figure 23. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTHD3102CT1G	ChipFET (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

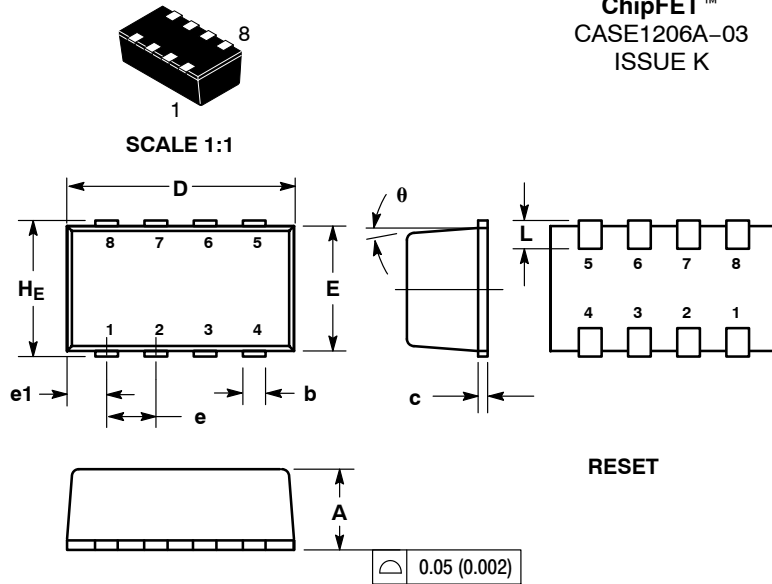
PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™ CASE1206A-03 ISSUE K

DATE 19 MAY 2009



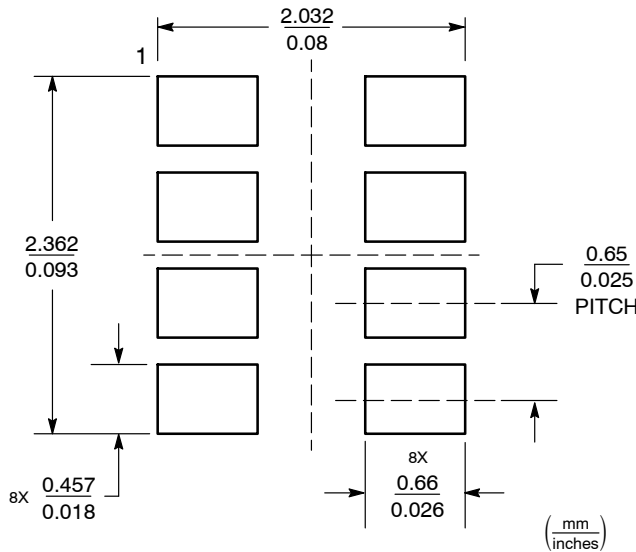
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

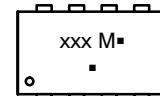
- | | | | | | |
|---|---|---|--|---|---|
| STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN | STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1 | STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE | STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR | STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE | STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN |
|---|---|---|--|---|---|

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
 - M = Month Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

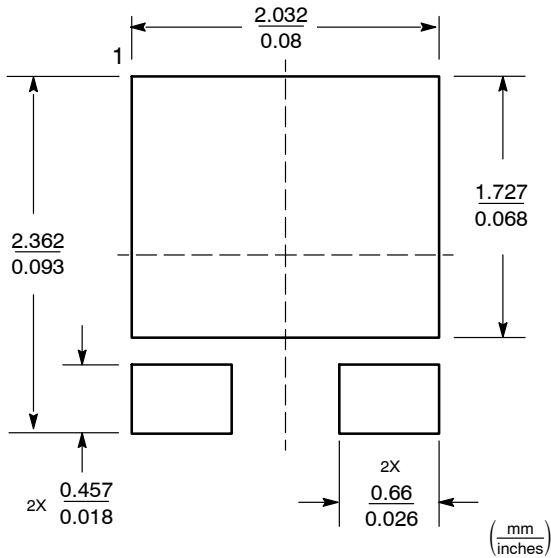
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

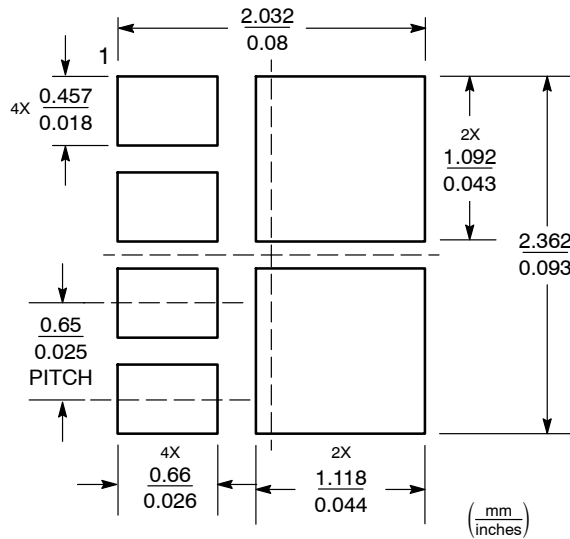
DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

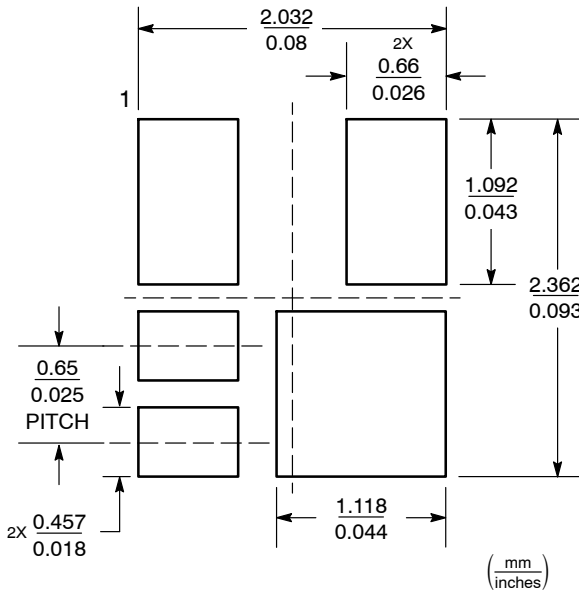
ADDITIONAL SOLDERING FOOTPRINTS*



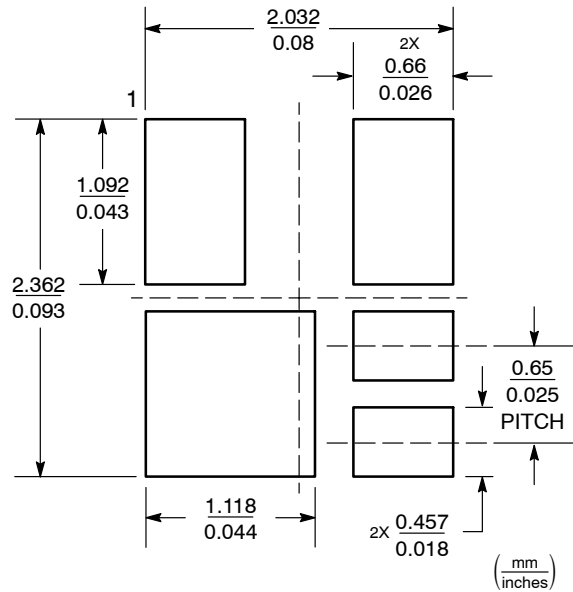
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 2 OF 2

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales