

# NTHD2110T

## Power MOSFET

-12 V, -6.4 A, Single P-Channel +TVS,  
ChipFET™ Package

### Features

- Low  $R_{DS(on)}$  MOSFET and TVS Diode ChipFET Package
- Integrated Drain Side TVS for 15 kV Contact Discharge ESD Protection
- 1.8 V Gate Rating
- This is a Pb-Free Device

### Applications

- Battery Switch and Load Management Applications in Portable Equipment

### MOSFET MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	-12	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 8$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-4.5	A
		$T_A = 85^\circ\text{C}$	-3.2	
		$t \leq 5 \text{ s}$	-6.4	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.1	W
		$t \leq 5 \text{ s}$	2.3	
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Storage Temperature Range	$T_J$	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	$T_L$	260	$^\circ\text{C}$	

### TVS MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 ms Double Exponential Waveform (Note 2)	PPK	150	W
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Specification (Contact)	ESD	16	kV
		400	V
		30	kV

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	110	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 5 \text{ s}$ (Note 1)	$R_{\theta JA}$	55	
Junction-to-Ambient - Steady State Min Pad (Note 3)	$R_{\theta JA}$	225	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Nonrepetitive Current Pulse per Figure 11.
3. Surface Mounted on FR4 board using 1 in sq size (Cu area = 1.127 in sq [1 oz] included traces).



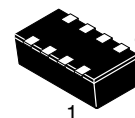
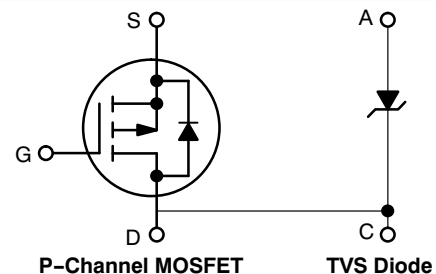
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-12 V	40 m $\Omega$ @ -4.5 V	-6.4 A
	53 m $\Omega$ @ -2.5 V	
	80 m $\Omega$ @ -1.8 V	

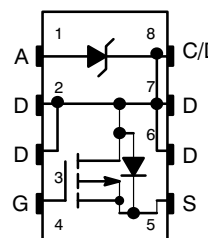
### TVS

$V_{RWM}$	$V_C$ @ MAX $I_{PP}$	$I_{PP}$ MAX
12	21.5	6.2 A

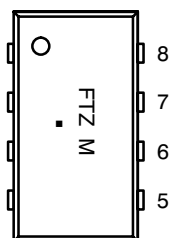


ChipFET  
CASE 1206A  
STYLE 6

### PIN CONNECTIONS



### MARKING DIAGRAM



FTZ = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTHD2110TT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHD2110T

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(Br)DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>dc</sub> , I <sub>D</sub> = -250 μA	-12			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C		-1.0	μA
			T <sub>J</sub> = 85°C		-5.0	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8.0 V			±0.1	μA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.40		-0.85	V
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.4 A		33	40	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.0 A		42	53	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -1.7 A		57	80	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5.0 V, I <sub>D</sub> = -6.4 A		13.7		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -6.0 V, V <sub>GS</sub> = 0 V f = 1.0 MHz		1072		pF
Output Capacitance	C <sub>oss</sub>			260		
Reverse Transfer Capacitance	C <sub>rss</sub>			134		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -6.0 V, I <sub>D</sub> = -6.4 A		10.5	14	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.6		
Gate-to-Source Charge	Q <sub>GS</sub>			1.3		
Gate-to-Drain Charge	Q <sub>GD</sub>			2.8		

### SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -6.0 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.0 A, R <sub>G</sub> = 6.0 Ω		7.5		ns
Rise Time	t <sub>r</sub>			8.6		
Turn-Off Delay Time	t <sub>d(off)</sub>			99.7		
Fall Time	t <sub>f</sub>			49.8		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = -1.7 A, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C		-0.7	-1.0	V
			T <sub>J</sub> = 125°C		-0.6		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> / dt = 100 A/μs, I <sub>S</sub> = -1.7 A		41.7		ns	
Reverse Recovery Charge	Q <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> / dt = 100 A/μs, I <sub>S</sub> = -1.7 A		22		nC	

4. Surface Mounted on FR4 board using 1 in sq size (Cu area = 1.127 in sq [1 oz] included traces).
5. Surface mounted on FR4 board using the minimum recommended pad size.
6. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>TVS DIODE</b>						
Reverse Working Voltage (Note 8)	V <sub>RWM</sub>		12			V
Breakdown Voltage (Note 9)	V <sub>BR</sub>	I <sub>T</sub> = 1 mA	14.5		15.7	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 12 V		0.6	10	nA
Clamping Voltage (Note 10)	V <sub>C</sub>	I <sub>PP</sub> = 1 A (8 x 20 μs Waveform)			15.7	V
Clamping Voltage (Note 10)	V <sub>C</sub>	I <sub>PP</sub> = 5 A (8 x 20 μs Waveform)			19.1	V
Maximum Peak Pulse Current (Note 10)	I <sub>PP</sub>	8 x 20 μs Waveform			6.2	A
Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V, f = 1 MHz (Anode-to-GND)			60	pF

8. TVS devices are normally selected according to the working peak reverse voltage (V<sub>RWM</sub>), which should be equal or greater than the DC or continuous peak operating voltage level.

9. V<sub>BR</sub> is measured at pulse test current I<sub>T</sub>.

10. Pulse waveform per Figure 11.

TYPICAL MOSFET PERFORMANCE CURVES

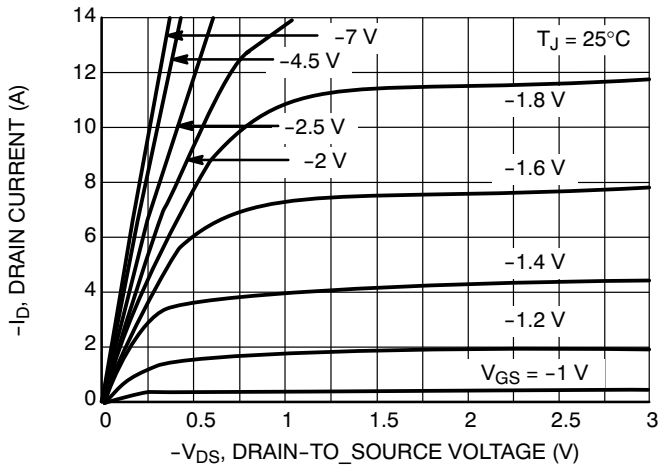


Figure 1. On-Region Characteristics

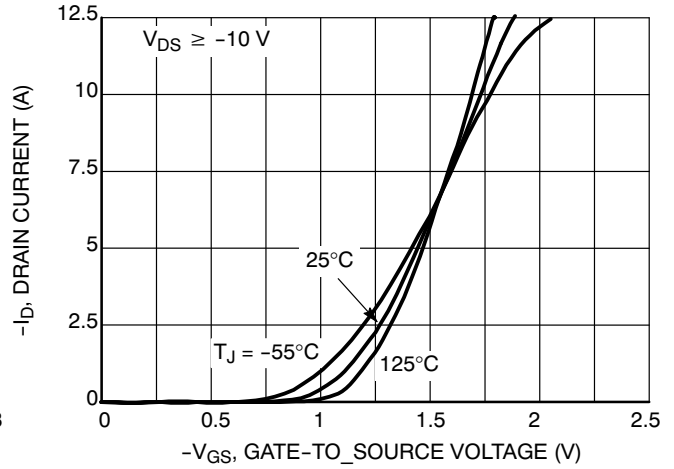


Figure 2. Transfer Characteristics

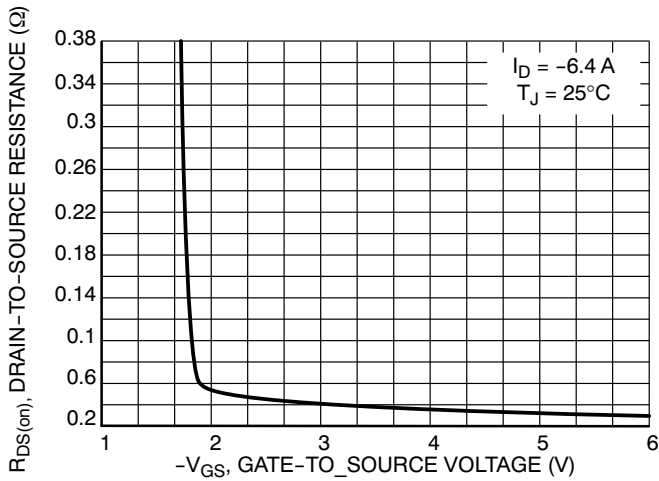


Figure 3. On-Resistance vs. Gate Voltage

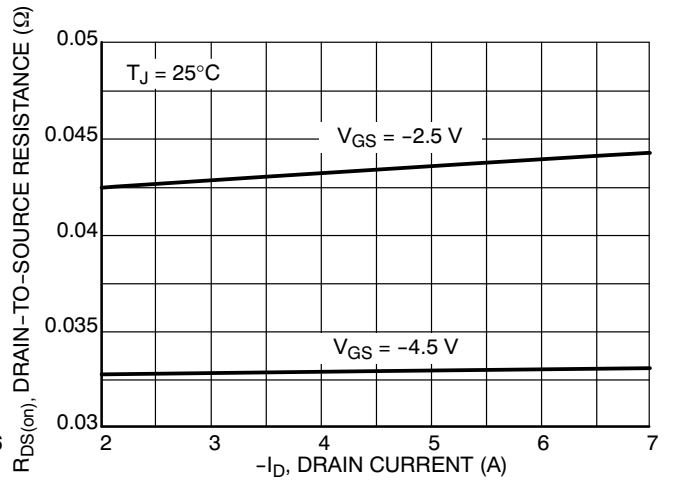


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

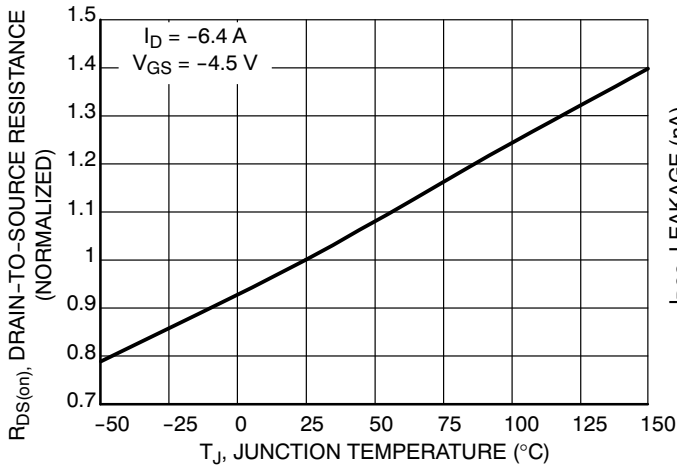


Figure 5. On-Resistance Variation with Temperature

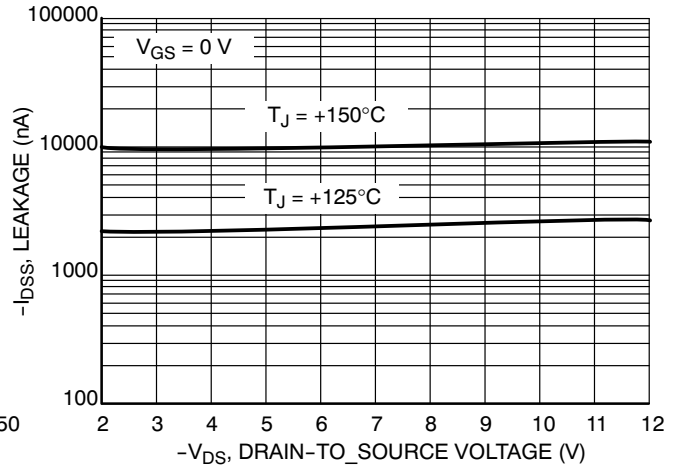


Figure 6. Drain-to-Source Leakage Current

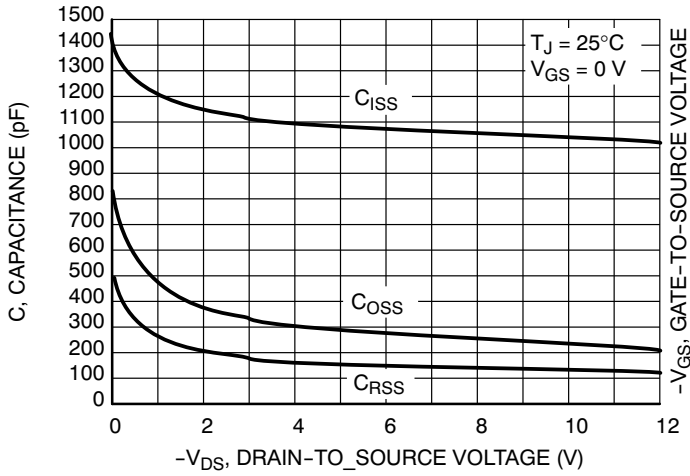


Figure 7. Capacitance Variation

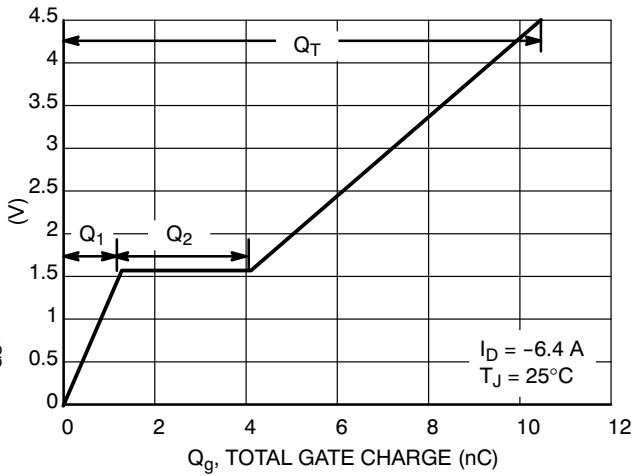


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

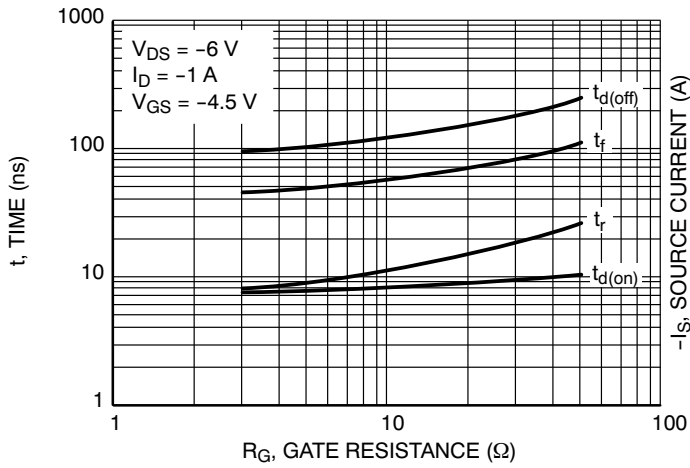


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

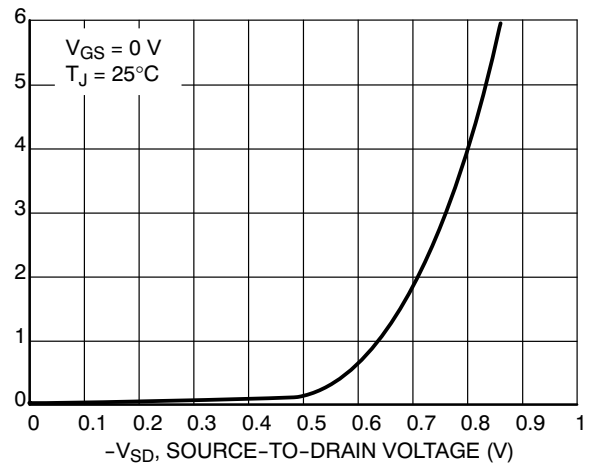


Figure 10. Diode Forward Voltage vs. Current

TYPICAL TVS PERFORMANCE CURVES

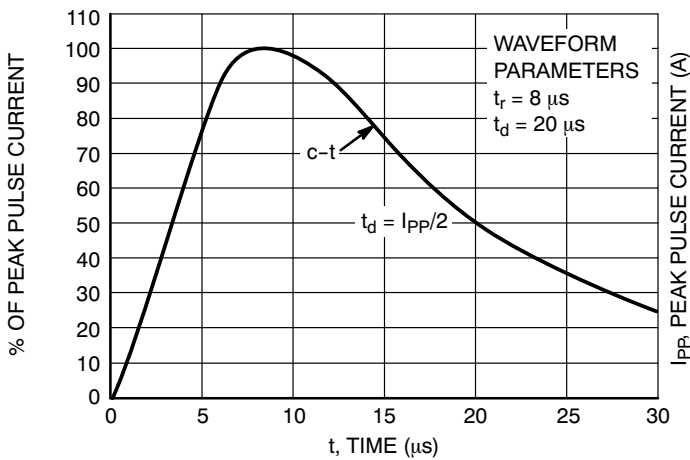


Figure 11. Pulse Waveform,  $8 \times 20\ \mu\text{s}$

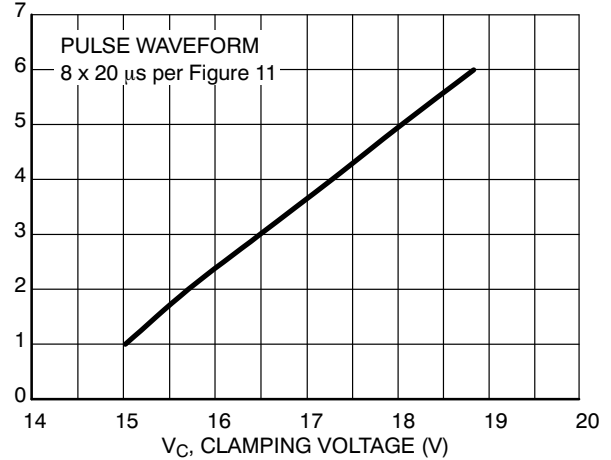


Figure 12. Clamping Voltage vs Peak Pulse Current

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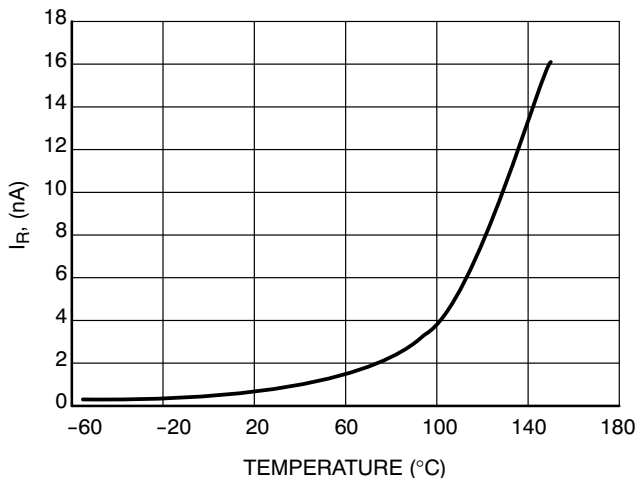


Figure 13. Typical Leakage vs. Temperature

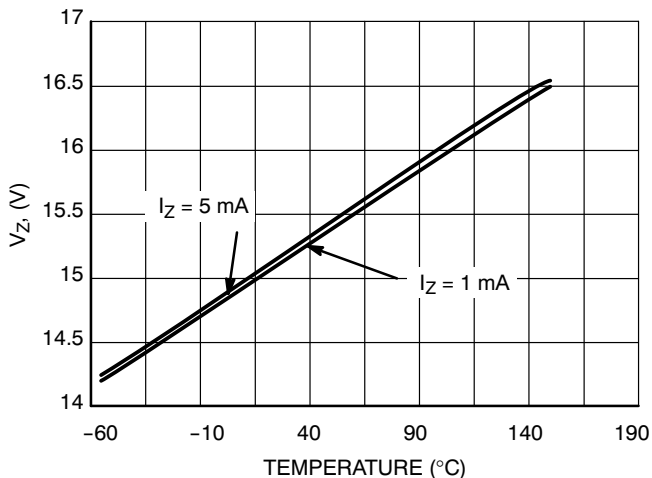


Figure 14. Typical  $V_Z$  @ 1 mA vs. Temperature

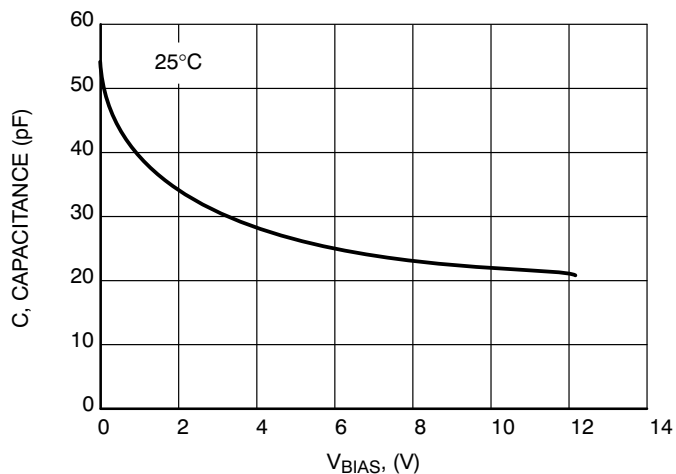


Figure 15. Capacitance vs.  $V_{BIAS}$

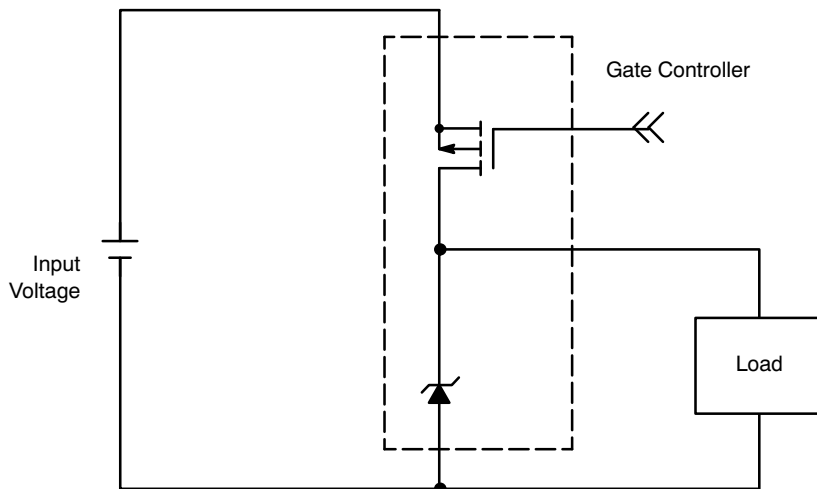


Figure 16. Typical Application Circuit

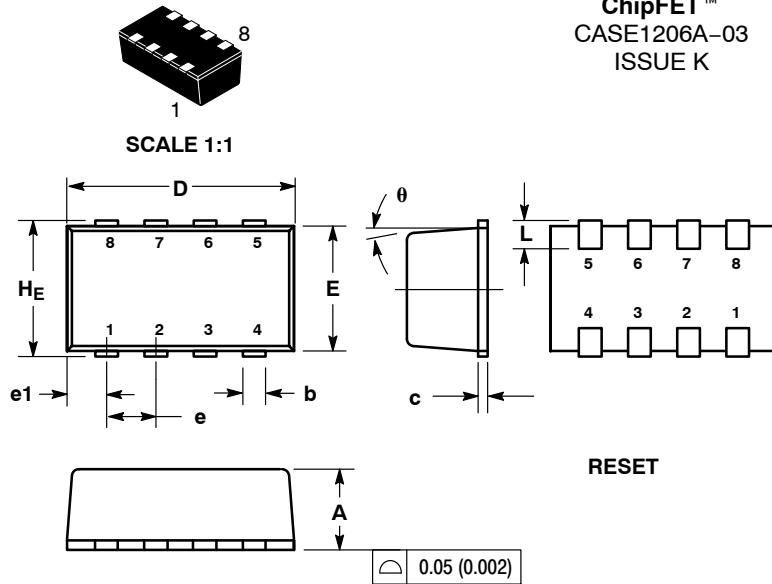
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## ChipFET™ CASE1206A-03 ISSUE K

DATE 19 MAY 2009



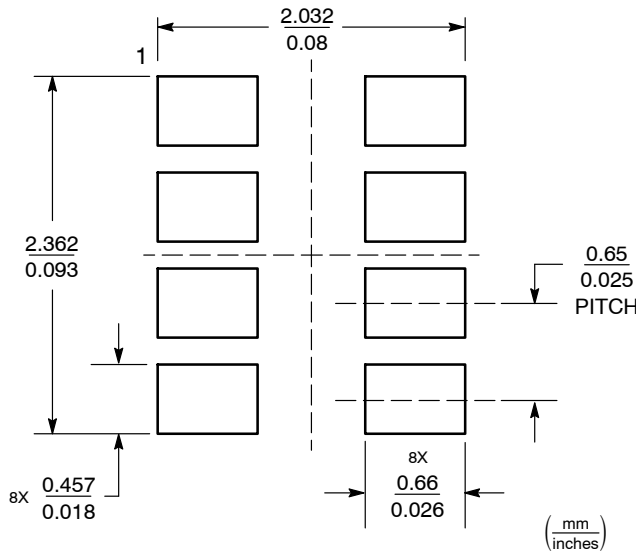
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

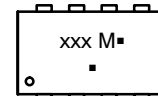
- |   |   |   |  |   |   |
|---|---|---|--|---|---|
| <b>STYLE 1:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. GATE<br>5. SOURCE<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN | <b>STYLE 2:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1 | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE | <b>STYLE 4:</b><br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. COLLECTOR<br>4. BASE<br>5. EMITTER<br>6. COLLECTOR<br>7. COLLECTOR<br>8. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. DRAIN<br>4. DRAIN<br>5. SOURCE<br>6. GATE<br>7. CATHODE<br>8. CATHODE | <b>STYLE 6:</b><br>PIN 1. ANODE<br>2. DRAIN<br>3. DRAIN<br>4. GATE<br>5. SOURCE<br>6. DRAIN<br>7. DRAIN<br>8. CATHODE / DRAIN |
|---|---|---|--|---|---|

### SOLDERING FOOTPRINT



### Basic Style

### GENERIC MARKING DIAGRAM\*



- xxx = Specific Device Code
  - M = Month Code
  - = Pb-Free Package
- (Note: Microdot may be in either location)

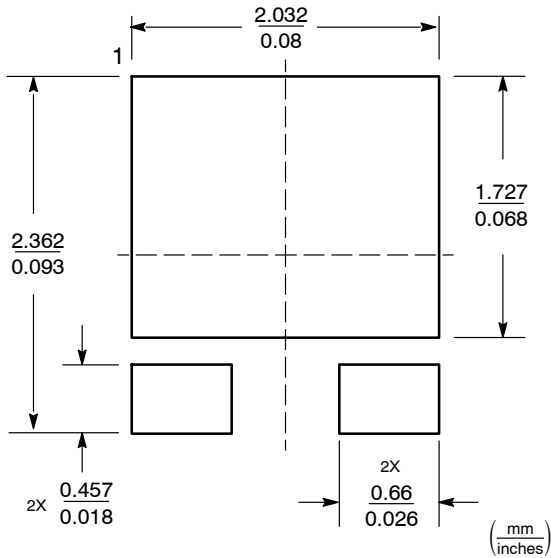
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

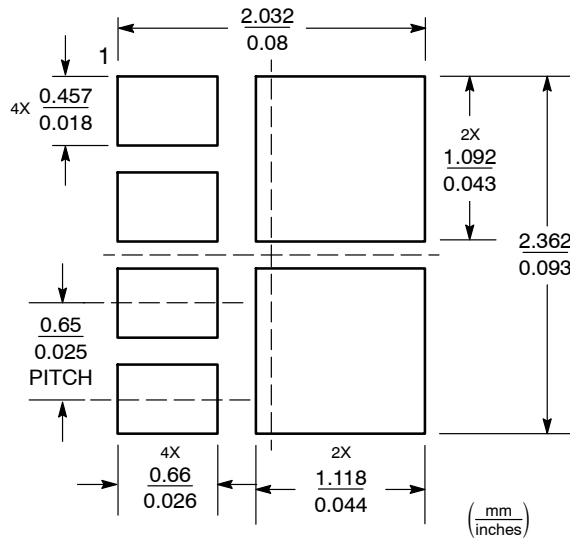
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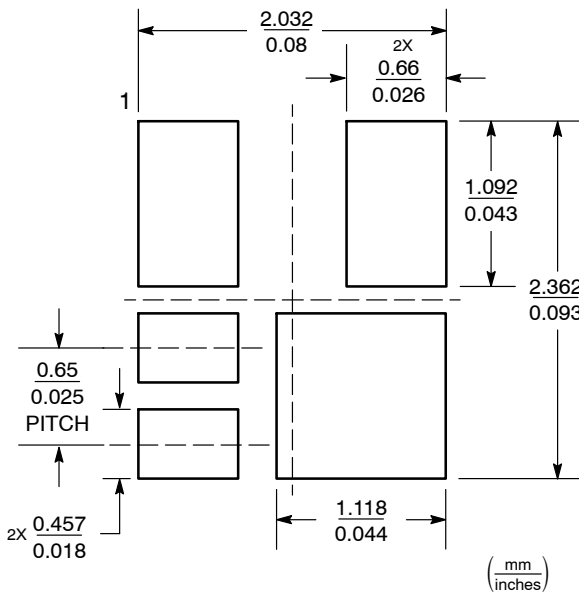
ADDITIONAL SOLDERING FOOTPRINTS\*



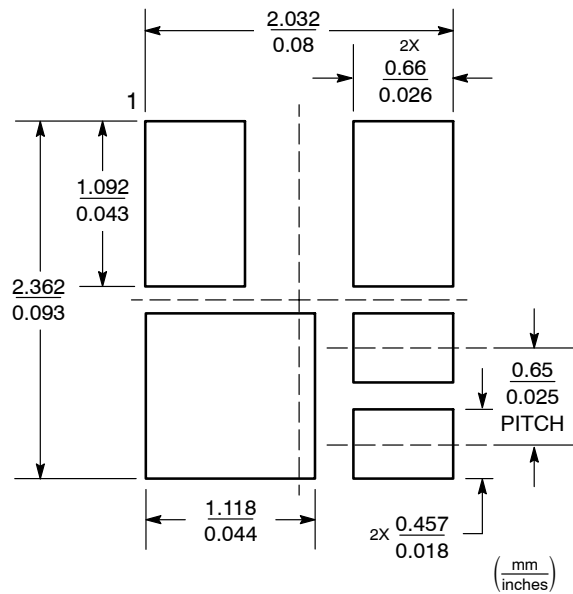
Styles 1 and 4



Style 2



Style 3



Style 5

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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