

NTHD2102P

Power MOSFET

-8.0 V, -4.6 A Dual P-Channel ChipFET™

Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low $R_{DS(on)}$ at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb-Free Package is Available

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-8.0	V
Gate-to-Source Voltage - Continuous	V_{GS}	± 8.0	V
Drain Current - Continuous - 5 seconds	I_D	-3.4	A
	I_D	-4.6	A
Total Power Dissipation Continuous @ $T_A = 25^\circ\text{C}$ (5 sec) @ $T_A = 25^\circ\text{C}$ Continuous @ 85°C (5 sec) @ 85°C	P_D	1.1	W
		2.1	
		0.6	
		1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Continuous Source Current (Diode Conduction)	I_S	-1.1	A
Thermal Resistance (Note 1) Junction-to-Ambient, 5 sec Junction-to-Ambient, Continuous	$R_{\theta JA}$ $R_{\theta JA}$	60	$^\circ\text{C}/\text{W}$
		113	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

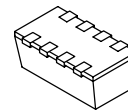
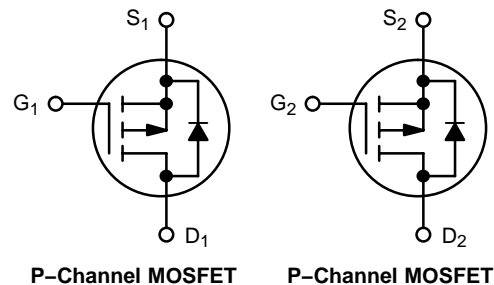
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



ON Semiconductor®

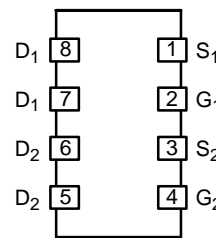
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-8.0 V	50 m Ω @ -4.5 V	-4.6 A
	68 m Ω @ -2.5 V	
	100 m Ω @ -1.8 V	

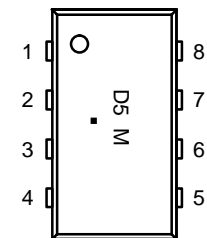


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



D5 = Specific Device Code
M = Month Code
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD2102PT1	ChipFET	3000/Tape & Reel
NTHD2102PT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD2102P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
----------------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	V _{(Br)DSS}	V _{GS} = 0 V, I _D = -250 μA	-8.0	-	-	V
Gate-Body Leakage Current Zero	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8.0 V		-	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -6.4 V, V _{GS} = 0 V V _{DS} = -6.4 V, V _{GS} = 0 V, T _J = 85°C		-	-1.0 -5.0	μA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.45	-	-1.5	V
Static Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.4 A V _{GS} = -2.5 V, I _D = -2.7 A V _{GS} = -1.8 V, I _D = -1.0 A	-	50 68 100	58 85 160	mΩ
Forward Transconductance	g _{FS}	V _{DS} = -5.0 V, I _D = -3.4 A	-	8.0	-	S
Diode Forward Voltage	V _{SD}	I _S = -1.1 A, V _{GS} = 0 V	-	-0.8	-1.2	V

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iSS}	V _{DS} = -6.4 V	-	715	-	pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V	-	160	-	
Transfer Capacitance	C _{rSS}	f = 1.0 MHz	-	120	-	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{DD} = -6.4 V		8.0	-	ns
Rise Time	t _r	V _{GS} = -4.5 V		20	-	
Turn-Off Delay Time	t _{d(off)}	I _D = -3.2 A		20	-	
Fall Time	t _f	R _G = 2.0 Ω		15	-	
Gate Charge	Q _g	V _{GS} = -2.5 V		8.0	16	nC
	Q _{gs}	I _D = -3.2 A		2.2	-	
	Q _{gd}	V _{DS} = -6.4 V		4.0	-	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -0.9 A, di/dt = 100		15	30	nA

2. Pulse Test: Pulse Width = 250 μs, Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

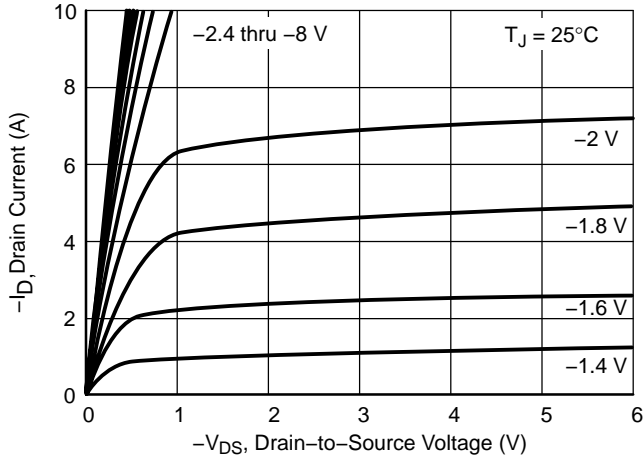


Figure 1. On-Region Characteristics

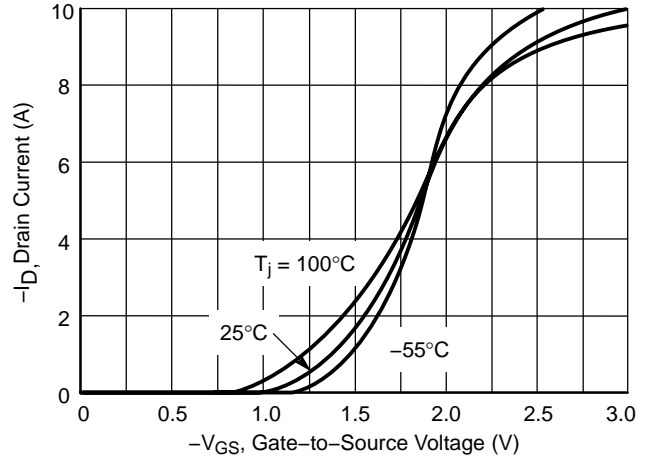


Figure 2. Transfer Characteristics

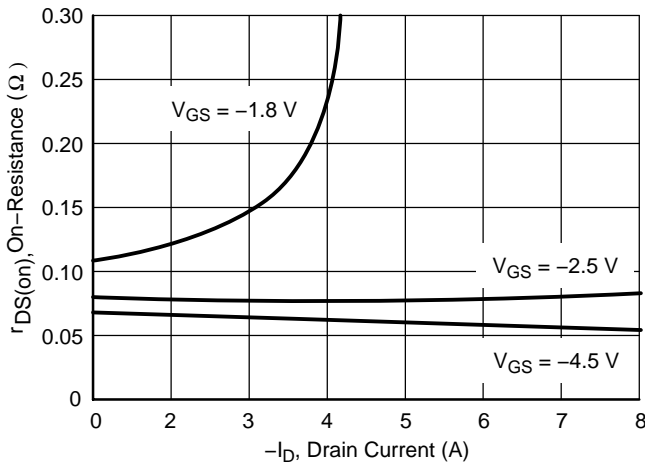


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

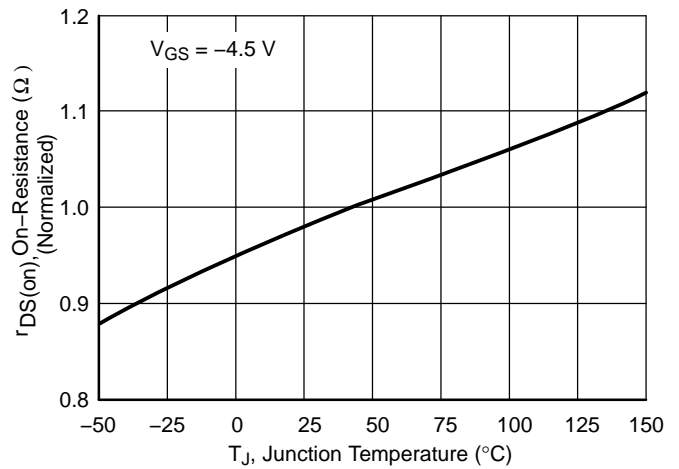


Figure 4. On-Resistance Variation vs. Temperature

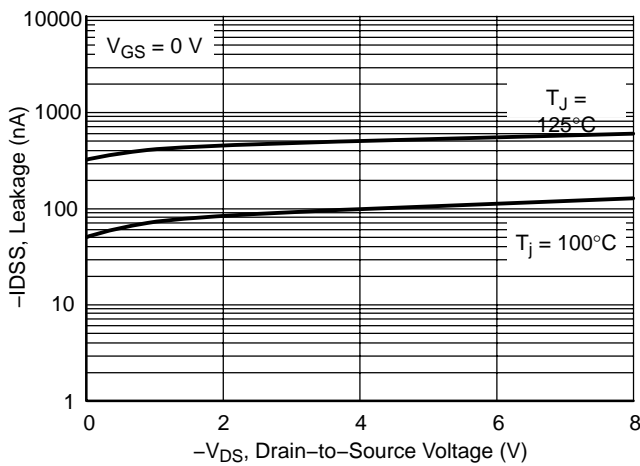


Figure 5. Drain-to-Source Leakage Current vs. Voltage

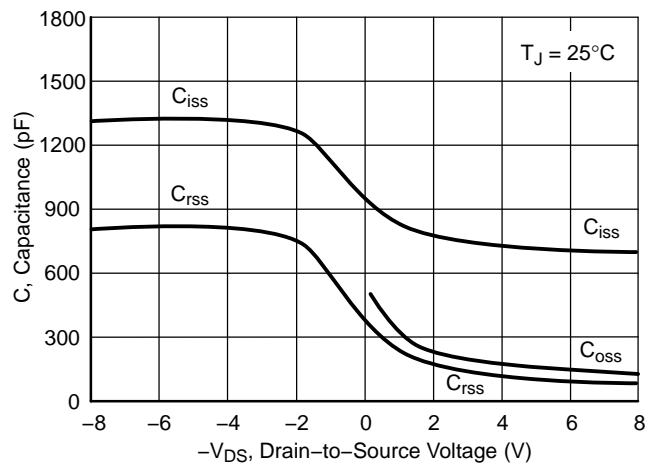


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

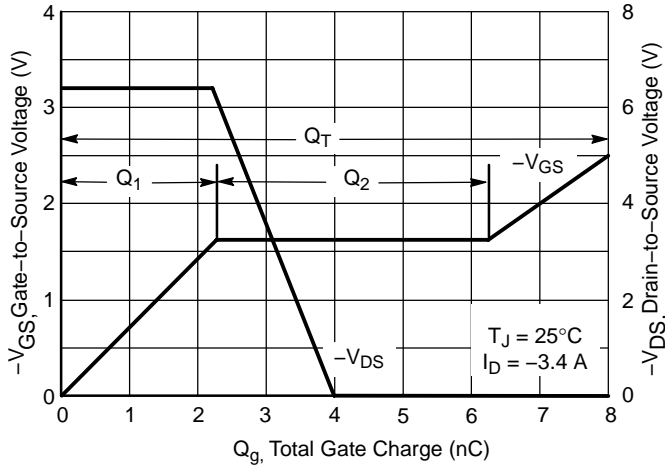


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

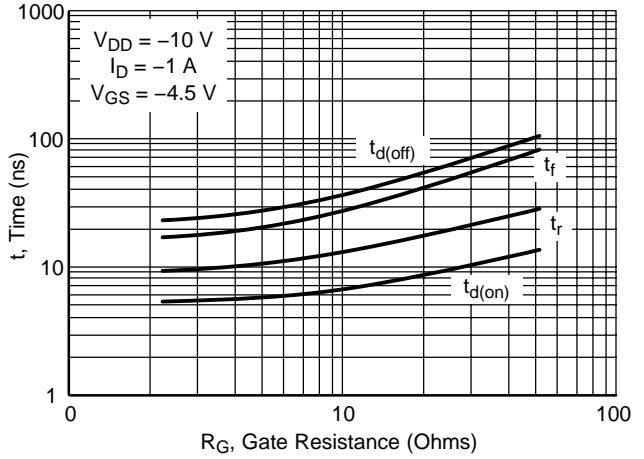


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

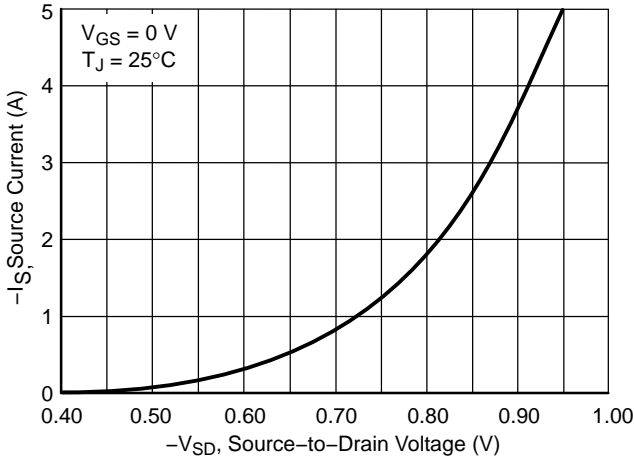


Figure 9. Diode Forward Voltage vs. Current

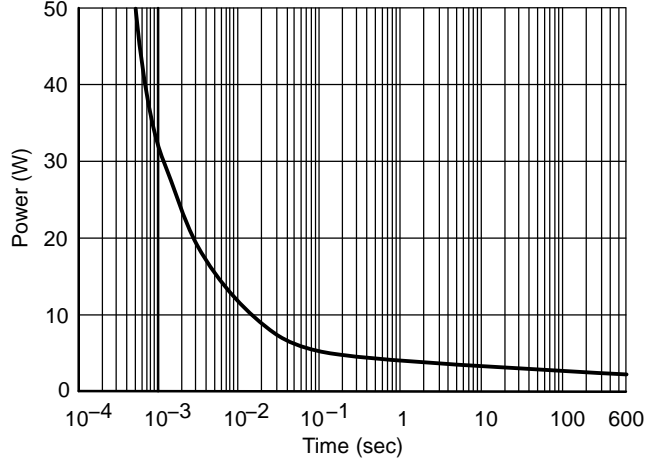


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

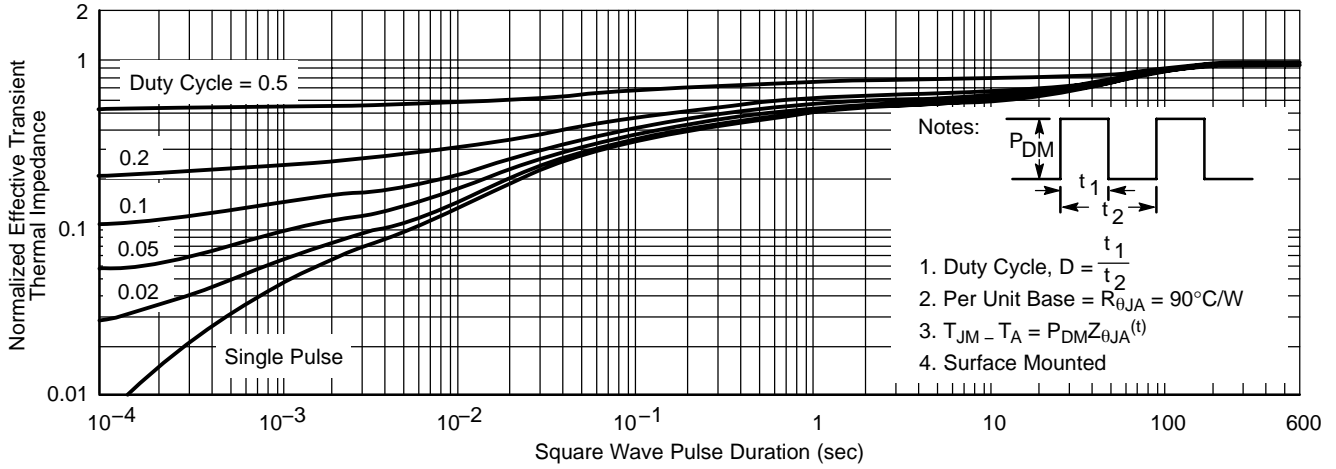


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

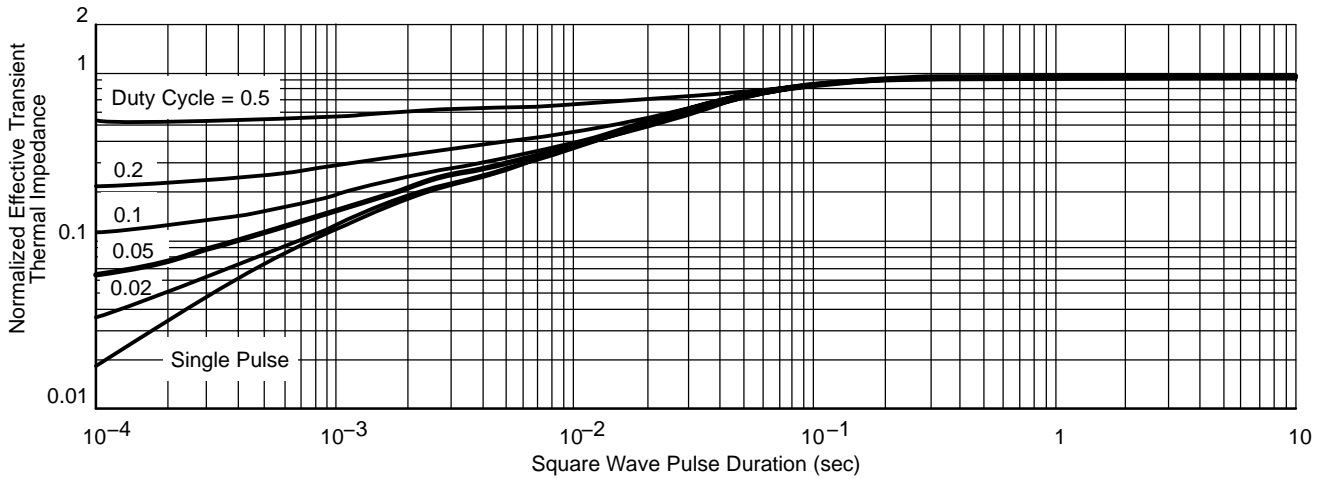


Figure 12. Normalized Thermal Transient Impedance, Junction-to-Foot

MECHANICAL CASE OUTLINE

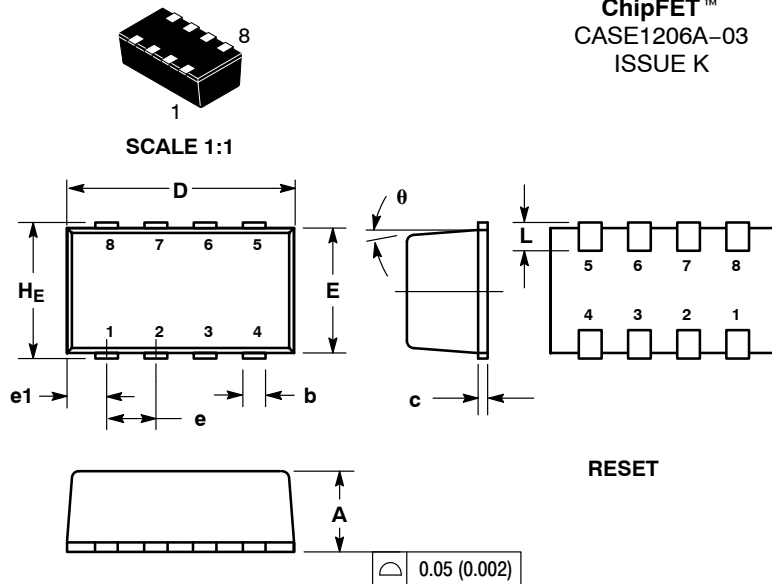
PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™ CASE1206A-03 ISSUE K

DATE 19 MAY 2009



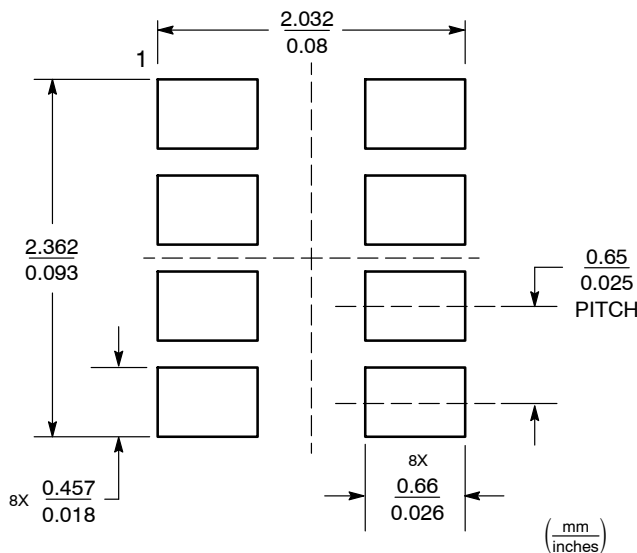
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

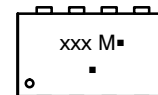
- | | | | | | |
|---|---|---|--|---|---|
| STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN | STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1 | STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE | STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR | STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE | STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN |
|---|---|---|--|---|---|

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
 - M = Month Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

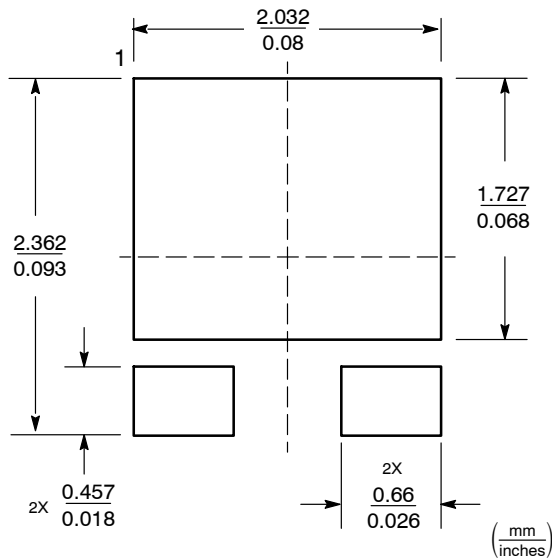
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

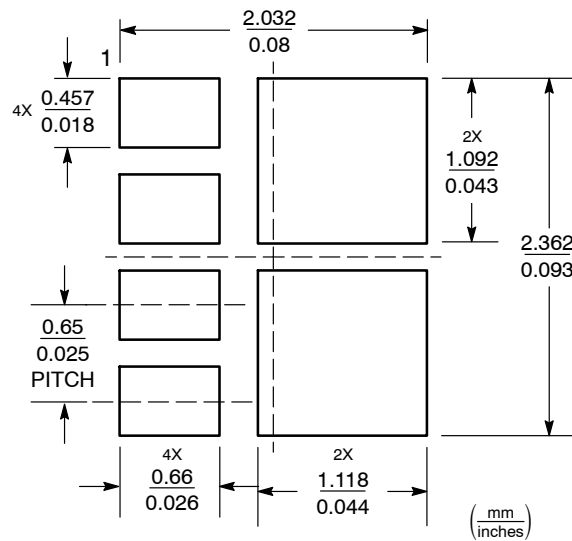
DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

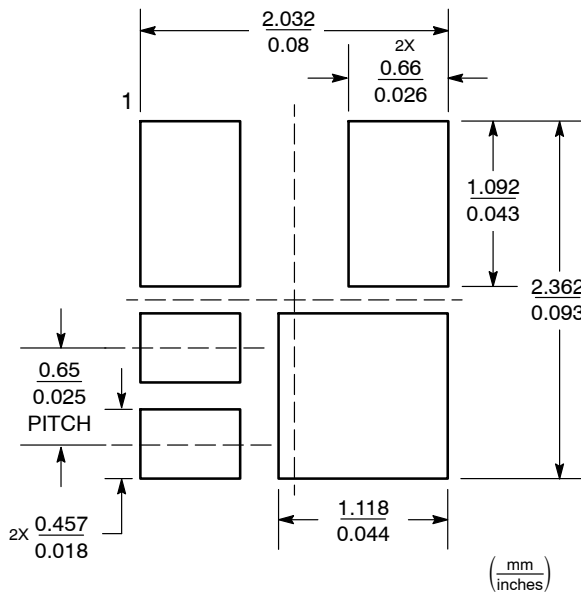
ADDITIONAL SOLDERING FOOTPRINTS*



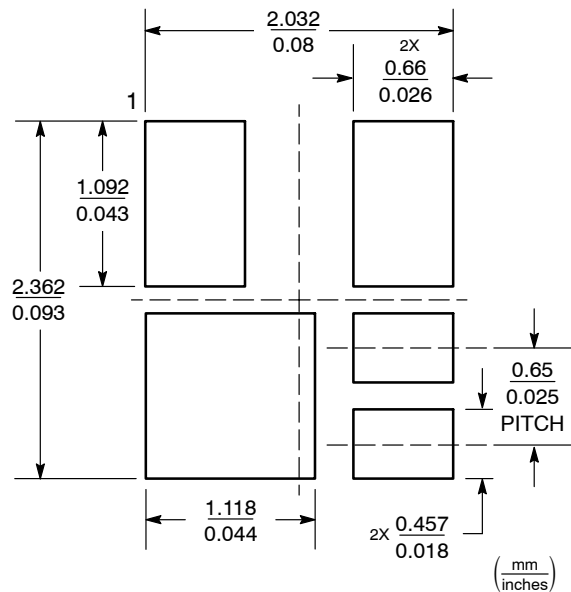
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 2 OF 2

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales