

NTGD3149C

Power MOSFET

Complementary, 20 V, +3.5/-2.7 A,
TSOP-6 Dual

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size (3 x 3 mm) Dual TSOP-6 Package
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb-Free Device

Applications

- DC-DC Conversion Circuits
- Load/Power Switching with Level Shift

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	20	V
Gate-to-Source Voltage (N-Ch & P-Ch)		V _{GS}	±8	V
N-Channel Continuous Drain Current (Note 1)	Steady State T _A = 25°C T _A = 85°C	I _D	3.2 2.3	A
	t ≤ 5 s T _A = 25°C		3.5	
P-Channel Continuous Drain Current (Note 1)	Steady State T _A = 25°C T _A = 85°C	I _D	2.4 1.7	A
	t ≤ 5 s T _A = 25°C		2.7	
Power Dissipation (Note 1)	Steady State T _A = 25°C	P _D	0.9	W
	t ≤ 5 s		1.1	
Pulsed Drain Current	N-Ch P-Ch	I _{DM}	11 8.0	A
	t _p = 10 μs			
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to 150	°C
Source Current (Body Diode)		I _S	0.8	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	R _{θJA}	140	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 1)	R _{θJA}	110	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

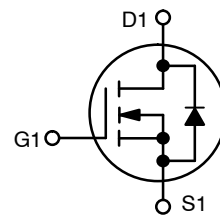
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



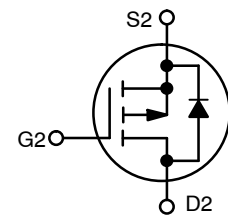
ON Semiconductor®

<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)
N-Ch 20 V	60 mΩ @ 4.5 V	3.5 A
	90 mΩ @ 2.5 V	
P-Ch -20 V	110 mΩ @ 4.5 V	-2.7 A
	145 mΩ @ 2.5 V	



N-CHANNEL MOSFET

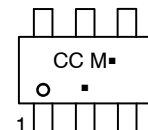


P-CHANNEL MOSFET



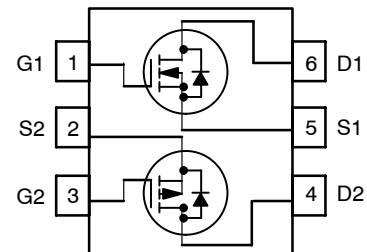
TSOP-6
CASE 318G
STYLE 13

MARKING DIAGRAM



CC = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NTGD3149C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	N	V _{GS} = 0 V	I _D = 250 μA	20		V
		P		I _D = -250 μA	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	N			1.1		mV/°C
		P			1.1		
Zero Gate Voltage Drain Current	I _{DSS}	N	V _{GS} = 0 V, V _{DS} = 16 V	T _J = 25 °C		1.0	μA
		P	V _{GS} = 0 V, V _{DS} = -16 V			-1.0	
		N	V _{GS} = 0 V, V _{DS} = 16 V	T _J = 85 °C		10	
		P	V _{GS} = 0 V, V _{DS} = -16 V			-10	
Gate-to-Source Leakage Current	I _{GSS}	N	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
		P	V _{DS} = 0 V, V _{GS} = ±8 V			±100	

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	N	V _{GS} = V _{DS}	I _D = 250 μA	0.4	1.0	V
		P		I _D = -250 μA	-0.4	-1.0	
Drain-to-Source On Resistance	R _{DS(on)}	N	V _{GS} = 4.5 V, I _D = 3.5 A		41	60	mΩ
		P	V _{GS} = -4.5 V, I _D = -2.7 A		83	110	
		N	V _{GS} = 2.5 V, I _D = 2.9 A		51	90	
		P	V _{GS} = -2.5 V, I _D = -2.4 A		104	145	
		N	V _{GS} = 1.8 V, I _D = 2.2 A		67	150	
		P	V _{GS} = -1.8 V, I _D = -1.9 A		143	220	
Forward Transconductance	g _{FS}	N	V _{DS} = 10 V, I _D = 3.5 A		4.7		S
		P	V _{DS} = -10 V, I _D = -2.7 A		5.1		

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	N	f = 1 MHz, V _{GS} = 0 V	V _{DS} = 10 V		387	pF
Output Capacitance	C _{OSS}					73	
Reverse Transfer Capacitance	C _{RSS}					43	
Input Capacitance	C _{ISS}	P		V _{DS} = -10 V		509	
Output Capacitance	C _{OSS}					76	
Reverse Transfer Capacitance	C _{RSS}					40	
Total Gate Charge	Q _{G(TOT)}	N	V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 2.0 A R _G = 6 Ω		4.6	5.5	nC
Threshold Gate Charge	Q _{G(TH)}				0.3		
Gate-to-Source Gate Charge	Q _{GS}				0.7		
Gate-to-Drain "Miller" Charge	Q _{GD}				1.2		
Total Gate Charge	Q _{G(TOT)}	P	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -1.0 A R _G = 6 Ω		5.2	5.5	
Threshold Gate Charge	Q _{G(TH)}				0.4		
Gate-to-Source Gate Charge	Q _{GS}				1.0		
Gate-to-Drain "Miller" Charge	Q _{GD}				1.2		

NTGD3149C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5\text{ V}, V_{DD} = 10\text{ V}, I_D = 1.0\text{ A}, R_G = 6.0\ \Omega$		6.5		ns
Rise Time	t_r				3.8		
Turn-Off Delay Time	$t_{d(OFF)}$				16.4		
Fall Time	t_f				2.4		
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\ \Omega$		7.0		
Rise Time	t_r				5.3		
Turn-Off Delay Time	$t_{d(OFF)}$				33.3		
Fall Time	t_f				29.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	$I_S = 0.8\text{ A}$		0.7	1.2	V
		P		$I_S = -0.8\text{ A}$		-0.7	-1.2	
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0\text{ V}, dI_S / dt = 100\text{ A}/\mu\text{s}$			7.7		ns
Charge Time	t_a					4.5		
Discharge Time	t_b					3.2		
Reverse Recovery Charge	Q_{RR}					1.9		
Reverse Recovery Time	t_{RR}	P	$V_{GS} = 0\text{ V}, dI_S / dt = 100\text{ A}/\mu\text{s}$			11.4		ns
Charge Time	t_a					7.5		
Discharge Time	t_b					3.9		
Reverse Recovery Charge	Q_{RR}					4.7		

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTGD3149CT1G	TSOP6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS (N-CHANNEL)

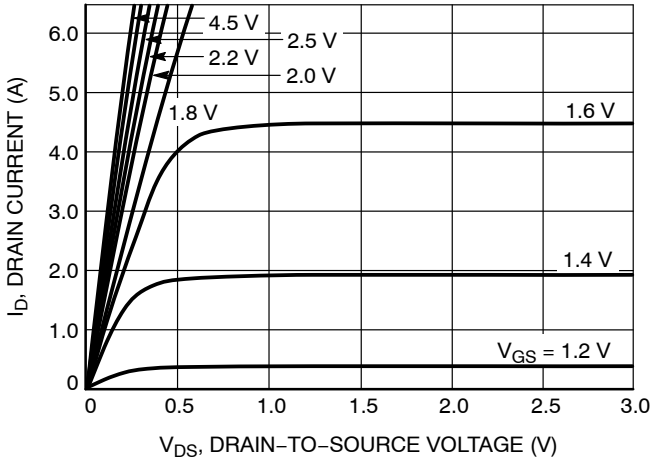


Figure 1. Nch On-Region Characteristics

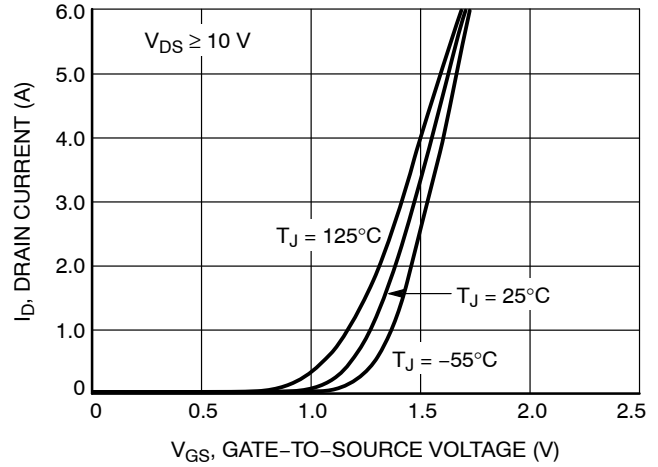


Figure 2. Nch Transfer Characteristics

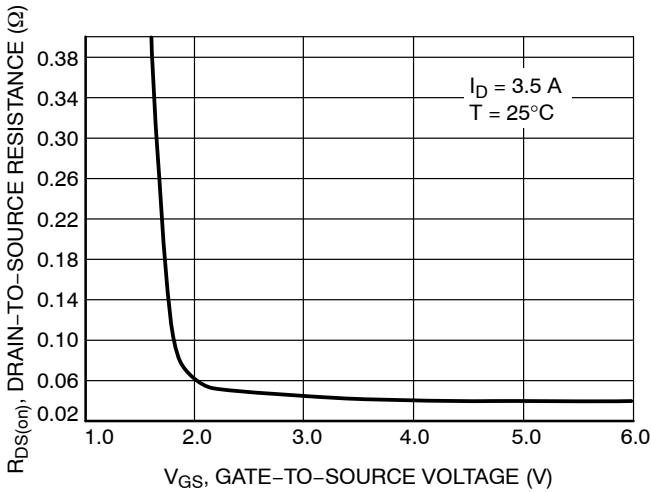


Figure 3. Nch On-Resistance vs. Gate Voltage

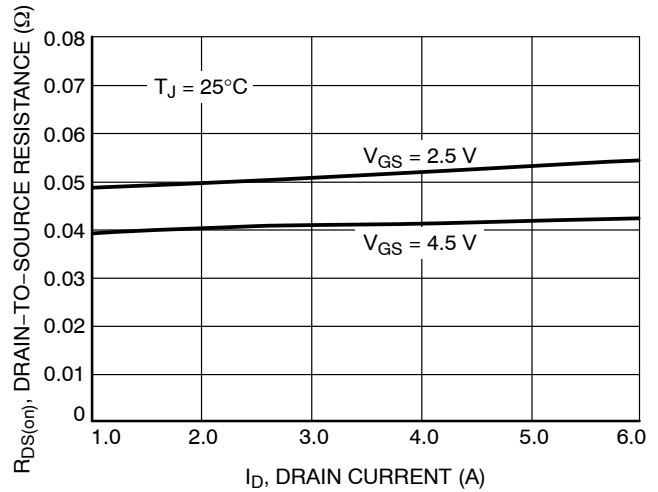


Figure 4. Nch On-Resistance vs. Drain Current and Gate Voltage

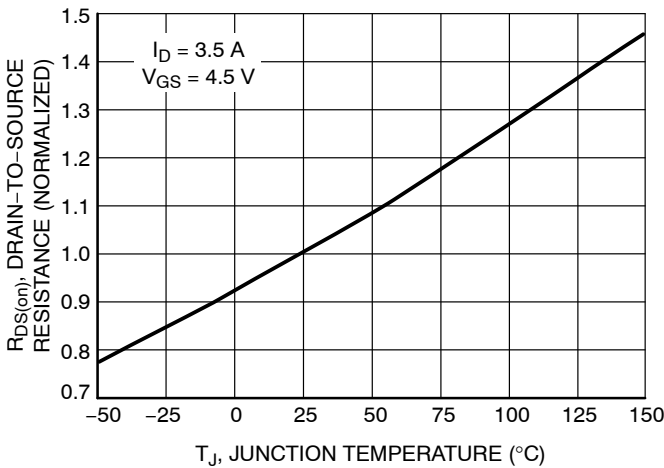


Figure 5. Nch On-Resistance Variation with Temperature

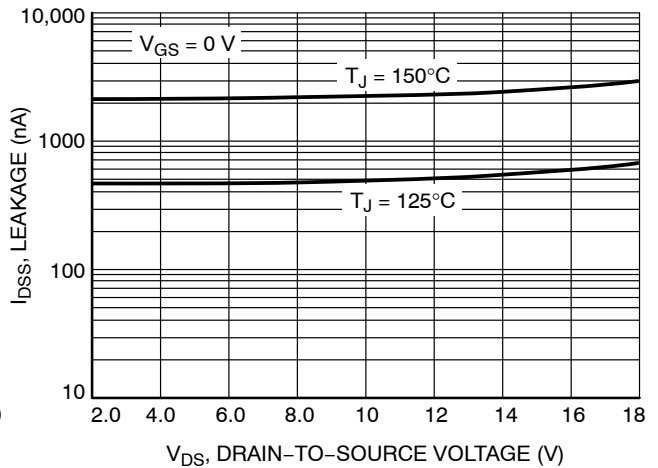


Figure 6. Nch Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (N-CHANNEL)

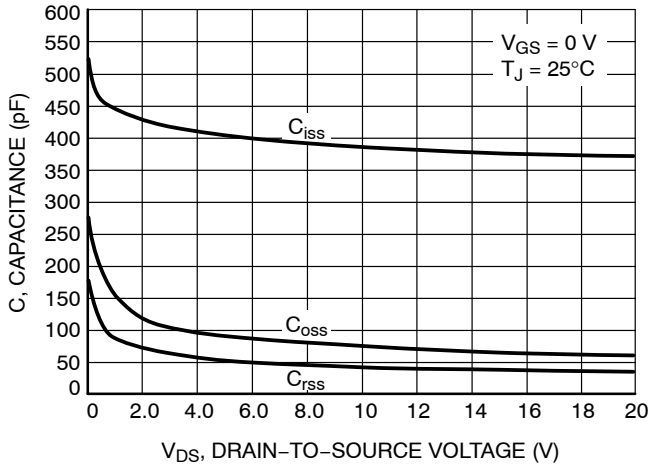


Figure 7. Nch Capacitance Variation

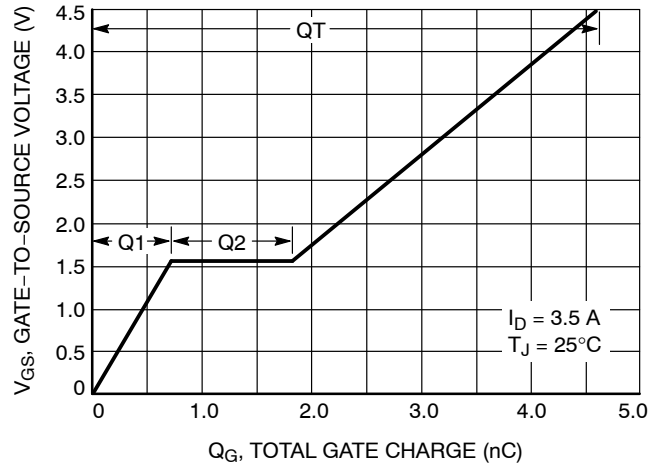


Figure 8. Nch Gate-to-Source Voltage vs. Total Charge

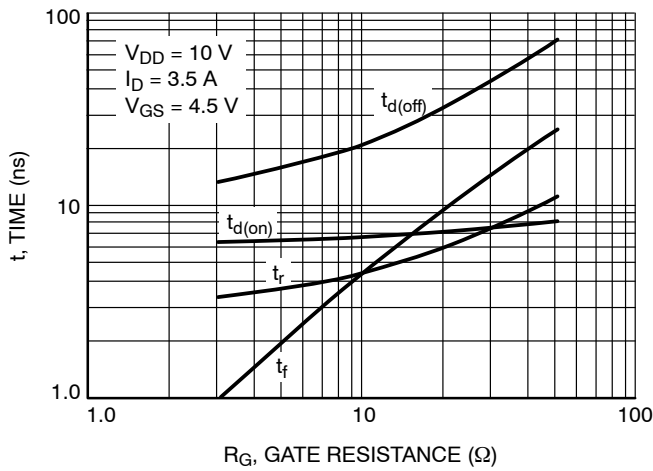


Figure 9. Nch Resistive Switching Time Variation vs. Gate Resistance

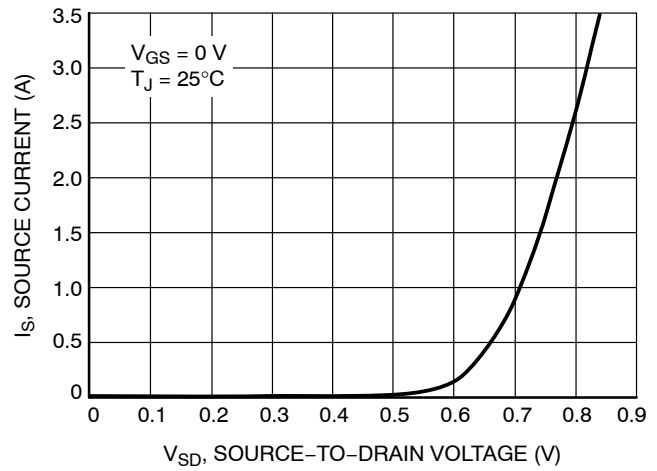


Figure 10. Nch Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (P-CHANNEL)

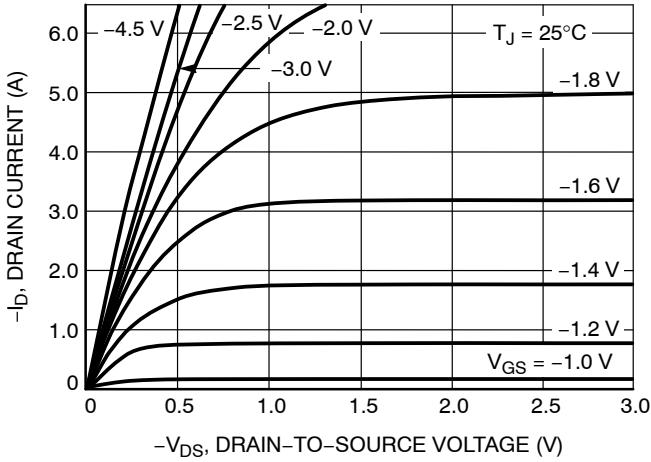


Figure 11. Pch On-Region Characteristics

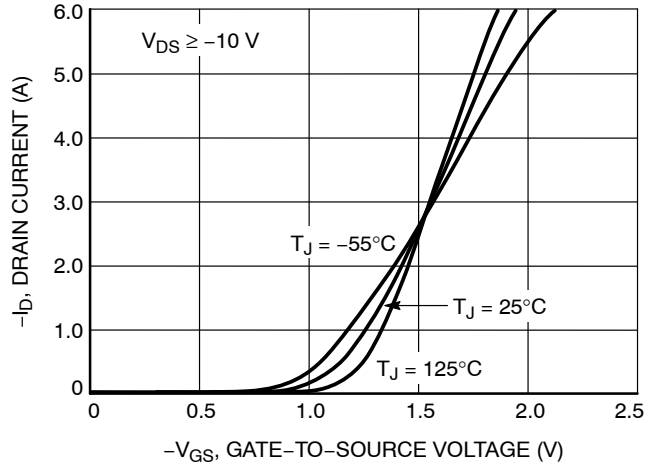


Figure 12. Pch Transfer Characteristics

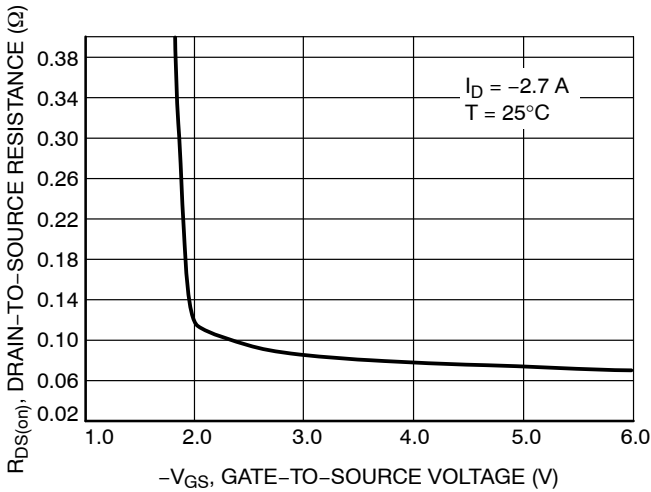


Figure 13. Pch On-Resistance vs. Gate Voltage

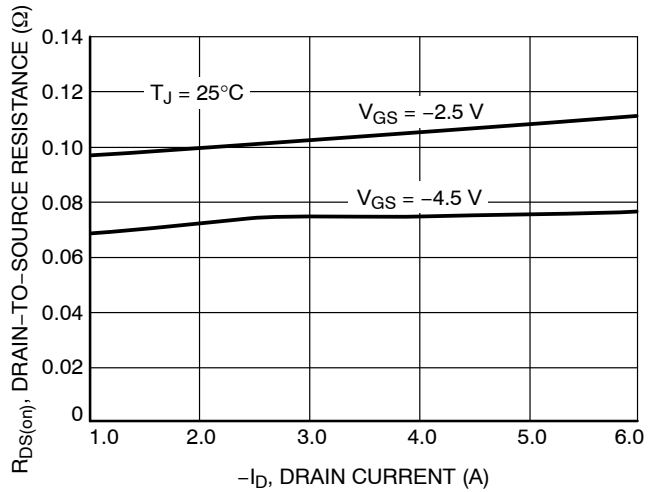


Figure 14. Pch On-Resistance vs. Drain Current and Gate Voltage

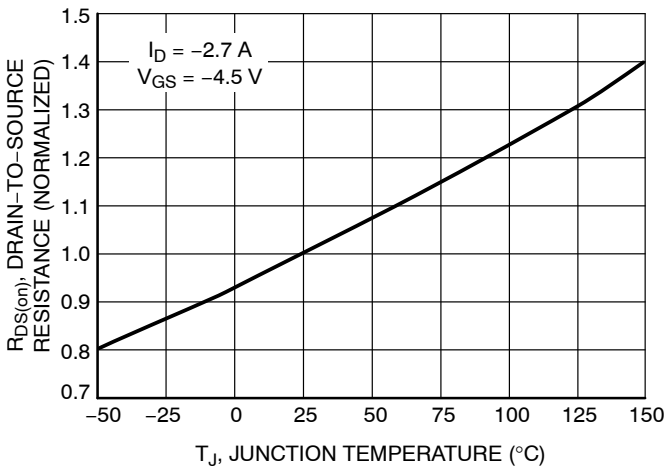


Figure 15. Pch On-Resistance Variation with Temperature

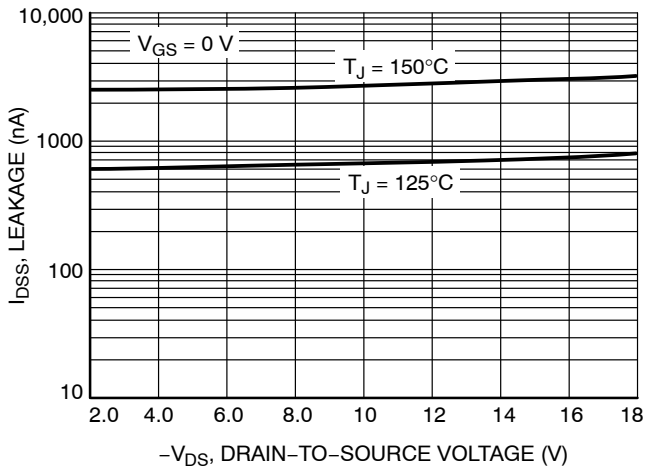


Figure 16. Pch Drain-to-Source Leakage Current vs. Voltage

NTGD3149C

TYPICAL CHARACTERISTICS (P-CHANNEL)

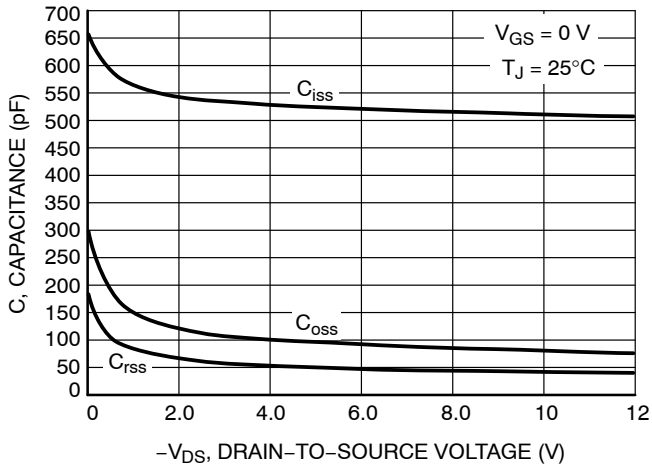


Figure 17. Pch Capacitance Variation

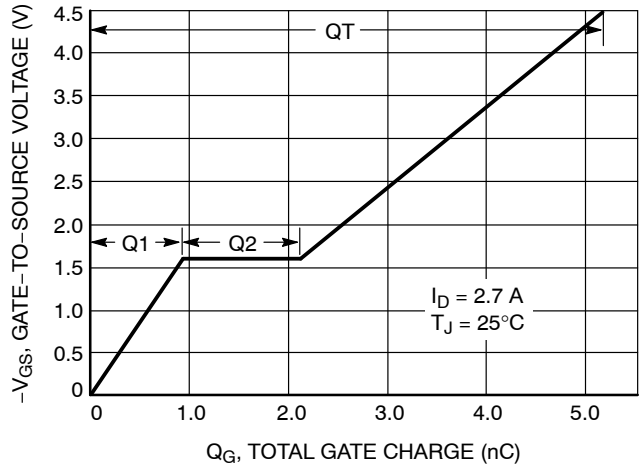


Figure 18. Pch Gate-to-Source Voltage vs. Total Charge

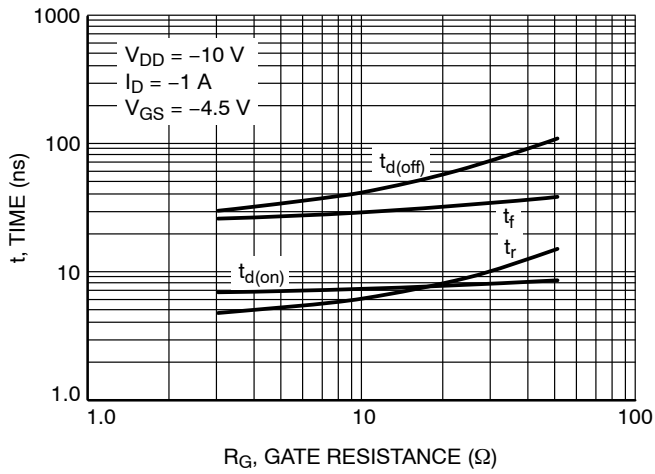


Figure 19. Pch Resistive Switching Time Variation vs. Gate Resistance

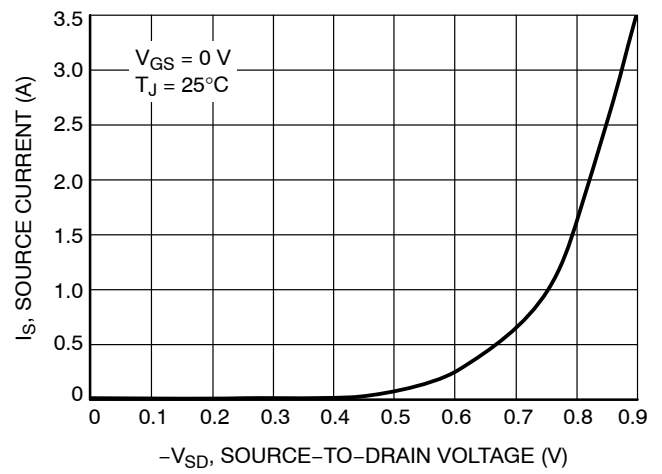


Figure 20. Pch Diode Forward Voltage vs. Current

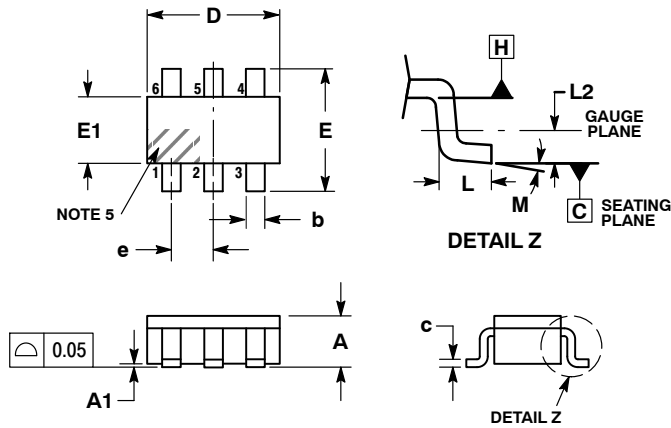
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



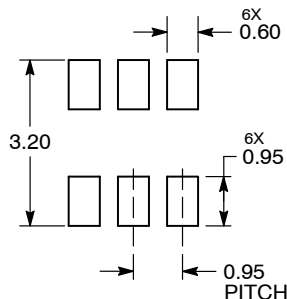
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- | | | | | | |
|----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| <p>STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN</p> | <p>STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2</p> | <p>STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out</p> | <p>STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD</p> | <p>STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR</p> |
| <p>STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER</p> | <p>STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND</p> | <p>STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+</p> | <p>STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2</p> | <p>STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O</p> |
| <p>STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1</p> | <p>STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN</p> | <p>STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE</p> | <p>STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



IC

STANDARD

- | | |
|----------------------------|----------------------------|
| XXX = Specific Device Code | XXX = Specific Device Code |
| A = Assembly Location | M = Date Code |
| Y = Year | ▪ = Pb-Free Package |
| W = Work Week | |
| ▪ = Pb-Free Package | |

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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