

# NTF6P02, NVF6P02

## MOSFET – Power, P-Channel, SOT-223

**-10 A, -20 V**

### Features

- Low  $R_{DS(on)}$
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- NVF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable\*
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Power Management in Portables and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	-20	Vdc
Gate-to-Source Voltage	$V_{GS}$	$\pm 8.0$	Vdc
Drain Current (Note 1)			
– Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	-10	A
– Continuous @ $T_A = 70^\circ\text{C}$	$I_D$	-8.4	A
– Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_{DM}$	-35	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	8.3	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -20 \text{ Vdc}$ , $V_{GS} = -5.0 \text{ Vdc}$ , $I_{L(pk)} = -10 \text{ A}$ , $L = 3.0 \text{ mH}$ , $R_G = 25\Omega$ )	$E_{AS}$	150	mJ
Thermal Resistance			$^\circ\text{C/W}$
– Junction to Lead (Note 1)	$R_{\theta JL}$	15	
– Junction to Ambient (Note 2)	$R_{\theta JA}$	71.4	
– Junction to Ambient (Note 3)	$R_{\theta JA}$	160	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Steady State.
2. When surface mounted to an FR4 board using 1" pad size, (Cu. Area 1.127 sq in), Steady State.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu. Area 0.412 sq in), Steady State.

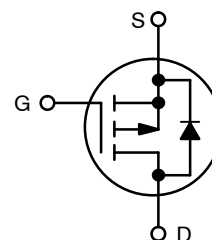


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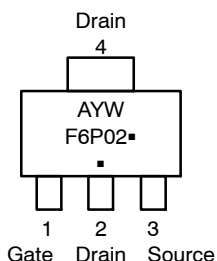
**-10 AMPERES  
-20 VOLTS**

**$R_{DS(on)} = 44 \text{ m}\Omega$  (Typ.)**



P-Channel MOSFET

### MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location  
Y = Year  
W = Work Week  
F6P02 = Specific Device Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTF6P02T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF6P02T3G*	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTF6P02, NVF6P02

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	-20 -	-25 -11	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	- -	- -	-1.0 -10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 8.0 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	± 100	nAdc

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage (Note 4) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	-0.4 -	-0.7 2.6	-1.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 4) (V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -6.0 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -4.0 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -3.0 Adc)	R <sub>DS(on)</sub>	- - -	44 57 57	50 70 -	mΩ
Forward Transconductance (Note 4) (V <sub>DS</sub> = -10 Vdc, I <sub>D</sub> = -6.0 Adc)	g <sub>fs</sub>	-	12	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	C <sub>iss</sub>	-	900	1200	pF
Output Capacitance		C <sub>oss</sub>	-	350	500	
Transfer Capacitance		C <sub>rss</sub>	-	90	150	
Input Capacitance	(V <sub>DS</sub> = -10 Vdc, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	C <sub>iss</sub>	-	940	-	pF
Output Capacitance		C <sub>oss</sub>	-	410	-	
Transfer Capacitance		C <sub>rss</sub>	-	110	-	

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V <sub>DD</sub> = -5.0 Vdc, I <sub>D</sub> = -1.0 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	7.0	12	ns
Rise Time		t <sub>r</sub>	-	25	45	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	75	125	
Fall Time		t <sub>f</sub>	-	50	85	
Turn-On Delay Time	(V <sub>DD</sub> = -16 Vdc, I <sub>D</sub> = -6.0 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 2.5 Ω)	t <sub>d(on)</sub>	-	8.0	-	ns
Rise Time		t <sub>r</sub>	-	30	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	60	-	
Fall Time		t <sub>f</sub>	-	60	-	
Gate Charge	(V <sub>DS</sub> = -16 Vdc, I <sub>D</sub> = -6.0 Adc, V <sub>GS</sub> = -4.5 Vdc) (Note 4)	Q <sub>T</sub>	-	15	20	nC
		Q <sub>gs</sub>	-	1.7	-	
		Q <sub>gd</sub>	-	6.0	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = -3.0 Adc, V <sub>GS</sub> = 0 Vdc) (Note 4) (I <sub>S</sub> = -2.1 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = -3.0 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- - -	-0.82 -0.74 -0.68	-1.2 - -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = -3.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs) (Note 4)	t <sub>rr</sub>	-	42	-	ns
		t <sub>a</sub>	-	17	-	
		t <sub>b</sub>	-	25	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.036	-	μC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

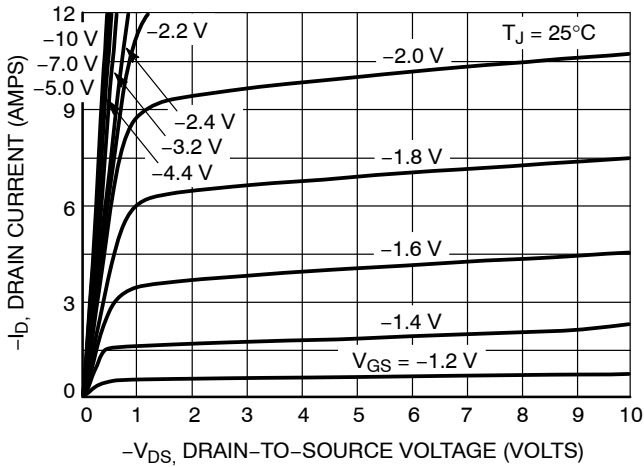


Figure 1. On-Region Characteristics

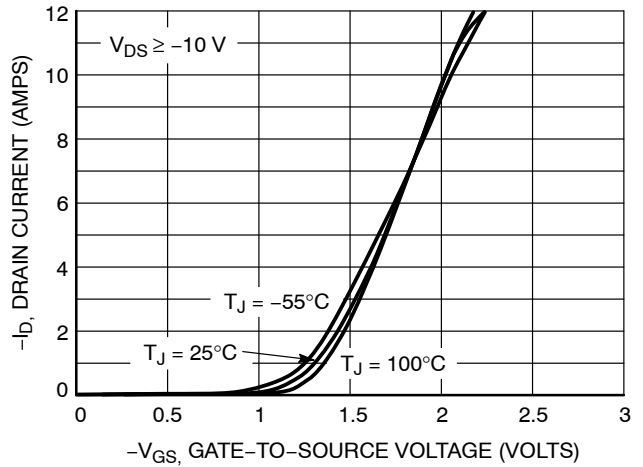


Figure 2. Transfer Characteristics

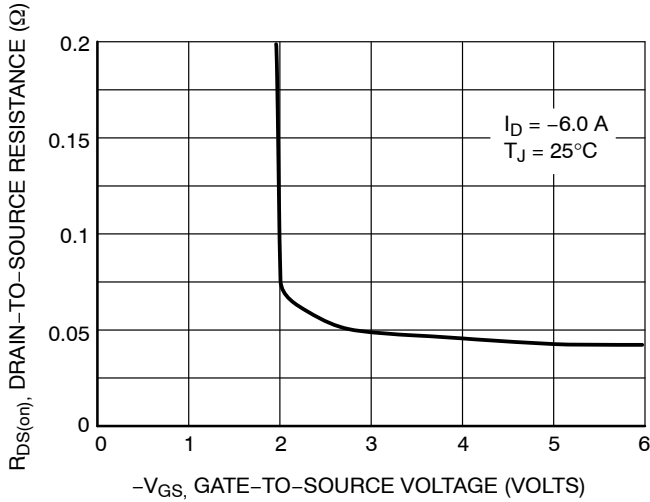


Figure 3. On-Resistance versus Gate-to-Source Voltage

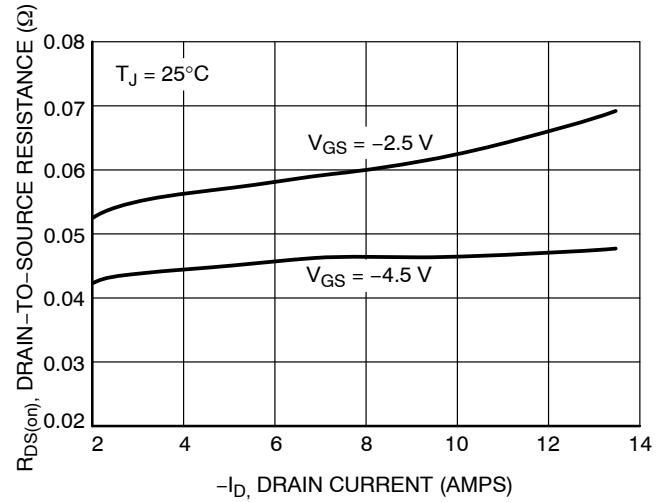


Figure 4. On-Resistance versus Drain Current and Gate Voltage

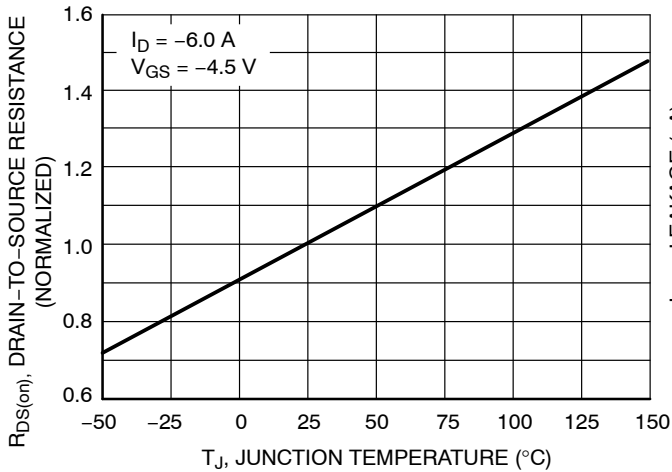


Figure 5. On-Resistance Variation with Temperature

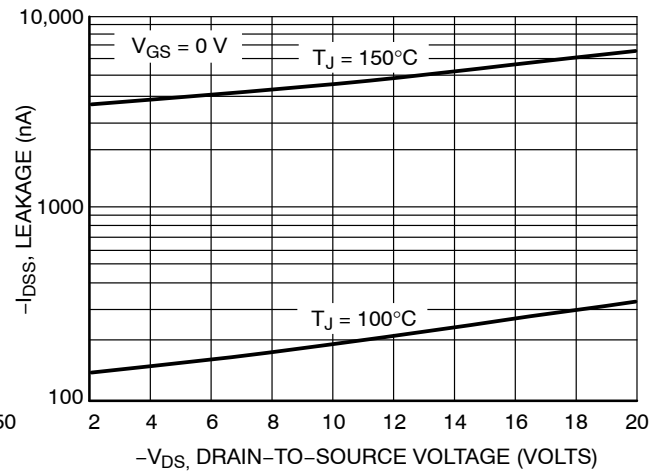


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

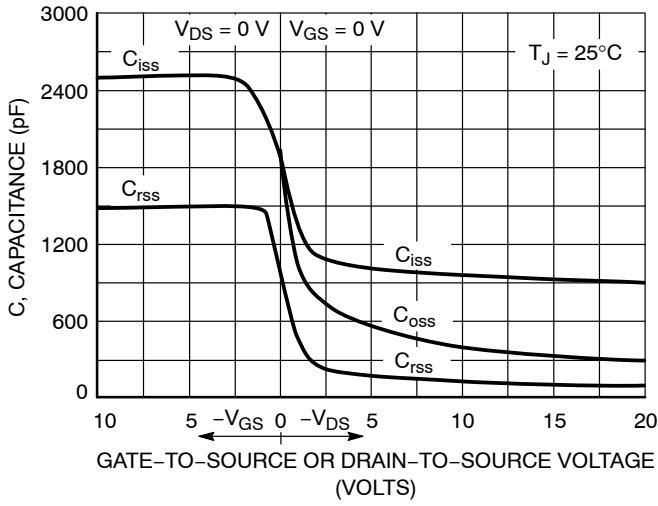


Figure 7. Capacitance Variation

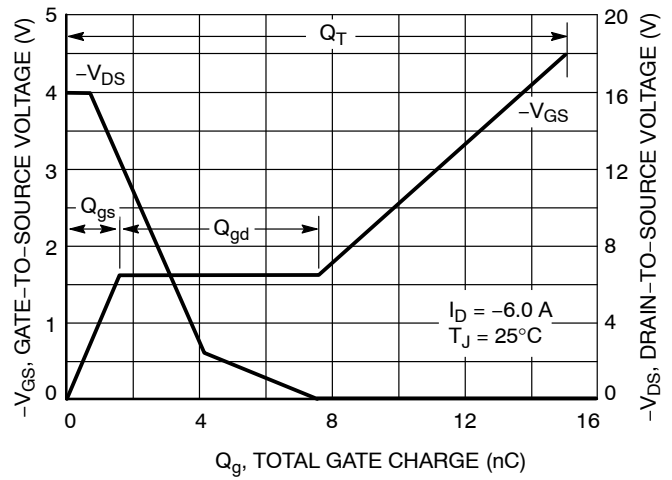


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

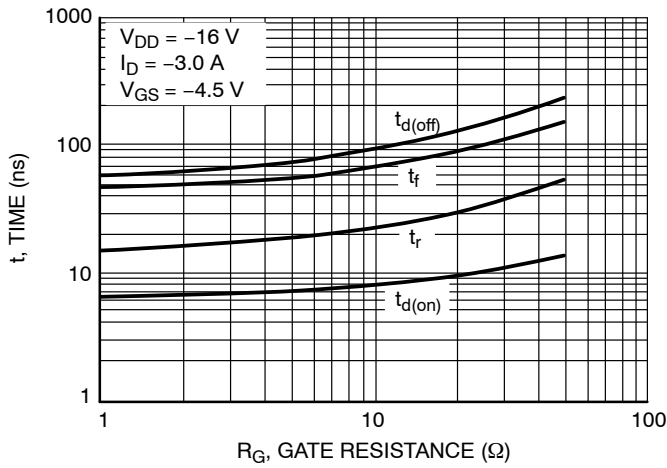


Figure 9. Resistive Switching Time Variation versus Gate Resistance

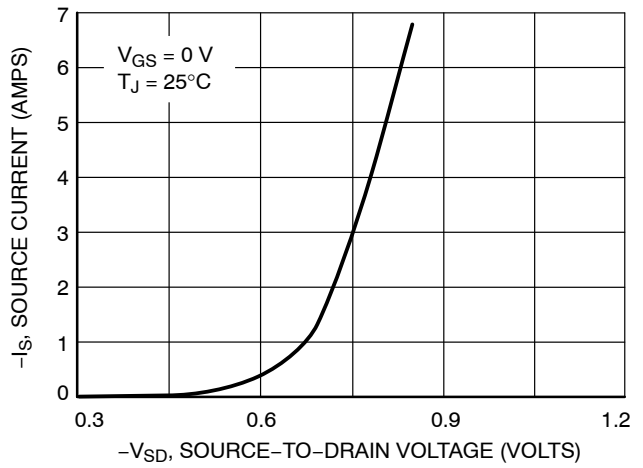


Figure 10. Diode Forward Voltage versus Current

# NTF6P02, NVF6P02

## TYPICAL ELECTRICAL CHARACTERISTICS

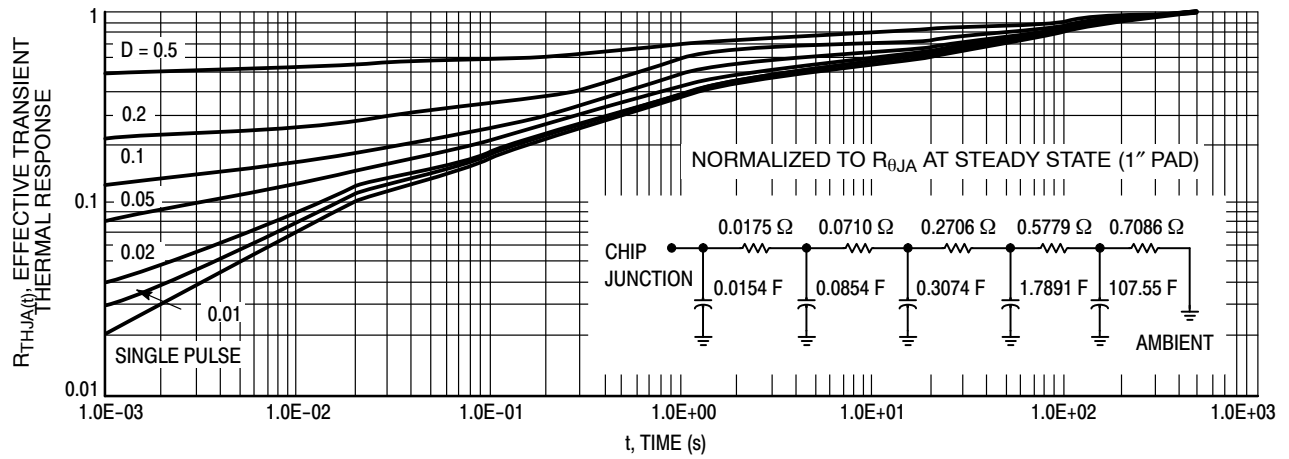


Figure 11. FET Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

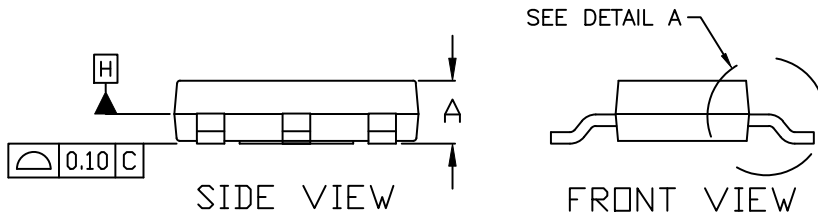
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

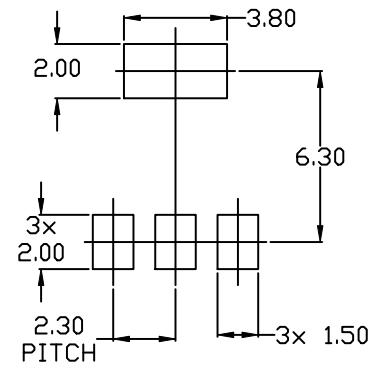
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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