ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74HC32
Integrated Circuit
TTL – High Speed CMOS,
Quad 2–Input OR Gate

Description:

The NTE74HC32 contains four 2–input OR gates in a 14–Lead DIP type package. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS–TTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LS–TTL loads.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- Typical Propagation Delay: 7ns at V_{CC} = 5V, C_L = 15pF, T_A = +25°C
- Fanout (Over Temperature Range):
  - Standard Outputs . . . 10 LS–TTL Loads
  - Bus Driver Outputs . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Drain Current (Per Output), I_{OUT} . . . . . ±25mA
DC Output Source or Sink Current (Per Output), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Maximum Junction, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 80°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
					Typ	Guaranteed Limits		
Minimum HIGH Level Input Voltage	V_{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum LOW Level Input Voltage	V_{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = −20μA	–	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V
			I_{OUT} = −4mA	4.5	–	3.98	3.84	V
			I_{OUT} = −5.2mA	6.0	–	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = 20μA	–	–	0.1	0.1	V
			I_{OUT} = 4mA	4.5	0.2	0.26	0.33	V
			I_{OUT} = 5.2mA	6.0	0.2	0.26	0.33	V
Maximum Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	μA
Maximum Quiescent Device Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	–	2.0	20	μA

Switching Specifications: (t_r = t_f = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Propagation Delay Time (Input to Output)	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	90	115	ns
			4.5	–	18	23	ns
			6.0	–	15	20	ns
Propagation Delay Time (Data Input to Output Y)	t_{PLH}, t_{PHL}	C_L = 15pF	5.0	7	–	–	ns
Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	75	95	ns
			4.5	–	15	19	ns
			6.0	–	13	16	ns
Maximum Input Capacitance	C_{IN}		–	–	10	10	pF
Power Dissipation Capacitance	C_{PD}	Note 3	5.0	22	–	–	pF

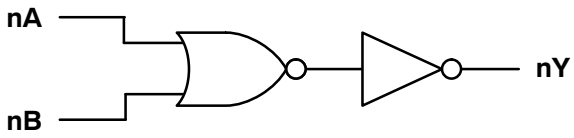
Note 3. C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = C_{PD} V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Truth Table:

Inputs		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Level
L = LOW Level

Logic Diagram



Pin Connection Diagram