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NTE74C74
Integrated Circuit
TTL– CMOS Dual D–Type Positive Edge Triggered Flip–Flop with Preset & Clear
14–Lead DIP

Description:

The NTE74C74 dual D–type flip–flop is a monolithic complementary MOS (CMOS) integrated circuit in a 14–Lead DIP type package constructed with N– and P–channel enhancement transistors. Each flip–flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear.

Features:

- Wide Supply Range: 3V to 15V
- Tenth Power TTL Compatible: Drive 2 LPT^{2}L Loads
- High Noise Immunity: 0.45 V_{CC} (typ)
- Low Power: 50nW (typ)
- Medium Speed Operation: 10Mhz (typ) with 10V Supply

Applications:

- Automotive
- Data Terminals
- Instrumentation
- Medical Electronics
- Alarm Systems
- Industrial Electronics
- Remote Metering
- Computers

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 700mW
Operating V_{CC} Range . . . . . 3V to 15V
Maximum V_{CC} Voltage 18V
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −55° to +125°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V		4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V		–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V		–	–	1.0	μA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V		–1.0	–	–	μA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.05	60	μA
CMOS/LPTTL Interface							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360μA		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 360μA		–	–	0.4	V
Output Drive							
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V	$V_{IN(0)}$ = 0, V_{OUT} = 0, T_A = +25°C	–1.75	–	–	mA
		V_{CC} = 10V		–8	–	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V	$V_{IN(0)}$ = 0, V_{OUT} = V_{CC}, T_A = +25°C	1.75	–	–	mA
		V_{CC} = 10V		8	–	–	mA

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time to a Logical “0” t_{pd0} or Logical “1” t_{pd1} from Clock to Q or $\overline{Q}$	t_{pd}	V_{CC} = 5V	–	180	300	ns
		V_{CC} = 10V	–	70	110	ns
Propagation Delay Time to a Logical “0” from Preset or Clear	t_{pd}	V_{CC} = 5V	–	180	300	ns
		V_{CC} = 10V	–	70	110	ns
Propagation Delay Time to a Logical “1” from Preset or Clear	t_{pd}	V_{CC} = 5V	–	250	400	ns
		V_{CC} = 10V	–	100	150	ns
Time Prior to Clock Pulse that Data Must be Present, t_{SETUP}	t_{S0}, t_{S1}	V_{CC} = 5V	100	50	–	ns
		V_{CC} = 10V	40	20	–	ns
Time after Clock Pulse that Data Must be Held	t_{H0}, t_{H1}	V_{CC} = 5V	–	–20	0	ns
		V_{CC} = 10V	–	–8.0	0	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	t_{PW1}	V_{CC} = 5V	–	100	250	ns
		V_{CC} = 10V	–	40	100	ns
Minimum Preset and Clear Pulse Width	t_{PW2}	V_{CC} = 5V	–	100	160	ns
		V_{CC} = 10V	–	40	70	ns
Maximum Clock Rise and Fall Time	t_r, t_f	V_{CC} = 5V	15	–	–	μs
		V_{CC} = 10V	5	–	–	μs

Note 2. AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{MAX}	V_{CC} = 5V	2.0	3.5	–	MHz
		V_{CC} = 10V	5.0	8.0	–	MHz
Input Capacitance	C_{IN}	Any Input, Note 3	–	5.0	–	pF
Power Dissipation Capacitance	C_{PD}	Note 4	–	40	–	pF

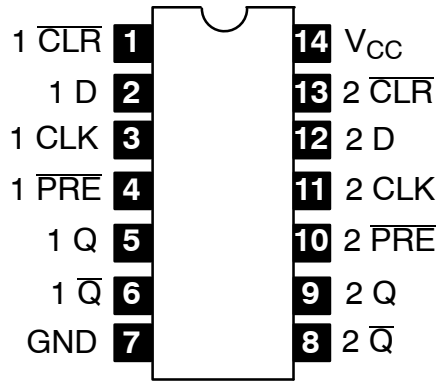
Note 2. AC Parameters are guaranteed by DC correlated testing.
Note 3. Capacitance is guaranteed by periodic testing.
Note 4. C_{PD} determines the no load AC power consumption of any CMOS device.

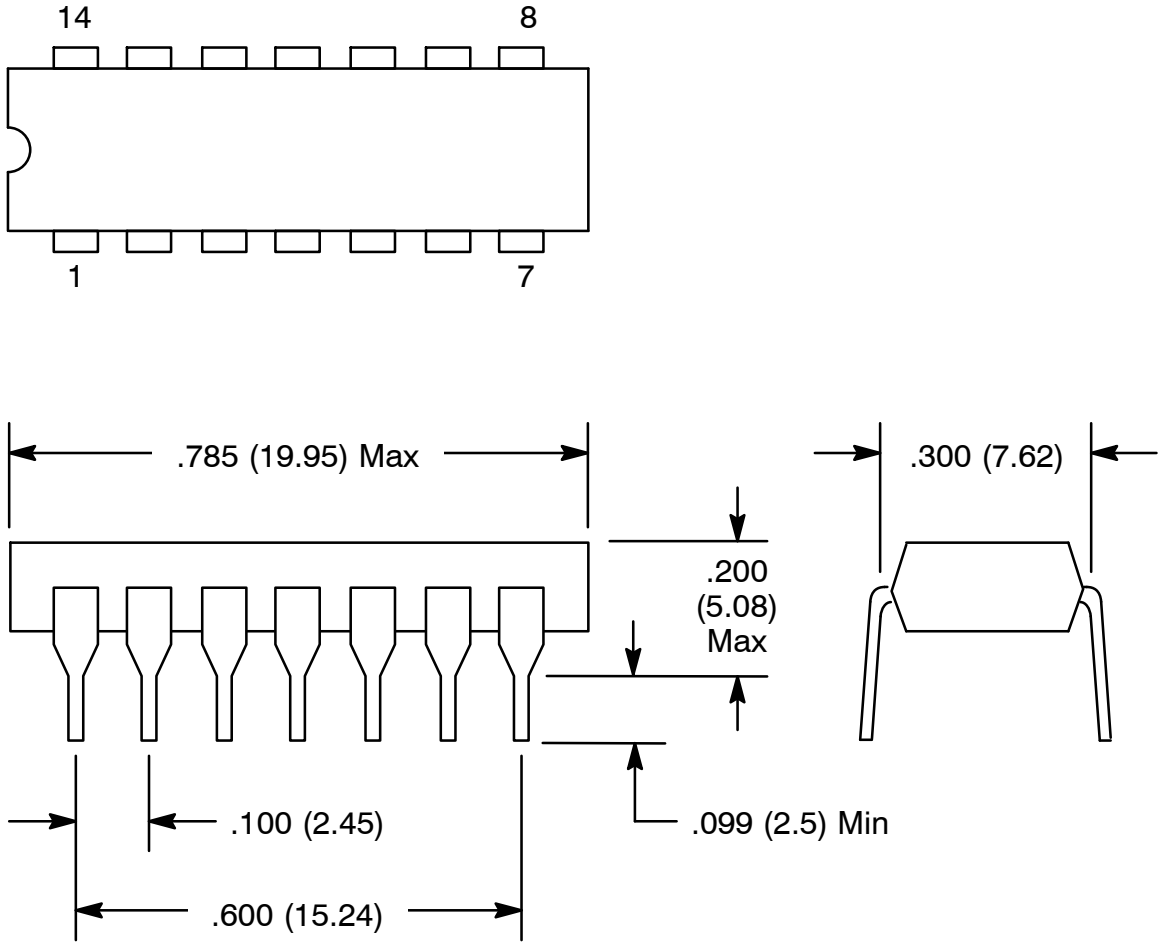
Truth Table:

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	NC	NC

NC = No change in output from previous status

Pin Connection Diagram




14
8
1
7
.785 (19.95) Max
.300 (7.62)
.200
(5.08)
Max
.100 (2.45)
.099 (2.5) Min
.600 (15.24)