ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4597B & NTE4598B
Integrated Circuit
CMOS, 8–Bit Bus–Compatible Latches

Description:

The NTE4597B (16–Lead DIP) and NTE4598B (18–Lead DIP) are 8–bit latches, one addressed with an internal counter (NTE4597B) and the other addressed with an external binary address (NTE4598B). The 8 latch–outputs are high drive, three–state and bus line compatible. The drive capability allows direct applications with MPU systems such as the NTE6800 family.

With the NTE4597B, a 3–bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the NTE4598B are accessed via the Address pins, A0, A1, and A2. A $\overline{\text{Full}}$ Flag is provided on the NTE4597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the data pin when the Strobe is high. Master reset is available on both devices.

Features:

- Serial Data Input
- Three–State Bus Compatible Parallel Outputs
- Three–State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire–O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0Vdc to 18Vdc
- Capable of Driving TTL Over the Rated Temperature Range With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage, Enable (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
Input Voltage, All Other Inputs (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} + 12V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} + 0.5V
Input or Output Current (DC or Transient), Per Pin, I_{in}, I_{out} . . . . . ±10mA
Power Dissipation, P_D 500mW
Derate Above +65°C . . . . . 7mW/°C
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

Electrical Characteristics: (Voltages Referenced to V_{SS}, Note 2)

Parameter	Sym-bol	V_{DD} Vdc	–55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 2) "0" Level	V_{IL}									
$\overline{\text{Enable}}$										
(V_O = 4.5 or 0.5Vdc)		5.0	–	0.8	–	1.1	0.8	–	0.8	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	1.6	–	2.2	1.6	–	1.6	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	2.4	–	3.4	2.4	–	2.4	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	2.0	–	2.0	1.9	–	2.0	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	6.0	–	6.0	3.1	–	6.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	10	–	10	4.3	–	10	–	Vdc
Input Voltage "0" Level	V_{IL}									
Other Inputs										
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11	–	11	8.25	–	11	–	Vdc
Output Drive Current Source	I_{OH}									
$\overline{\text{Full}}$ – Sink Only										
(V_{OH} = 4.6Vdc)		5.0	–1.0	–	–1.0	–2.0	–	–1.0	–	mAdc
(V_{OH} = 9.5Vdc)		10	–	–	–	–6.0	–	–	–	mAdc
(V_{OH} = 13.5Vdc)		15	–	–	–	–12	–	–	–	mAdc
(V_{OL} = 0.4Vdc) Sink	I_{OL}	5.0	1.6	–	1.6	3.2	–	1.6	–	mAdc
(V_{OL} = 0.5Vdc)		10	–	–	–	6.0	–	–	–	mAdc
(V_{OL} = 1.5Vdc)		15	–	–	–	12	–	–	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Three–State Leakage Current	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	μAdc
		15	–	20	–	0.015	20	–	600	μAdc
Total Supply Current	I_T	5.0	I_T = (2.0μA/kHz) f + I_{DD}							μAdc
(External Load Capacitance of 130pF, Note 3)		10	I_T = (4.0μA/kHz) f + I_{DD}							μAdc
		15	I_T = (6.0μA/kHz) f + I_{DD}							μAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics: (C_L = 130pF + 1 TTL Load, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					
t_{TLH}, t_{THL} = (0.5ns/pF) C_L + 35ns		5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.2ns/pF) C_L + 25ns		10	–	50	100	ns
T_{TLH}, t_{THL} = (0.16ns/pF) C_L + 20ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
$\overline{\text{Enable}}$ to Output		5.0	–	160	320	ns
		10	–	125	250	ns
		15	–	100	200	ns
Strobe to Output		5.0	–	200	400	ns
		10	–	100	200	ns
		15	–	80	160	ns
Strobe to $\overline{\text{Full}}$ (NTE4597B Only)		5.0	–	200	400	ns
		10	–	100	200	ns
		15	–	80	160	ns
$\overline{\text{Reset}}$ to Output		5.0	–	175	350	ns
		10	–	90	180	ns
		15	–	70	140	ns
Pulse Width	t_{WH}, t_{WL}					
$\overline{\text{Enable}}$		5.0	320	160	–	ns
		10	240	120	–	ns
		15	160	80	–	ns
Strobe		5.0	200	100	–	ns
		10	100	50	–	ns
		15	80	40	–	ns
Increment (NTE4597B Only)		5.0	200	100	–	ns
		10	100	50	–	ns
		15	80	40	–	ns
$\overline{\text{Reset}}$		5.0	300	150	–	ns
		10	160	80	–	ns
		15	100	50	–	ns
Setup Time	t_{su}					
Data		5.0	100	50	–	ns
		10	50	25	–	ns
		15	35	20	–	ns
Address (NTE4598B Only)		5.0	200	100	–	ns
		10	100	50	–	ns
		15	70	35	–	ns
Increment (NTE4597B Only)		5.0	400	200	–	ns
		10	200	100	–	ns
		15	170	85	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics (Cont'd): (C_L = 130pF + 1 TTL Load, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Hold Time	t_h					
Data		5.0	100	50	–	ns
		10	50	25	–	ns
		15	35	20	–	ns
Address (NTE4598B Only)		5.0	100	50	–	ns
		10	50	25	–	ns
		15	35	20	–	ns
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	20	–25	–	ns
		10	20	–15	–	ns
		15	20	–10	–	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Latch Truth Table

Strobe	$\overline{\text{Reset}}$	Address Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

* = No change in state of latch

X = Don't Care

Latch Truth Table

$\overline{\text{Enable}}$	Outputs
1	High Impedance
0	D_n

D_n = State of nth latch

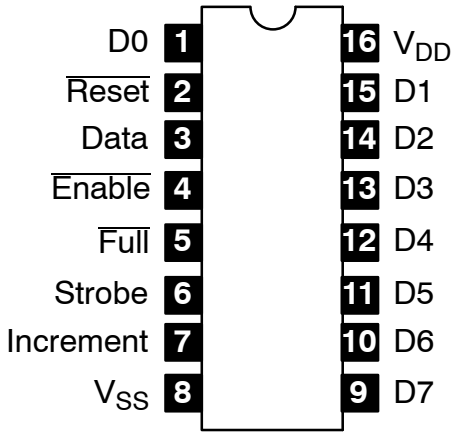
Truth Table for NTE4597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
↓	X	1	Count Up	–
↑	X	1	No Change	–
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't Care

Pin Connection Diagram

NTE4597B



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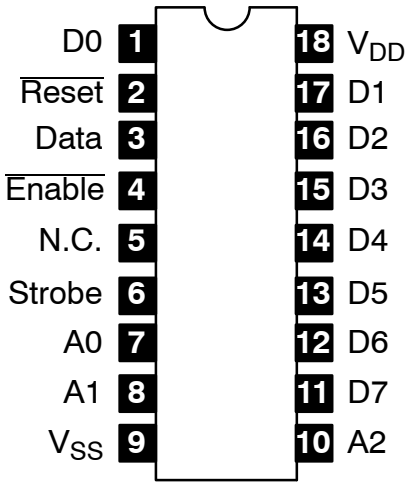

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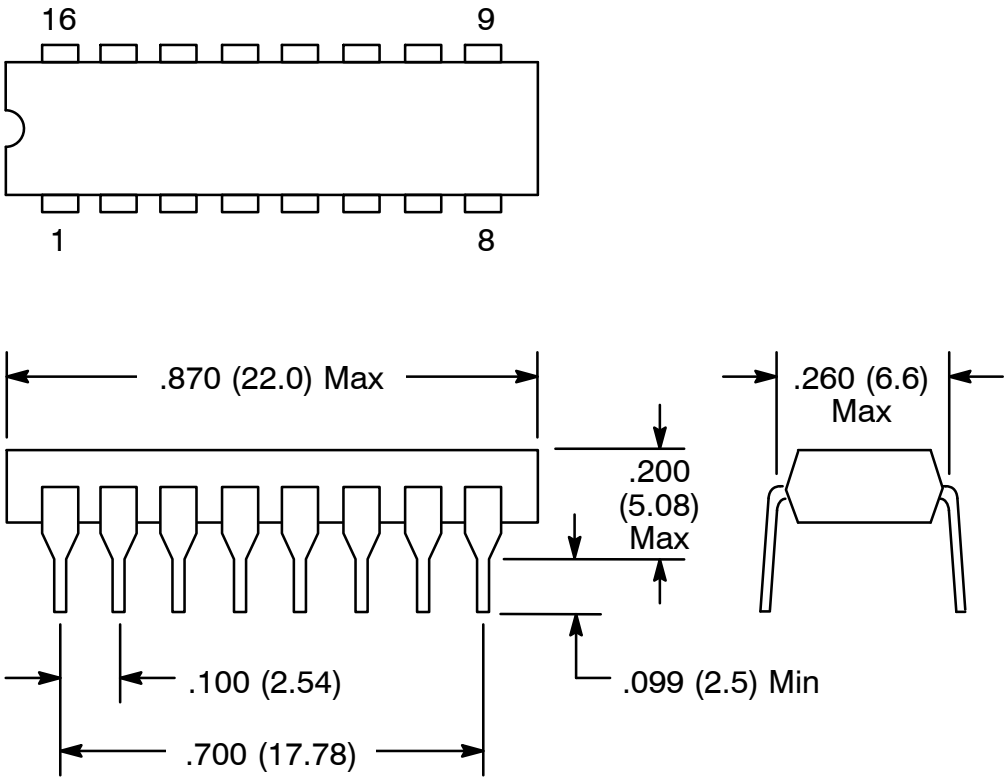

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