ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4042B & NTE4042BT
Integrated Circuit
CMOS, Quad Transparent Latch

Description:

The NTE4042B (16–Lead DIP) and NTE4042BT (SOIC–16) are quad transparent latch devices constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

Features:

- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	µAdc
		15	–	4.0	–	0.006	4.0	–	120	µAdc
Total Supply Current	I_T	5.0	I_T = (1.0µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs all buffers switching, Note 3, Note 4)		10	I_T = (2.0µA/kHz) f + I_{DD}							µAdc
		15	I_T = (3.0µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns	t_{TLH}, t_{THL}	5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, D to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 135ns	t_{PLH}. t_{PHL}	5.0	–	220	440	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 57ns		10	–	90	180	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 35ns		15	–	60	120	ns
Propagation Delay Time, Clock to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 135ns	t_{PLH}. t_{PHL}	5.0	–	220	440	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 57ns		10	–	90	180	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 35ns		15	–	60	120	ns
Clock Pulse Width	t_{WH}	5.0	300	150	–	ns
		10	100	50	–	ns
		15	80	40	–	ns
Clock Pulse Rise and Fall Time	t_{PLH}. t_{PHL}	5.0	–	–	15	ns
		10	–	–	5.0	ns
		15	–	–	4.0	ns
Hold Time	t_h	5.0	100	50	–	ns
		10	50	25	–	ns
		15	40	20	–	ns
Setup Time	t_{su}	5.0	50	0	–	ns
		10	30	0	–	ns
		15	25	0	–	ns

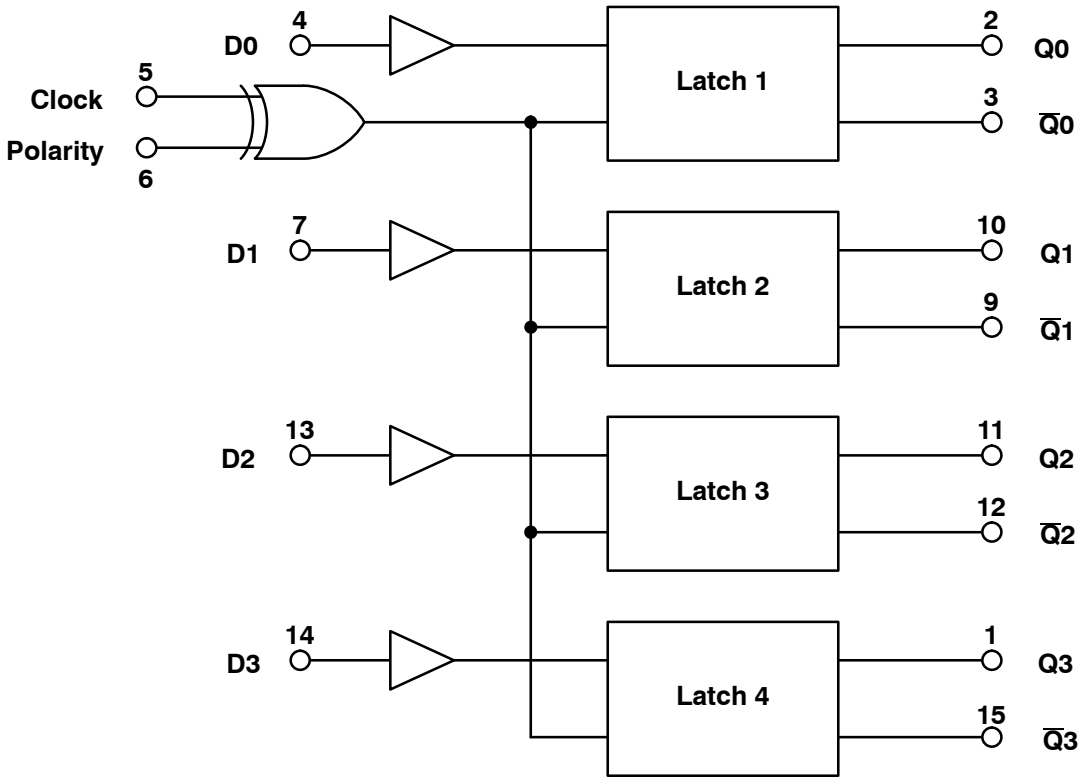
Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table:

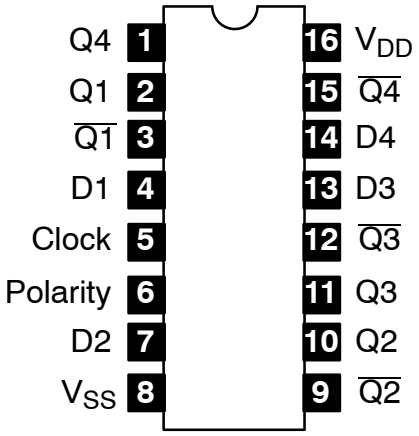
Clock	Polarity	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

Logic Diagram

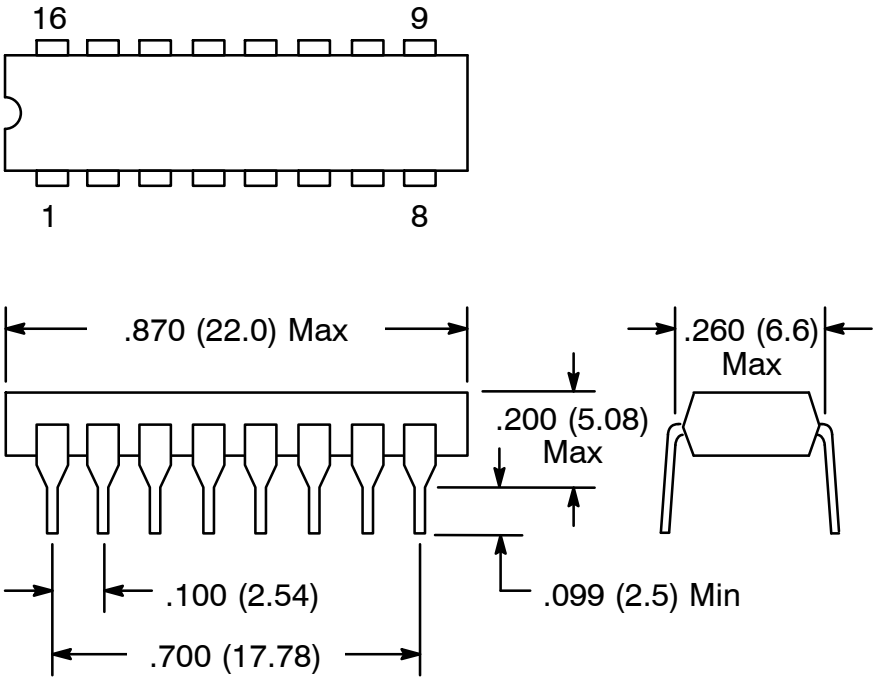


V_{DD} = Pin16
V_{SS} = Pin8

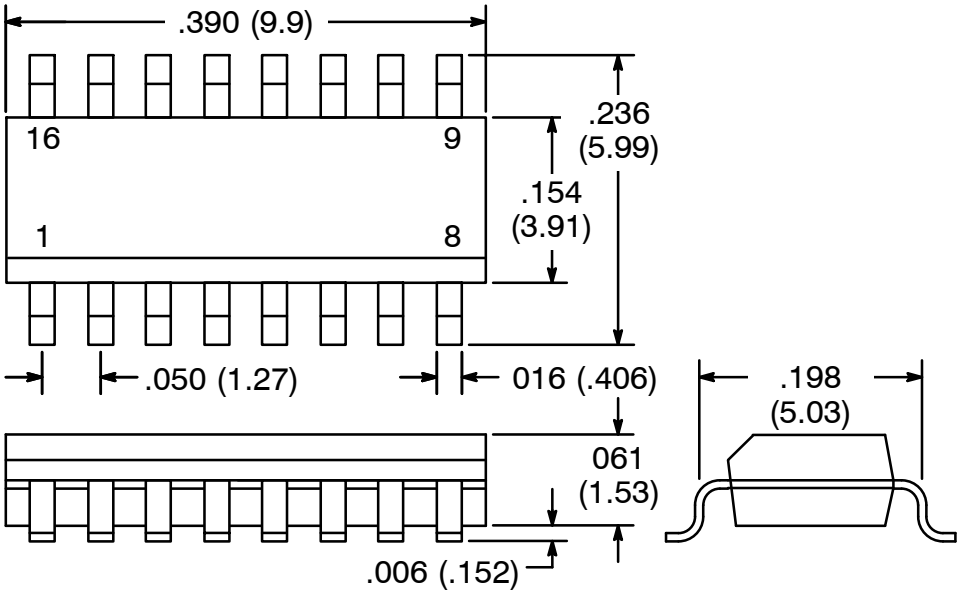
Pin Connection Diagram



NTE4042B



NTE4042BT



NOTE: Pin1 on Beveled Edge