

# NTD30N02

## Power MOSFET 30 Amps, 24 Volts

### N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Features

- Pb-Free Packages are Available

#### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	24	Vdc
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	Vdc
Drain Current			Adc
– Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	30	
– Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_{DM}$	100	Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	75	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 24 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $L = 1.0 \text{ mH}$ , $I_L(pk) = 10 \text{ A}$ , $R_G = 25 \Omega$ )	$E_{AS}$	50	mJ
Thermal Resistance			$^\circ\text{C/W}$
– Junction-to-Case	$R_{\theta JC}$	1.65	
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	67	
– Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in. pad size, (Cu Area 1.127 sq in).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 sq in).

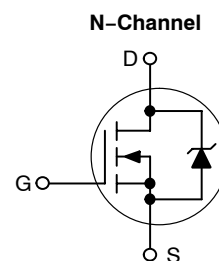


ON Semiconductor®

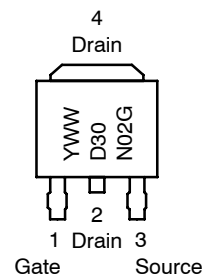
<http://onsemi.com>

**30 AMPERES  
24 VOLTS**

**$R_{DS(on)} = 11.2 \text{ m}\Omega$  (Typ.)**



#### MARKING DIAGRAM



D30N02 = Device Code  
Y = Year  
WW = Work Week  
G = Pb-Free Device

#### ORDERING INFORMATION

Device	Package	Shipping†
NTD30N02	DPAK	75 Units/Rail
NTD30N02G	DPAK (Pb-Free)	75 Units/Rail
NTD30N02T4	DPAK	2500 Tape & Reel
NTD30N02T4G	DPAK (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTD30N02

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	24 -	26.5 25.5	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 24 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	- - -	- - -	0.8 1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	2.1 -4.1	3.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 30 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 20 Adc) (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 15 Adc)	R <sub>DS(on)</sub>	- - -	- 11.2 20	14.5 14.5 24	mΩ
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 15 Adc)	g <sub>FS</sub>	-	20	-	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	1000	-	pF
Output Capacitance		C <sub>oss</sub>	-	425	-	
Transfer Capacitance		C <sub>rss</sub>	-	175	-	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>DD</sub> = 20 Vdc, I <sub>D</sub> = 30 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 2.5 Ω)	t <sub>d(on)</sub>	-	7.0	15	ns
Rise Time		t <sub>r</sub>	-	28	55	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	22	35	
Fall Time		t <sub>f</sub>	-	12	20	
Turn-On Delay Time	(V <sub>DD</sub> = 20 Vdc, I <sub>D</sub> = 15 Adc, V <sub>GS</sub> = 4.5 Vdc, R <sub>G</sub> = 2.5 Ω)	t <sub>d(on)</sub>	-	12.5	-	ns
Rise Time		t <sub>r</sub>	-	115	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	15	-	
Fall Time		t <sub>f</sub>	-	17	-	
Gate Charge	(V <sub>DS</sub> = 20 Vdc, I <sub>D</sub> = 30 Adc, V <sub>GS</sub> = 4.5 Vdc) (Note 3)	Q <sub>T</sub>	-	14.4	20	nC
		Q <sub>1</sub>	-	4.0	-	
		Q <sub>2</sub>	-	8.5	-	

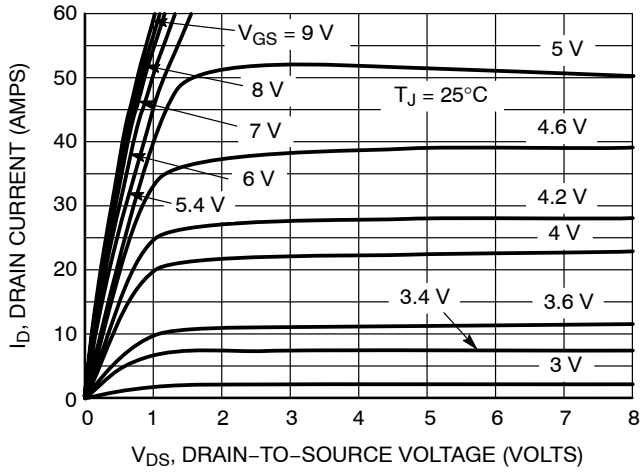
### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 15 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc) (Note 3) (I <sub>S</sub> = 15 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- - -	0.95 1.10 0.80	1.2 - -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	30	-	ns
		t <sub>a</sub>	-	14.5	-	
		t <sub>b</sub>	-	15.5	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.013	-	μC

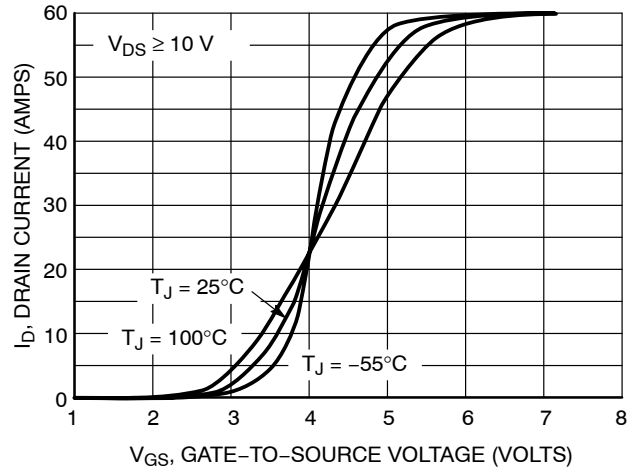
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

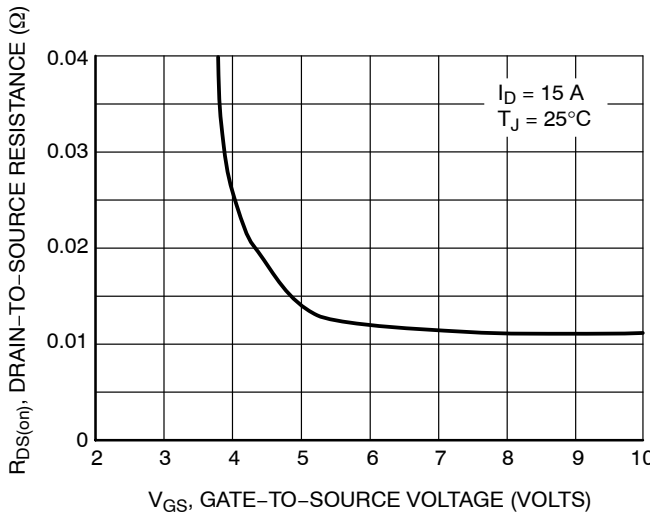
# NTD30N02



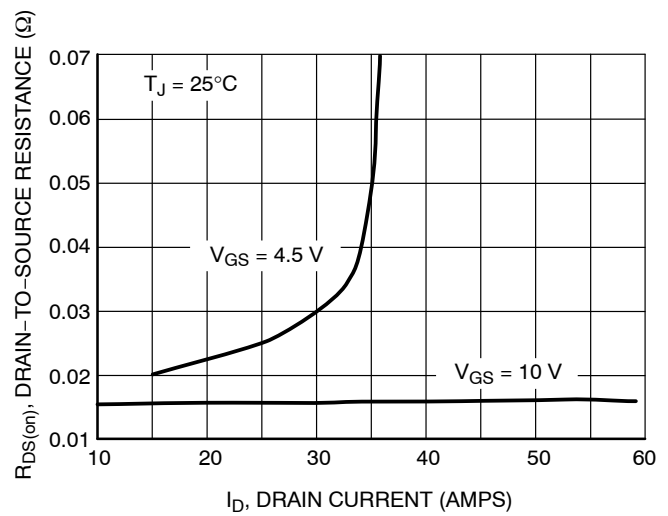
**Figure 1. On-Region Characteristics**



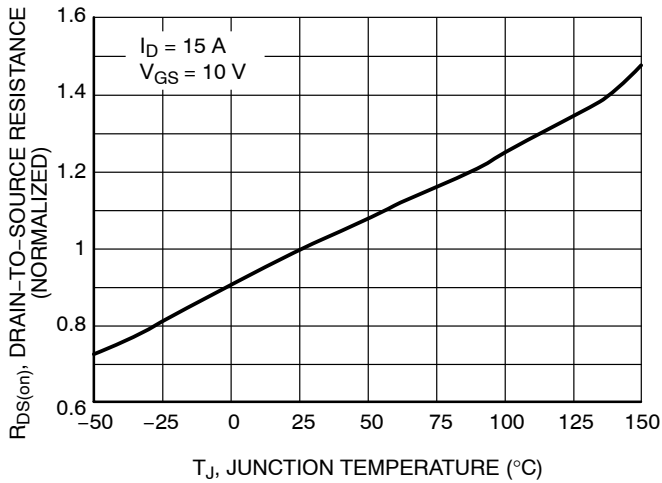
**Figure 2. Transfer Characteristics**



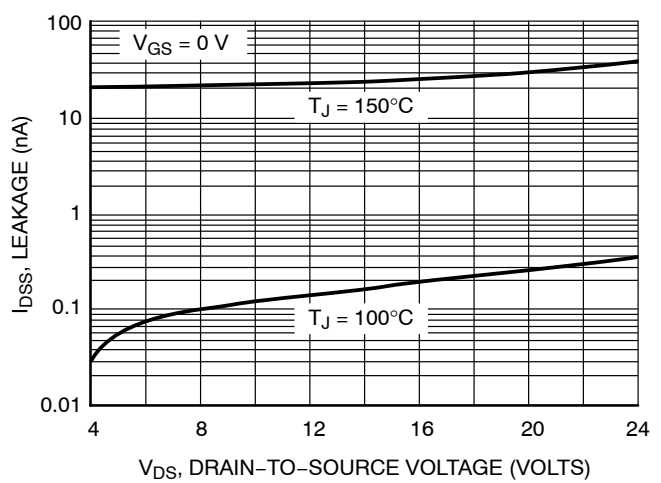
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current versus Voltage**

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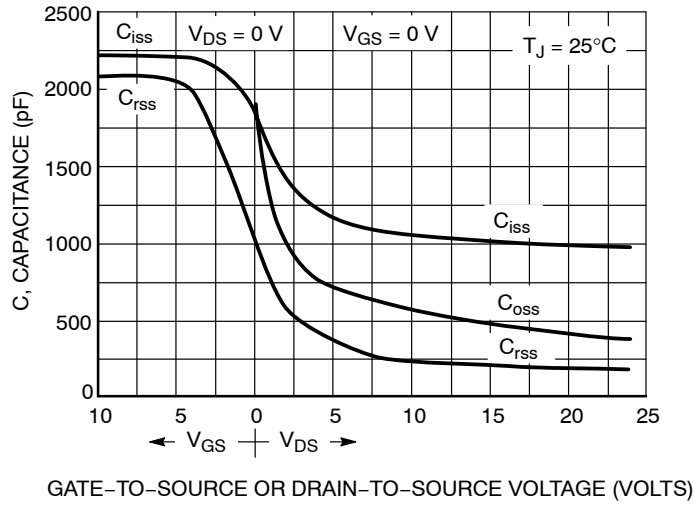


Figure 7. Capacitance Variation

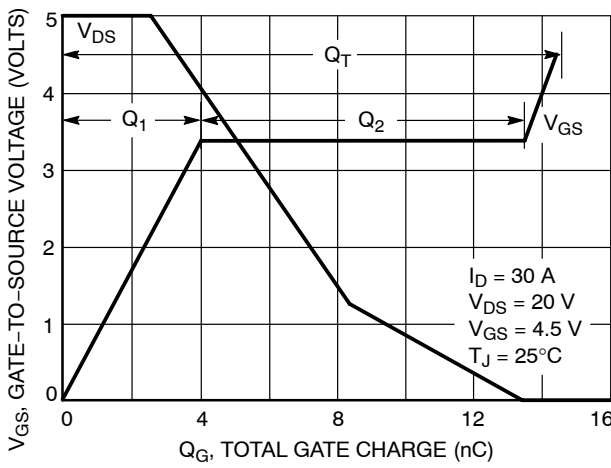


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

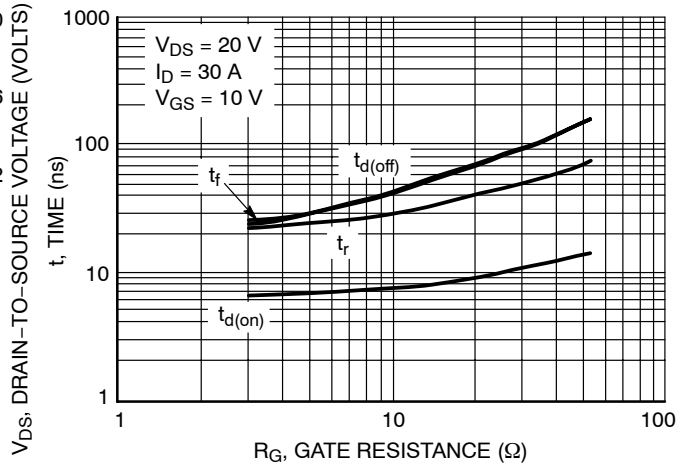


Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

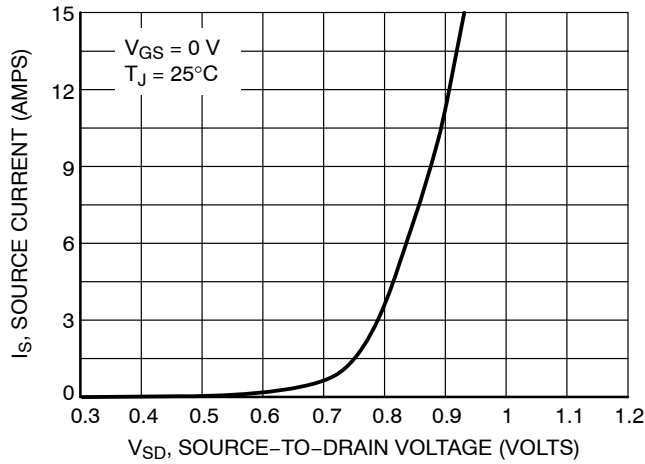


Figure 10. Diode Forward Voltage versus Current

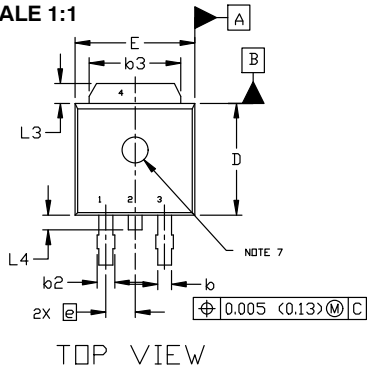
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



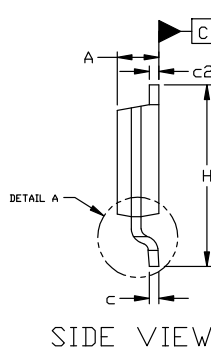
## DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

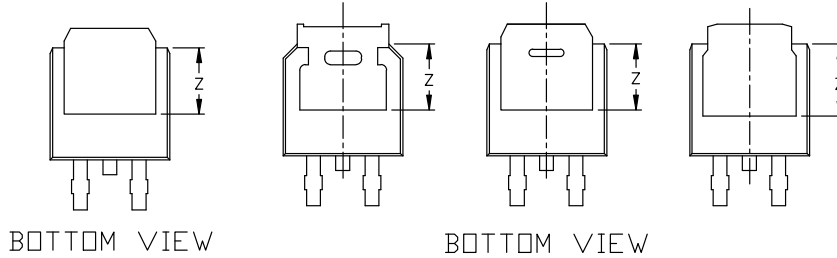


SIDE VIEW

NOTES:

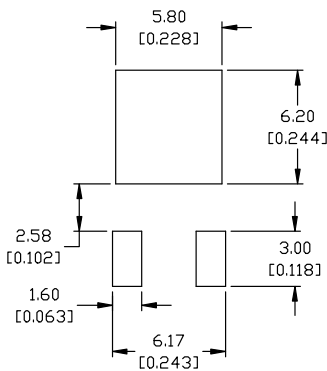
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

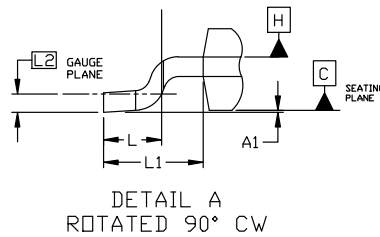
ALTERNATE CONSTRUCTIONS



### RECOMMENDED MOUNTING FOOTPRINT\*

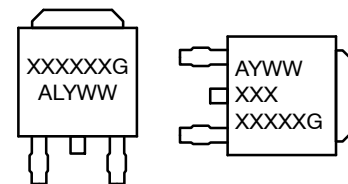
\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- |  |  |   |   |  |
|--|--|---|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN          | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE              | <b>STYLE 5:</b><br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE     |
| <b>STYLE 6:</b><br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2                 | <b>STYLE 7:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 8:</b><br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE   | <b>STYLE 9:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |



DETAIL A  
ROTATED 90° CW

### GENERIC MARKING DIAGRAM\*



- IC**                      **Discrete**
- XXXXXX = Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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