

# NST45011MW6T1G, NSVT45011MW6T3G

## Dual Matched General Purpose Transistor

### NPN Matched Pair

These transistors are housed in an ultra-small SOT-363 package ideally suited for portable products. They are assembled to create a pair of devices highly matched in all parameters, eliminating the need for costly trimming. Applications are Current Mirrors; Differential, Sense and Balanced Amplifiers; Mixers; Detectors and Limiters.

#### Features

- Current Gain Matching to 10%
- Base-Emitter Voltage Matched to 2 mV
- Drop-In Replacement for Standard Device
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	$V_{CEO}$	45	V
Collector - Base Voltage	$V_{CBO}$	50	V
Emitter - Base Voltage	$V_{EBO}$	6.0	V
Collector Current - Continuous	$I_C$	100	mA <sub>dc</sub>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation Per Device	$P_D$	380	mW
FR-5 Board (Note 1) $T_A = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$		250	
		3.0	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	328	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-5 = 1.0 x 0.75 x 0.062 in

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

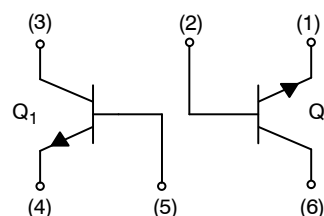


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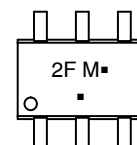
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SOT-363  
CASE 419B  
STYLE 1



#### MARKING DIAGRAMS



2F = Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
NST45011MW6T1G	SOT-363 (Pb-Free)	3,000 / Tape & Reel
NSVT45011MW6T3G	SOT-363 (Pb-Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NST45011MW6T1G, NSVT45011MW6T3G

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector – Emitter Breakdown Voltage, ( $I_C = 10\text{ mA}$ )	$V_{(BR)CEO}$	45	–	–	V
Collector – Emitter Breakdown Voltage, ( $I_C = 10\ \mu\text{A}$ , $V_{EB} = 0$ )	$V_{(BR)CES}$	50	–	–	V
Collector – Base Breakdown Voltage, ( $I_C = 10\ \mu\text{A}$ )	$V_{(BR)CBO}$	50	–	–	V
Emitter – Base Breakdown Voltage, ( $I_E = 1.0\ \mu\text{A}$ )	$V_{(BR)EBO}$	6.0	–	–	V
Collector Cutoff Current ( $V_{CB} = 30\text{ V}$ ) ( $V_{CB} = 30\text{ V}$ , $T_A = 150^\circ\text{C}$ )	$I_{CBO}$	–	–	15 5.0	nA $\mu\text{A}$
<b>ON CHARACTERISTICS</b>					
DC Current Gain ( $I_C = 10\ \mu\text{A}$ , $V_{CE} = 5.0\text{ V}$ ) ( $I_C = 2.0\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ ) ( $I_C = 2.0\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ ) (Note 2)	$h_{FE}$  $h_{FE(1)}/h_{FE(2)}$	150 200 0.9	– 300 1.0	– 500 1.1	–
Collector – Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0.5\text{ mA}$ ) ( $I_C = 100\text{ mA}$ , $I_B = 5.0\text{ mA}$ )	$V_{CE(sat)}$	– –	– –	250 600	mV
Base – Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0.5\text{ mA}$ ) ( $I_C = 100\text{ mA}$ , $I_B = 5.0\text{ mA}$ )	$V_{BE(sat)}$	700 850	750 890	800 950	mV
Base – Emitter On Voltage ( $I_C = 2.0\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ ) ( $I_C = 10\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ ) ( $I_C = 2.0\text{ mA}$ , $V_{CE} = 5.0\text{ V}$ ) (Note 3)	$V_{BE(on)}$  $V_{BE(1)} - V_{BE(2)}$	580 – –	660 – 1.0	700 770 2.0	mV
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Current – Gain – Bandwidth Product, ( $I_C = 10\text{ mA}$ , $V_{CE} = 5\text{ Vdc}$ , $f = 100\text{ MHz}$ )	$f_T$	100	–	–	MHz
Output Capacitance, ( $V_{CB} = 10\text{ V}$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	–	–	4.5	pF
Noise Figure, ( $I_C = 0.2\text{ mA}$ , $V_{CE} = 5\text{ Vdc}$ , $R_S = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $BW = 200\text{Hz}$ )	NF	–	–	10	dB
Noise Figure, ( $I_C = 0.1\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $R_S = 1\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $BW = 200\text{Hz}$ )	NF	–	1.0	–	dB

2.  $h_{FE(1)}/h_{FE(2)}$  is the ratio of one transistor compared to the other transistor within the same package. The smaller  $h_{FE}$  is used as numerator.  
 3.  $V_{BE(1)} - V_{BE(2)}$  is the absolute difference of one transistor compared to the other transistor within the same package.

TYPICAL CHARACTERISTICS

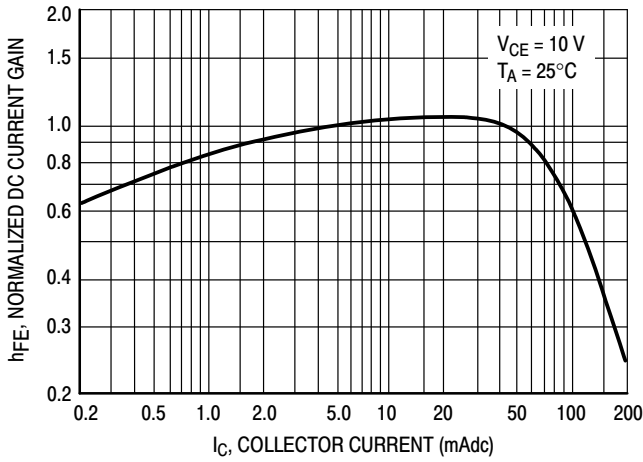


Figure 1. Normalized DC Current Gain

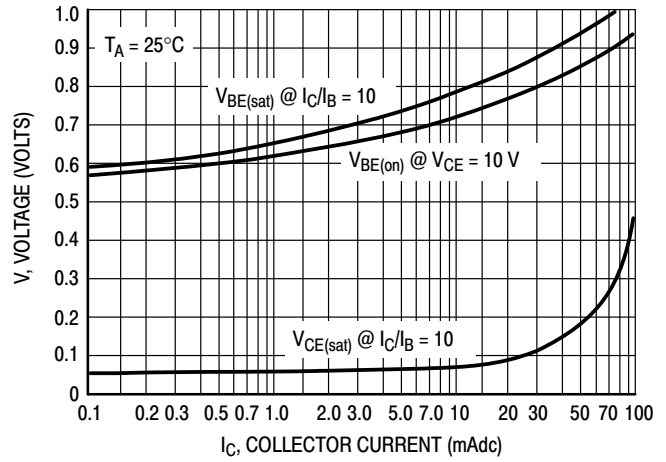


Figure 2. "Saturation" and "On" Voltages

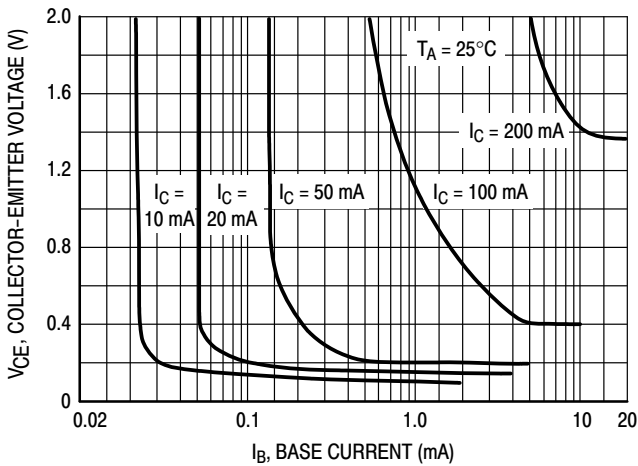


Figure 3. Collector Saturation Region

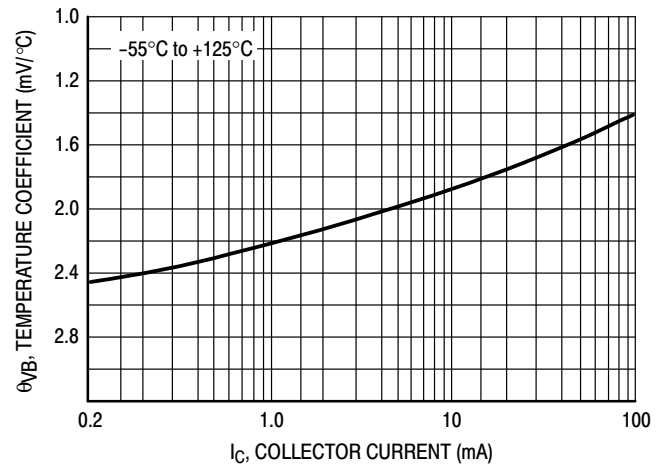


Figure 4. Base-Emitter Temperature Coefficient

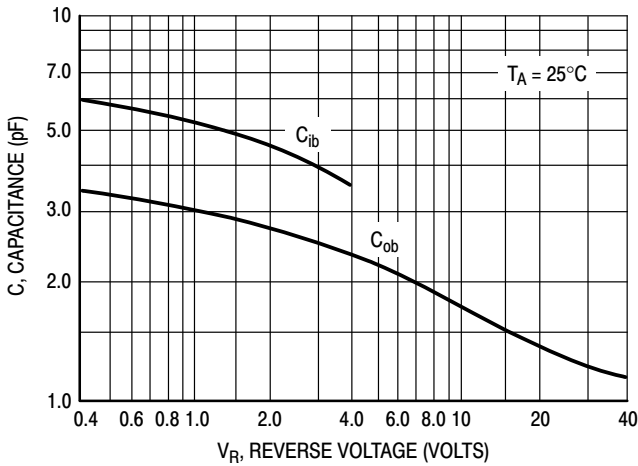


Figure 5. Capacitances

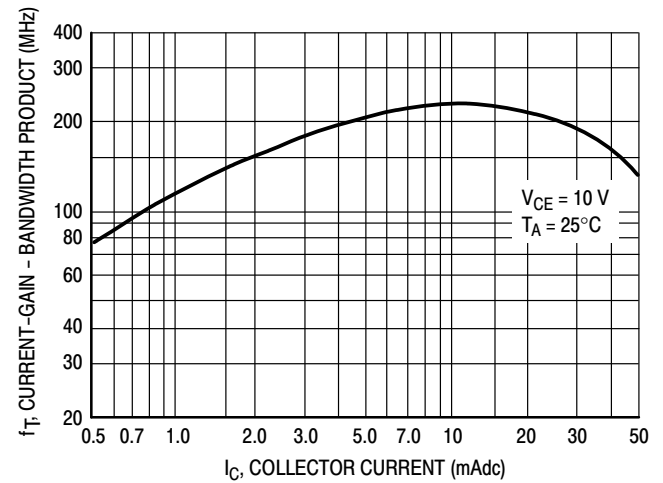


Figure 6. Current-Gain - Bandwidth Product

# NST45011MW6T1G, NSVT45011MW6T3G

## TYPICAL CHARACTERISTICS

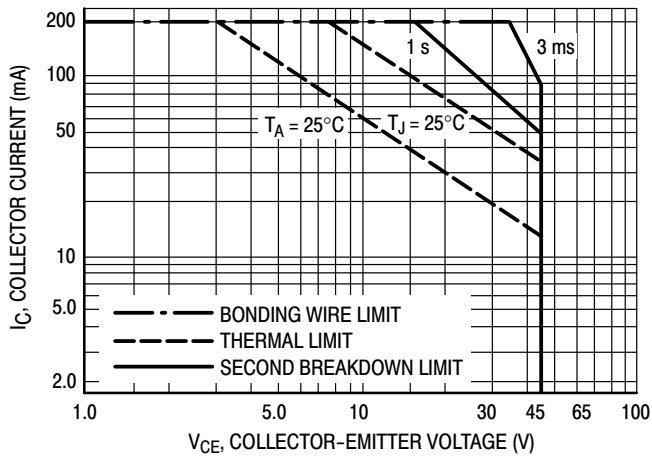


Figure 7. Active Region Safe Operating Area

The safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 7 is based upon  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  or  $T_A$  is variable depending upon conditions.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1  
SCALE 2:1

SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE Y

DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

### GENERIC MARKING DIAGRAM\*



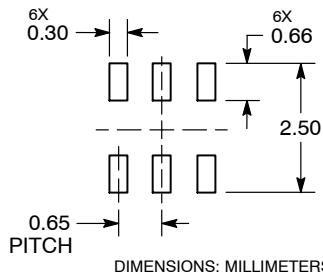
- XXX = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### STYLES ON PAGE 2

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**SC-88/SC70-6/SOT-363**  
**CASE 419B-02**  
**ISSUE Y**

DATE 11 DEC 2012

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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