

NMLU1210

Full Bridge Rectifier

Dual 20 V N-Channel with dual 3.2 A Schottky Barrier Diode, 4.0 x 4.0 x 0.5 mm μ Cool™ Package

Features

- Full-Bridge Rectifier Block
- Up to 3.2 A operation
- Low $R_{DS(on)}$ MOSFET to minimize conduction loss
- Low gate charge MOSFET
- Low V_F Schottky diode
- Ultra Low Inductance Package
- This Device uses Halogen-Free Molding Compound
- These are Pb-Free Devices

Applications

- Wireless Charging
- AC-DC Rectification
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

RECTIFIER MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Input voltage between two MOSFET drain	V_{LL}	20	V	
Bridge Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 125	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	
Continuous Drain Current R_{JA} (Note 1)	I_O	$T_A = 25^\circ\text{C}$	2.2	A
		$T_A = 85^\circ\text{C}$	1.16	
Power Dissipation R_{JA} (Note 1)	P_D	$T_A = 25^\circ\text{C}$	1.2	W
		$T_A = 85^\circ\text{C}$	0.47	
Continuous Drain Current $R_{JA} t < 5$ s (Note 1)	I_O	$T_A = 25^\circ\text{C}$	3.2	A
		$T_A = 85^\circ\text{C}$	1.88	
Power Dissipation $R_{JA} t < 5$ s (Note 1)	P_D	$T_A = 25^\circ\text{C}$	2.34	W
		$T_A = 85^\circ\text{C}$	0.94	
Continuous Drain Current R_{JA} (Note 2)	I_O	$T_A = 25^\circ\text{C}$	1.16	A
		$T_A = 85^\circ\text{C}$	0.6	
Power Dissipation R_{JA} (Note 2)	P_D	$T_A = 25^\circ\text{C}$	0.47	W
		$T_A = 85^\circ\text{C}$	0.185	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.



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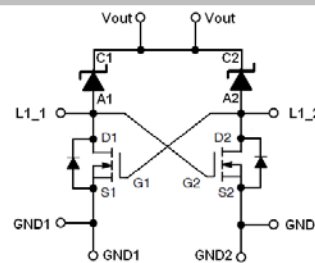
<http://onsemi.com>

MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	23 m Ω @ 4.5 V	3.2 A
	17 m Ω @ 10 V	

SCHOTTKY DIODE

V_R MAX	V_F TYP	I_F MAX
20 V	0.45 V	3.2 A



RECTIFIER

4.0 4.0 mm μ Cool Pin Connections (Top View)

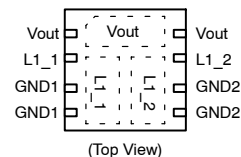
MARKING DIAGRAM



1210 = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(*Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NMLU1210TWG	UDFN (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	82.5	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	42.5	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	209	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

BRIDGE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Rectifying Forward Voltage (Note 5)	V_{fd2}	Input voltage $V_{LL} = \pm 5$ V; The output current of Rectifier $I_{out} = 2$ A		0.45	.56	V
Rectifier leakage current	I_{leak}	Input voltage $V_{LL} = 16$ V; No Load on the Rectifier output		31	1000	uA
Rectifier Reverse leakage current	I_{rleak}	Input voltage $V_{LL} = 0$ V; The output voltage of the Rectifier $V_{out} = 5$ V		21	1000	uA

5. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μA	1.2		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$			4		mV/°C
Drain-to-Source On Resistance (Note 6)	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.2$ A		17	26	m Ω
		$V_{GS} = 4.5$ V, $I_D = 3.2$ A		23	32	
Forward Transconductance	g_{FS}	$V_{DS} = 10$ V, $I_D = 2.0$ A		3.5		S

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 6)	V_{SD}	$V_{GS} = 0$ V, $I_S = 2.0$ A	$T_J = 25^\circ\text{C}$		0.79	V
			$T_J = 125^\circ\text{C}$		0.65	

6. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Instantaneous Forward Voltage (Note 7)	V_F	$I_F = 1.0$ A		0.36		V
		$I_F = 2.0$ A		0.41		
Maximum Instantaneous Reverse Current	I_R	$V_R = 20$ V		0.04		mA

7. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 100^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Instantaneous Forward Voltage (Note 8)	V_F	$I_F = 1.0$ A		0.29		V
		$I_F = 2.0$ A		0.36		
Maximum Instantaneous Reverse Current	I_R	$V_R = 20$ V		4		mA

8. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$
 9. For detailed MOSFET and Diode parameters, please refer to the ON Semiconductor datasheets of NTTFS4930N and MBR230LSFT1G. The test on each individual die is limited to the system package.

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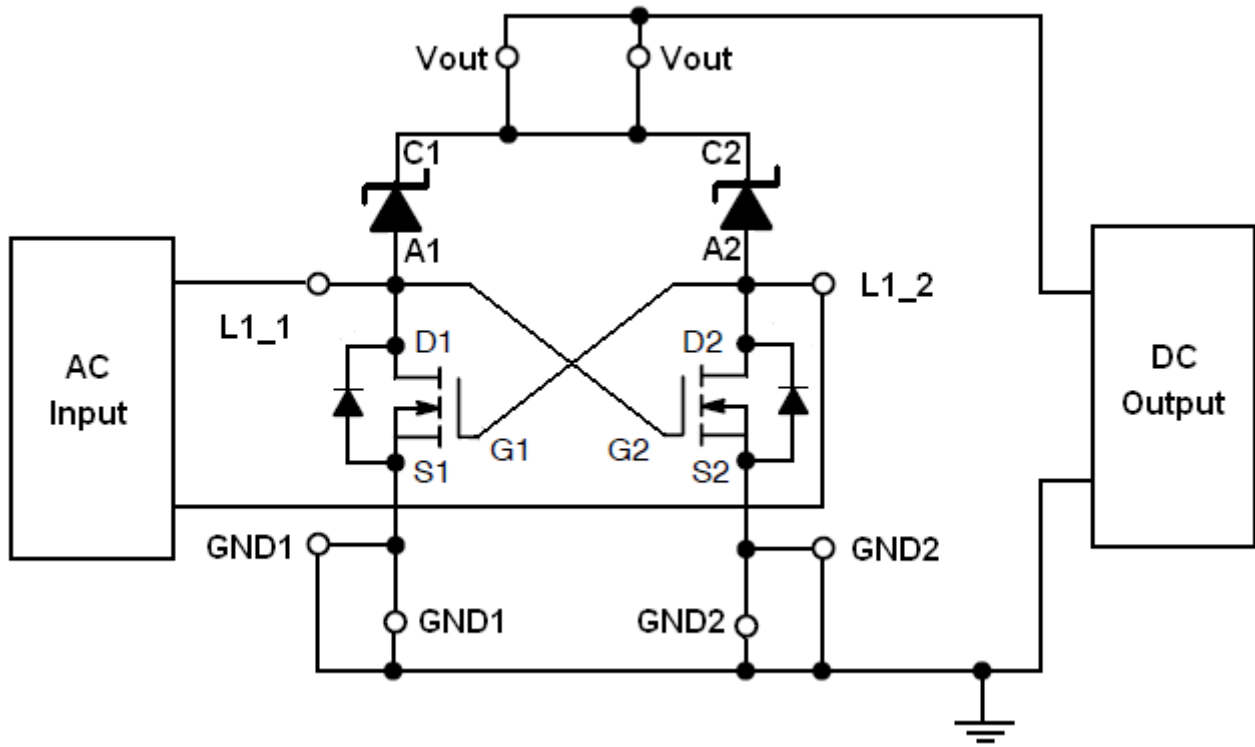


Figure 1. Typical Application Circuit

GND1 and GND2 are not internally connected. The user should make the connection in the PCB design.

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise specified)

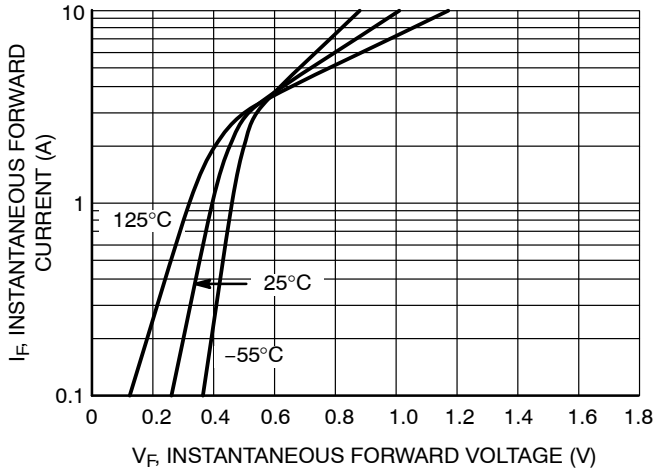


Figure 2. Bridge Typical Forward Voltage Drop at $V_{in} \geq 5\text{ V}$

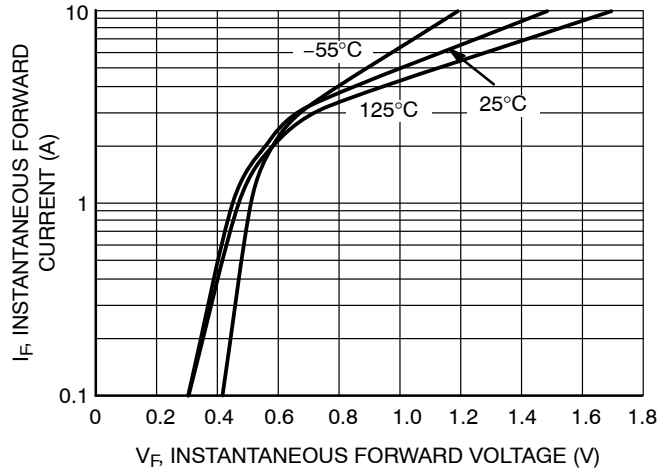


Figure 3. Bridge Maximum Forward Voltage Drop at $V_{in} \geq 5\text{ V}$

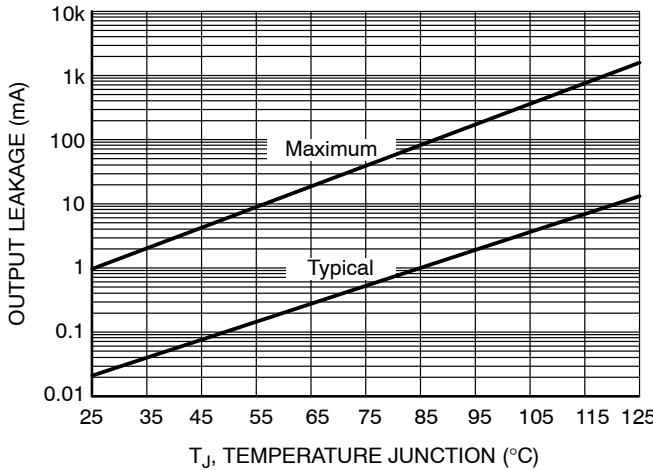


Figure 4. Output Leakage at 5 V Bias vs. Junction Temperature

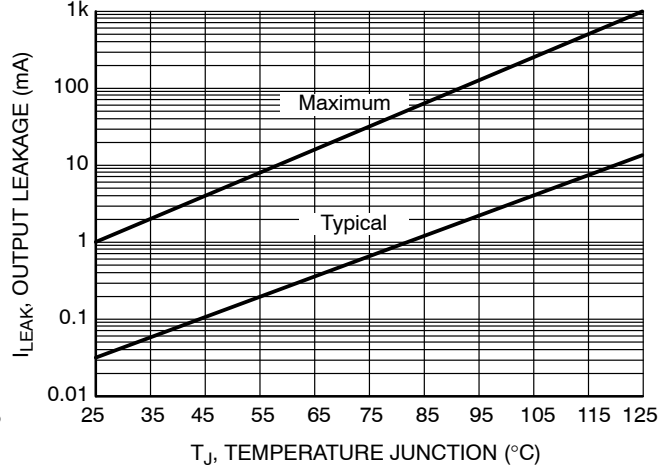


Figure 5. Input Leakage at 16 V vs. Junction Temperature

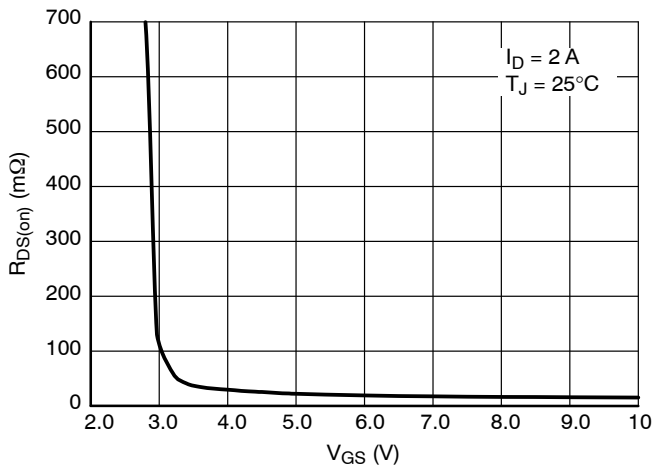


Figure 6. FET Typical On-Resistance vs. Gate-to-Source Voltage (from 3 V to 10 V)

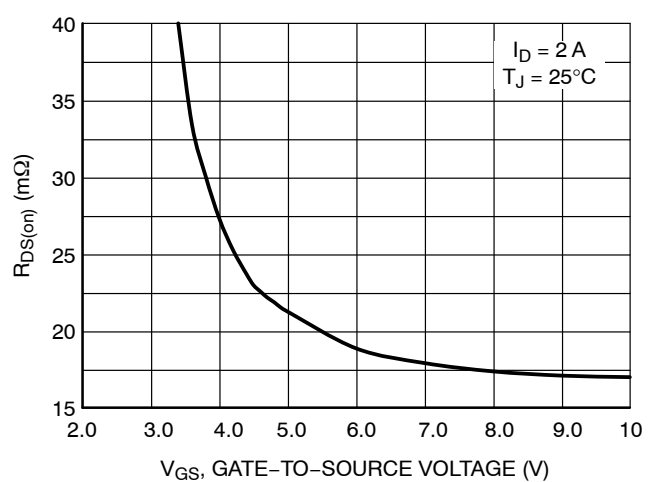


Figure 7. FET Typical On-Resistance vs. Gate-to-Source Voltage

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TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise specified)

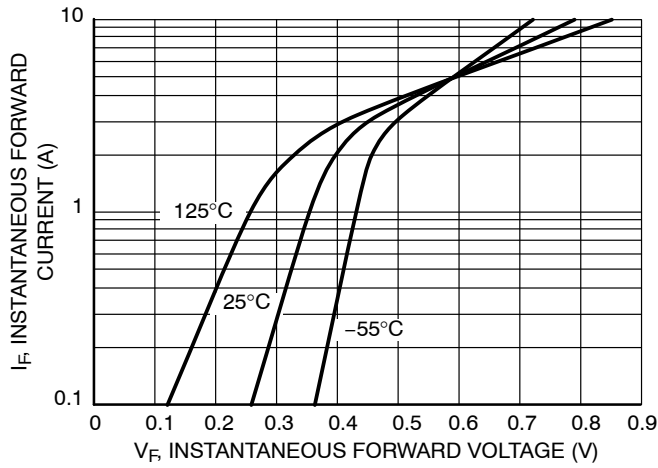


Figure 8. Schottky Typical Forward Current vs. Forward Voltage

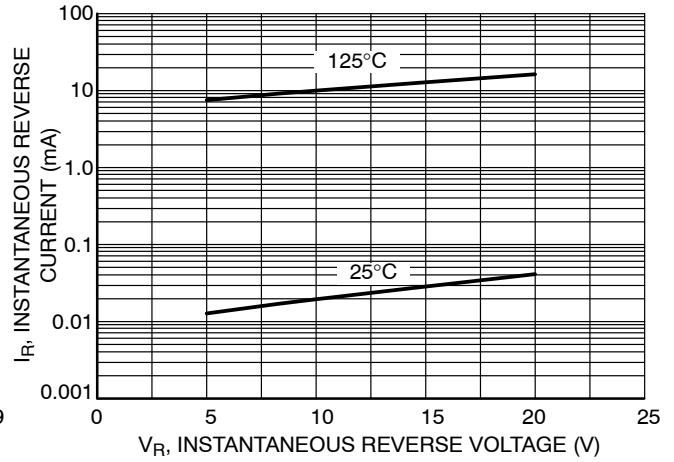


Figure 9. Schottky Typical Reverse Current vs. Reverse Voltage

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

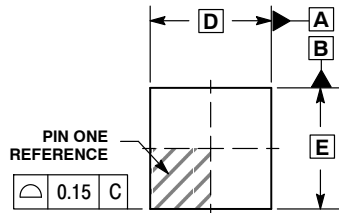
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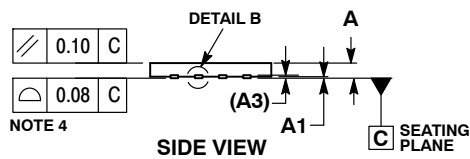
UDFN8 4x4, 0.8P CASE 517BS ISSUE A

DATE 06 SEP 2011

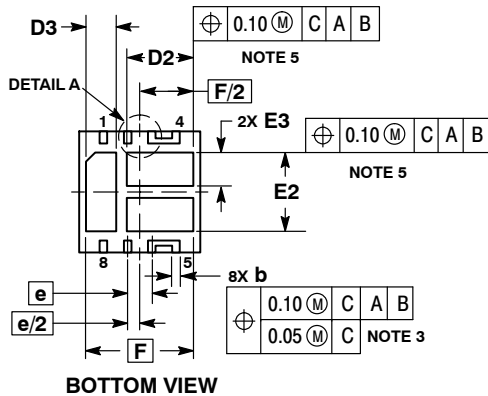
SCALE 2:1



TOP VIEW

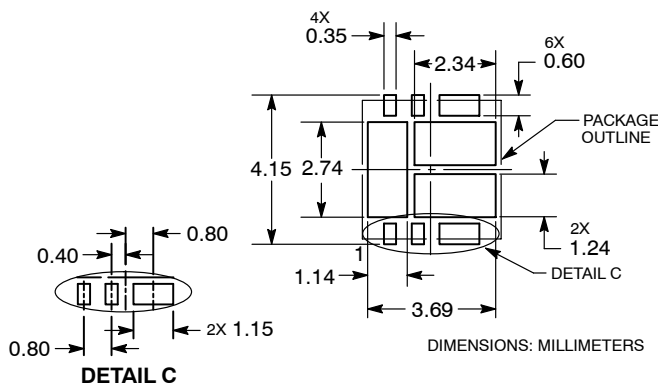


SIDE VIEW

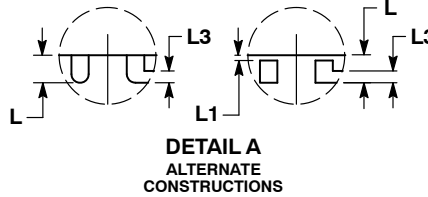


BOTTOM VIEW

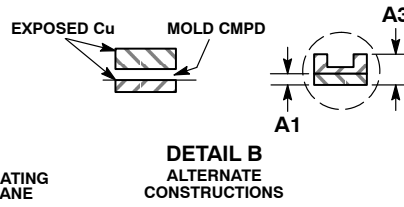
RECOMMENDED SOLDERING FOOTPRINT*



DETAIL C



DETAIL A
ALTERNATE
CONSTRUCTIONS



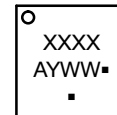
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE EXPOSED PADS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	4.00	BSC
D2	2.10	2.30
D3	0.90	1.10
E	4.00	BSC
E2	2.50	2.70
E3	1.00	1.20
e	0.80	BSC
F	3.55	BSC
L	0.30	0.50
L1	0.00	0.15
L3	0.13	0.23

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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