

# NLSF3T126

## Quad Bus Buffer with 3-State Control Inputs

The NLSF3T126 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves noninverting high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The NLSF3T126 requires the 3-state control input (OE) to be set Low to place the output into high impedance.

The T126 inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The NLSF3T126 input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $t_{PD} = 3.8$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4.0$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- Pb-Free Package is Available\*

FUNCTION TABLE

Inputs		Output
A	OE	Y
L	H	L
H	H	H
X	L	Z

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



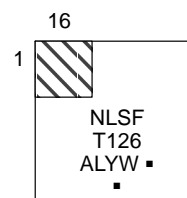
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QFN-16  
CASE 485G

### MARKING DIAGRAM



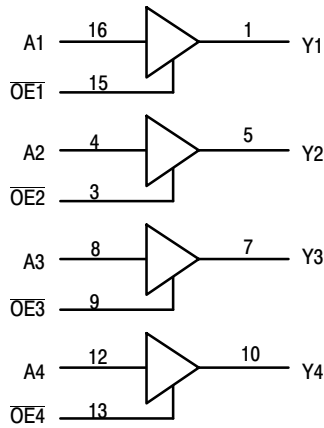
NLSFT126 = Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### ORDERING INFORMATION

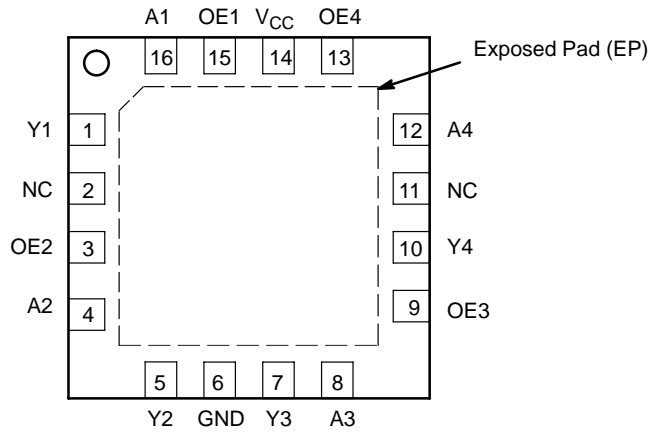
Device	Package	Shipping†
NLSF3T126MNR2	QFN-16	3000/Tape & Reel
NLSF3T126MNR2G	QFN-16 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NLSF3T126



**Figure 1. Logic Diagram  
Active-High Output Enables**



**Figure 2. QFN – 16 Pinout (Top View)**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage	$V_{in}$	-0.5 to +7.0	V
DC Output Voltage	$V_{out}$	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )	$I_{OK}$	$\pm 20$	mA
DC Output Current, per Pin	$I_{out}$	$\pm 25$	mA
DC Supply Current, $V_{CC}$ and GND Pins	$I_{CC}$	$\pm 75$	mA
Power Dissipation in Still Air, QFN Packages	$P_D$	500	mW
Storage Temperature	$T_{stg}$	-65 to +150	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	$V_{CC}$	2.0	5.5	V
DC Input Voltage	$V_{in}$	0	5.5	V
DC Output Voltage	$V_{out}$	0	5.5 $V_{CC}$	V
Operating Temperature	$T_A$	-40	+85	$^{\circ}C$
Input Rise and Fall Time	$t_r, t_f$	0	20	ns/V

# NLSF3T126

## DC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Symbol	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Minimum High-Level Input Voltage	2.3 V ± 0.3 V 3.3 V ± 0.3 V 5.0 V ± 0.5 V	V <sub>IH</sub>		0.5 V <sub>CC</sub> 0.4 V <sub>CC</sub> 0.44 V <sub>CC</sub>			0.5 V <sub>CC</sub> 0.4 V <sub>CC</sub> 0.44 V <sub>CC</sub>		0.5 V <sub>CC</sub> 0.4 V <sub>CC</sub> 0.44 V <sub>CC</sub>		V
Maximum Low-Level Input Voltage	2.3 V ± 0.3 V 3.3 V ± 0.3 V 5.0 V ± 0.5 V	V <sub>IL</sub>				0.3 V <sub>CC</sub> 0.18 V <sub>CC</sub> 0.18 V <sub>CC</sub>		0.3 V <sub>CC</sub> 0.18 V <sub>CC</sub> 0.18 V <sub>CC</sub>		0.3 V <sub>CC</sub> 0.18 V <sub>CC</sub> 0.18 V <sub>CC</sub>	V
Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>OL</sub> @ I <sub>OL</sub> , 50 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	V <sub>OH</sub>	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -2.0 mA I <sub>OH</sub> = -4.0 mA I <sub>OH</sub> = -8.0 mA		2.0 3.0 4.5	1.82 2.58 3.94			1.72 2.48 3.80		1.60 2.34 3.66		
Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>OL</sub> @ I <sub>OL</sub> , 50 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	V <sub>OL</sub>	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 2.0 mA I <sub>OL</sub> = 4.0 mA I <sub>OL</sub> = 8.0 mA		2.0 3.0 4.5			0.36 0.36 0.36		0.44 0.44 0.44		0.52 0.52 0.52	
Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	I <sub>IN</sub>	0 to 5.5			±0.1		±1.0		±1.0	μA
Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	I <sub>CC</sub>	5.5			2.0		20		40	μA
Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	I <sub>CCT</sub>	5.5			1.35		1.50		1.65	mA
Maximum 3-State Leakage Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	I <sub>OZ</sub>	5.5			±0.25		±2.5		±2.5	μA
Output Leakage Current	V <sub>OUT</sub> = 5.5 V	I <sub>OPD</sub>	0.0			0.5		5.0		10	μA

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Parameter	Test Conditions	Symbol	$T_A = 25^\circ\text{C}$			$T_A = \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Maximum Propagation Delay, A to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	$t_{PLH}$ , $t_{PHL}$	1.0	14.5	16.9	1.0	18.1	1.0	19.2	ns
	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		1.0 1.0	5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	12.0 16.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		1.0 1.0	3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5	1.0 1.0	8.5 10.5	ns
Maximum Output Enable Time, $\overline{OE}$ to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	$t_{PZL}$ , $t_{PZH}$	1.0	14.8	16.2	1.0	17.4	1.0	19.3	ns
	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $R_L = 1.0$ k $\Omega$ $C_L = 50$ pF		1.0 1.0	5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	11.5 15.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1.0$ k $\Omega$ $C_L = 50$ pF		1.0 1.0	3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0	1.0 1.0	7.5 9.5	ns
Maximum Output Disable Time, $\overline{OE}$ to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	$t_{PLZ}$ , $t_{PHZ}$	1.0	15.4	18.0	1.0	19.8	1.0	22.0	ns
	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF $R_L = 1.0$ k $\Omega$		1.0	9.5	13.2	1.0	15.0	1.0	18.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1.0$ k $\Omega$		1.0	6.1	8.8	1.0	10.0	1.0	12.0	ns
Output-to-Output Skew	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF (Note 1)	$t_{OSLH}$ , $t_{OSHL}$			1.5		1.5		2.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 1)				1.0		1.0		1.5	ns
Maximum Input Capacitance		$C_{in}$		4.0	10		10		10	pF
Maximum 3-State Output Capacitance (Output in High Impedance State)		$C_{out}$		6.0						pF
Power Dissipation Capacitance (Note 2)		$C_{PD}$	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0$ V						pF	
			15							

1. Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ .

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$  (per buffer).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Characteristic	Symbol	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
Quiet Output Maximum Dynamic $V_{OL}$	$V_{OLP}$	0.3	0.8	V
Quiet Output Minimum Dynamic $V_{OL}$	$V_{OLV}$	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	$V_{IHD}$		3.5	V
Maximum Low Level Dynamic Input Voltage	$V_{ILD}$		1.5	V

SWITCHING WAVEFORMS

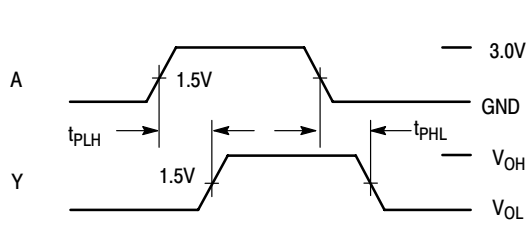


Figure 3.

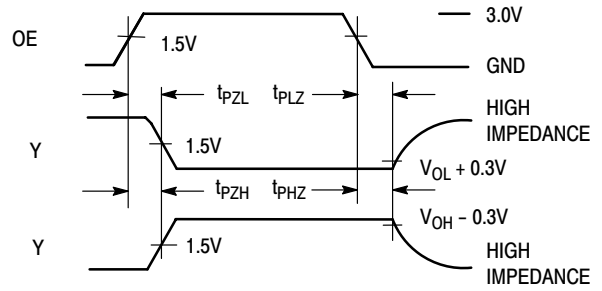
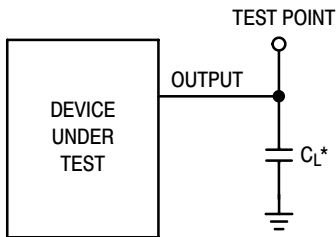
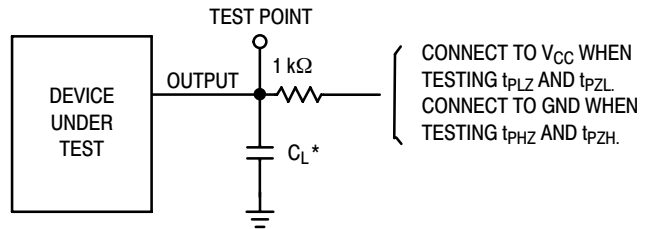


Figure 4.



\*Includes all probe and jig capacitance

Figure 5. Test Circuit



\*Includes all probe and jig capacitance

Figure 6. Test Circuit

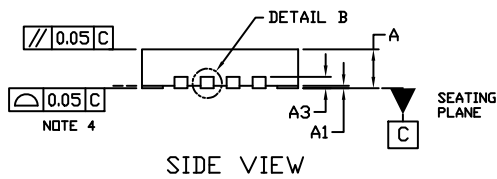
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

**QFN16 3x3, 0.5P**  
CASE 485G  
ISSUE G

DATE 08 OCT 2021

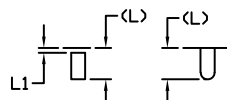


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



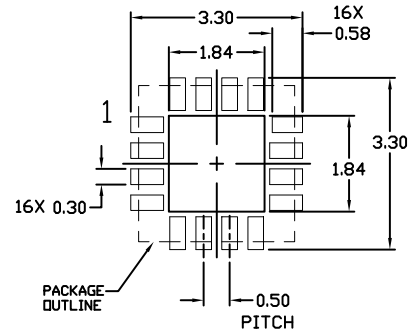
DETAIL B  
ALTERNATE  
CONSTRUCTIONS



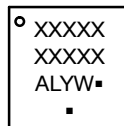
DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

**MOUNTING FOOTPRINT**



**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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