

# NLAST4501

## Single SPST Analog Switch

The NLAST4501 is an analog switch manufactured in sub-micron silicon-gate CMOS technology. It achieves very low  $R_{ON}$  while maintaining extremely low power dissipation. The device is a bilateral switch suitable for switching either analog or digital signals, which may vary from zero to full supply voltage.

The NLAST4501 is a low voltage, TTL (low threshold) compatible device, pin for pin compatible with the MAX4501.

The Enable pin is compatible with standard TTL level outputs when supply voltage is nominal 5.0 V. It is also over-voltage tolerant, making it a very useful logic level translator.

### Features

- Guaranteed  $R_{ON}$  of  $32\ \Omega$  at 5.5 V
- Low Power Dissipation:  $I_{CC} = 2\ \mu A$
- Low Threshold Enable pin TTL compatible at 5.0 V
- TTL version and pin for pin with NLA4501
- Provides Voltage translation for many different voltage levels
  - 3.3 to 5.0 V, Enable pin may go as high as +5.5 V
  - 1.8 to 3.3 V
  - 1.8 to 2.5 V
- Improved version of MAX4501 (at any voltage between 2 and 5.5 V)
- Chip Complexity: FETs = 11
- Pb-Free Packages are Available

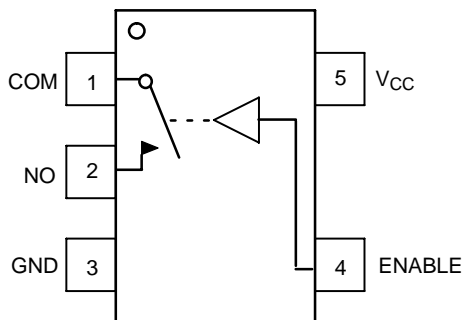


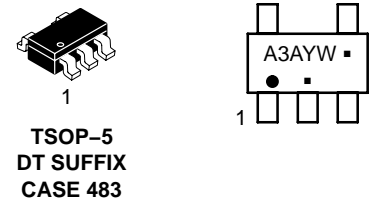
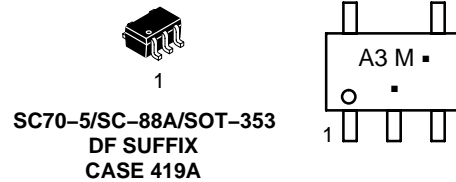
Figure 1. Pinout (Top View)



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### MARKING DIAGRAMS



A3 = Specific Device Code  
 M = Date Code\*  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position and underbar may vary depending upon manufacturing location.

### PIN ASSIGNMENT

Pin	Function
1	COM
2	NO
3	GND
4	ENABLE
5	$V_{CC}$

### FUNCTION TABLE

On/Off Enable Input	State of Analog Switch
L	Off
H	On

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# NLAST4501

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Positive DC Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
Digital Input Voltage (Enable)	$V_{IN}$	-0.5 to +7.0	V
Analog Output Voltage ( $V_{NO}$ or $V_{COM}$ )	$V_{IS}$	-0.5 to $V_{CC} + 0.5$	V
DC Current, Into or Out of Any Pin	$I_{IK}$	$\pm 20$	mA
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}C$
Lead Temperature, 1 mm from Case for 10 Seconds	$T_L$	260	$^{\circ}C$
Junction Temperature under Bias	$T_J$	+150	$^{\circ}C$
Thermal Resistance	SC70-5/SC-88A (Note 1) TSOP-5	$\theta_{JA}$ 350 230	$^{\circ}C/W$
Power Dissipation in Still Air at 85 $^{\circ}C$	SC70-5/SC-88A TSOP-5	$P_D$ 150 200	mW
Moisture Sensitivity	MSL	Level 1	
Flammability Rating	Oxygen Index: 30% - 35%	$F_R$	UL 94 V-0 @ 0.125 in
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	$V_{ESD}$ > 2000 > 100 N/A	V
Latchup Performance	Above $V_{CC}$ and Below GND at 85 $^{\circ}C$ (Note 5)	$I_{Latchup}$	$\pm 300$ mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Positive DC Supply Voltage	$V_{CC}$	2.0	5.5	V
Digital Input Voltage (Enable)	$V_{IN}$	GND	5.5	V
Static or Dynamic Voltage Across an Off Switch	$V_{IO}$	GND	$V_{CC}$	V
Analog Input Voltage (NO, COM)	$V_{IS}$	GND	$V_{CC}$	V
Operating Temperature Range, All Package Types	$T_A$	-55	+125	$^{\circ}C$
Input Rise or Fall Time, (Enable Input)	$t_r, t_f$	$V_{CC} = 3.3 V \pm 0.3 V$ 0	100 20	ns/V

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature $^{\circ}C$	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

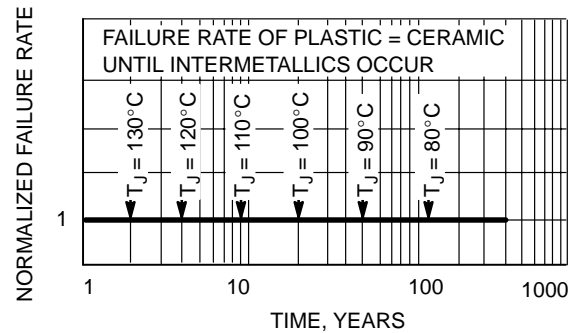


Figure 2. Failure Rate vs. Time Junction Temperature

# NLAST4501

## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V <sub>CC</sub>	Guaranteed Max Limit			Unit
				-55°C to 25°C	< 85°C	< 125°C	
Minimum High-Level Input Voltage, Enable Inputs		V <sub>IH</sub>	3.0	1.4	1.4	1.4	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
Maximum Low-Level Input Voltage, Enable Inputs		V <sub>IL</sub>	3.0	0.53	0.53	0.53	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
Maximum Input Leakage Current, Enable Inputs	V <sub>IN</sub> = 5.5 V or GND	I <sub>IN</sub>	0 V to 5.5 V	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current (per package)	Enable and VIS = V <sub>CC</sub> or GND	I <sub>CC</sub>	5.5	1.0	1.0	2.0	µA

## DC ELECTRICAL CHARACTERISTICS – Analog Section

Parameter	Condition	Symbol	V <sub>CC</sub>	Guaranteed Max Limit			Unit
				-55°C to 25°C	< 85°C	< 125°C	
Maximum ON Resistance (Figures 8 – 12)	V <sub>IN</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to GND  I <sub>IS</sub>   ≤ 10.0mA	R <sub>ON</sub>	3.0	45	50	55	Ω
			4.5	30	35	40	
			5.5	25	30	35	
ON Resistance Flatness	V <sub>IN</sub> = V <sub>IH</sub>  I <sub>IS</sub>   ≤ 10.0 mA V <sub>IS</sub> = 1 V, 2 V, 3.5 V	R <sub>FLAT(ON)</sub>	4.5	4	4	5	Ω
Off Leakage Current, Pin 2 (Figure 3)	V <sub>IN</sub> = V <sub>IL</sub> V <sub>NO</sub> = 1.0 V, V <sub>COM</sub> = 4.5 V or V <sub>COM</sub> = 1.0 V and V <sub>NO</sub> 4.5 V	I <sub>NO(OFF)</sub>	5.5	1	10	100	nA
Off Leakage Current, Pin 1 (Figure 3)	V <sub>IN</sub> = V <sub>IL</sub> V <sub>NO</sub> = 4.5 V or 1.0 V V <sub>COM</sub> = 1.0 V or 4.5 V	I <sub>COM(OFF)</sub>	5.5	1	10	100	nA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns)

Parameter	Test Conditions	Symbol	V <sub>CC</sub> (V)	Guaranteed Max Limit									Unit
				-55°C to 25°C			< 85°C			< 125°C			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Turn-On Time	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 4, 5, and 13)	t <sub>ON</sub>	2.0		7.0	14			16			16	ns
			3.0		5.0	10			12			12	
			4.5		4.5	9			11			11	
			5.5		4.5	9			11			11	
Turn-Off Time	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 4, 5, and 13)	t <sub>OFF</sub>	2.0		11.0	22			24			24	ns
			3.0		7.0	14			16			16	
			4.5		5.0	10			12			12	
			5.5		5.0	10			12			12	
<b>Typical @ 25, VCC = 5.0 V</b>													
Maximum Input Capacitance, Select Input Analog I/O (switch off) Common I/O (switch off) Feedthrough (switch on)	C <sub>IN</sub> C <sub>NO</sub> or C <sub>NC</sub> C <sub>COM(OFF)</sub> C <sub>COM(ON)</sub>							8 10 10 20					pF

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## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Parameter	Condition	Symbol	V <sub>CC</sub> V	Limit 25°C	Unit
Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response	V <sub>IS</sub> = 0 dBm V <sub>IS</sub> centered between V <sub>CC</sub> and GND (Figures 6 and 14)	BW	3.0 4.5 5.5	190 200 220	MHz
Maximum Feedthrough On Loss	V <sub>IS</sub> = 0 dBm @ 10 kHz V <sub>IS</sub> centered between V <sub>CC</sub> and GND (Figure 6)	V <sub>ONL</sub>	3.0 4.5 5.5	-2 -2 -2	dB
Off-Channel Isolation	f = 100 kHz; V <sub>IS</sub> = 1 V RMS V <sub>IS</sub> centered between V <sub>CC</sub> and GND (Figures 6 and 15)	V <sub>ISO</sub>	3.0 4.5 5.5	-93	dB
Charge Injection Enable Input to Common I/O	V <sub>IS</sub> = V <sub>CC</sub> to GND, F <sub>IS</sub> = 20 kHz t <sub>r</sub> = t <sub>f</sub> = 3 ns R <sub>IS</sub> = 0 Ω, C <sub>L</sub> = 1000 pF Q = C <sub>L</sub> * ΔV <sub>OUT</sub> (Figures 7 and 16)	Q	3.0 5.5	1.5 3.0	pC
Total Harmonic Distortion THD + Noise	F <sub>IS</sub> = 20 Hz to 1 MHz, R <sub>L</sub> = R <sub>gen</sub> = 600 Ω, C <sub>L</sub> = 50 pF V <sub>IS</sub> = 3.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 5.0 V <sub>PP</sub> sine wave (Figure 17)	THD	3.3 5.5	0.3 0.15	%

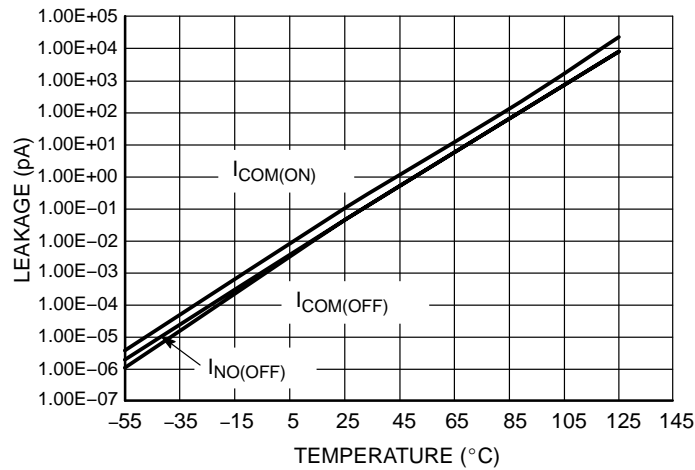


Figure 3. Switch Leakage vs. Temperature

# NLAST4501

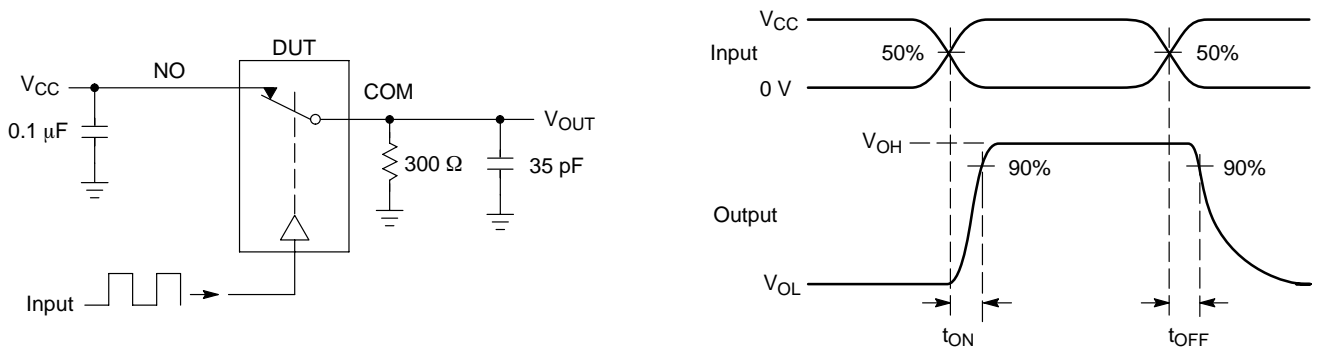


Figure 4.  $t_{ON}/t_{OFF}$

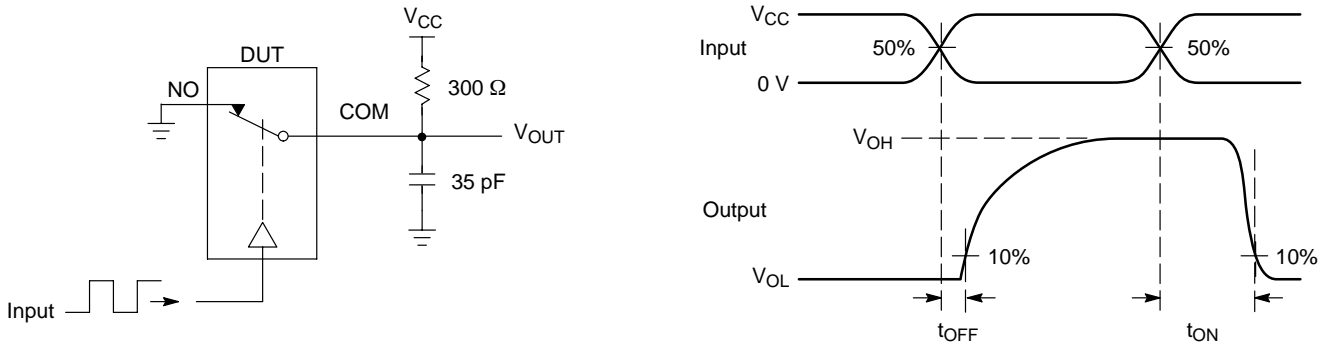
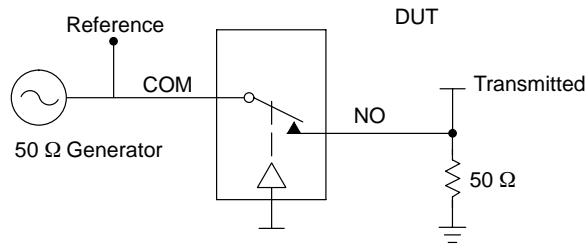


Figure 5.  $t_{ON}/t_{OFF}$

# NLAST4501



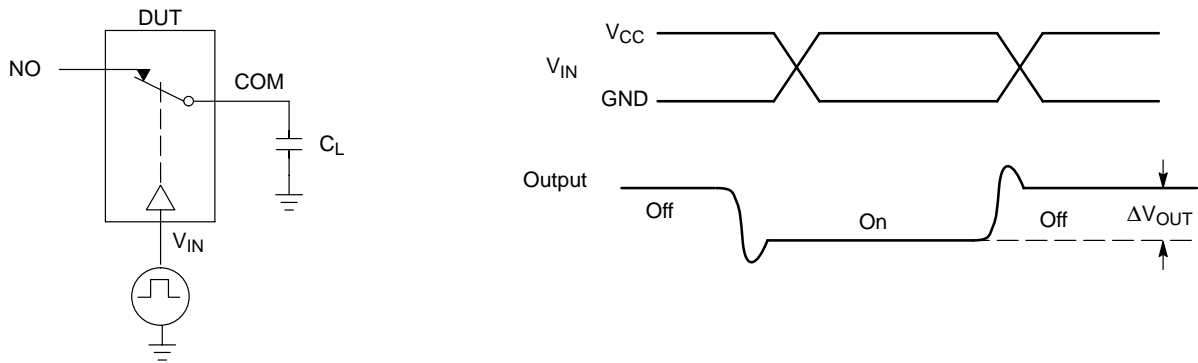
Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

**Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**



**Figure 7. Charge Injection: (Q)**

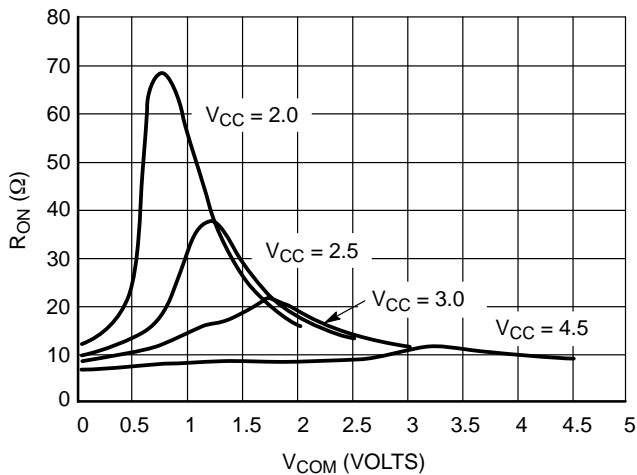


Figure 8.  $R_{ON}$  vs.  $V_{COM}$  and  $V_{CC}$  (@25°C)

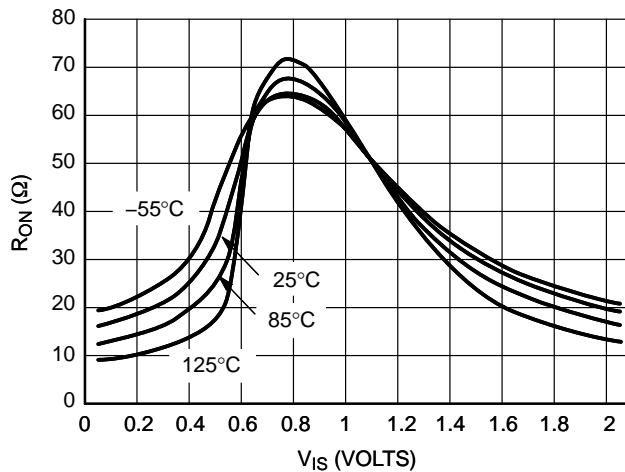


Figure 9.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 2.0$  V

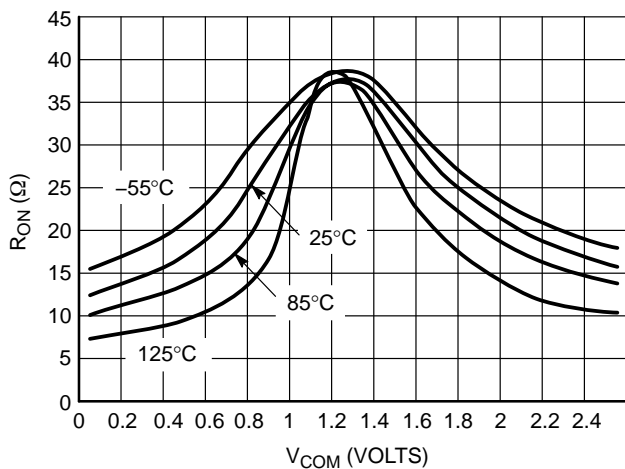


Figure 10.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 2.5$  V

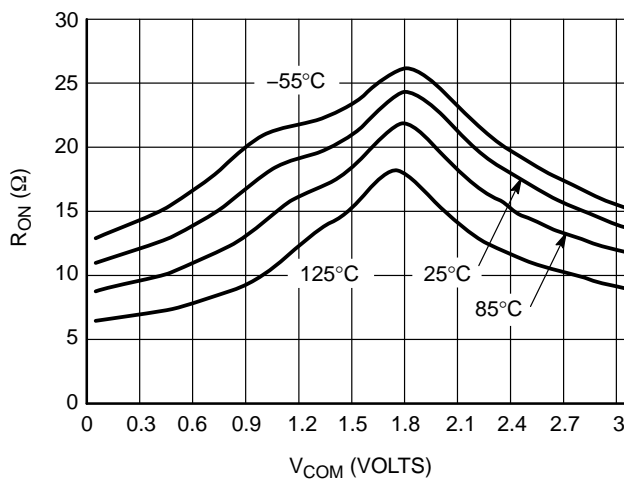


Figure 11.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 3.0$  V

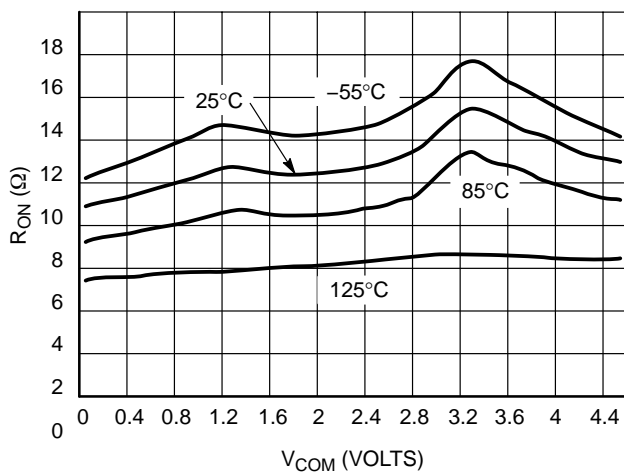


Figure 12.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 4.5$  V

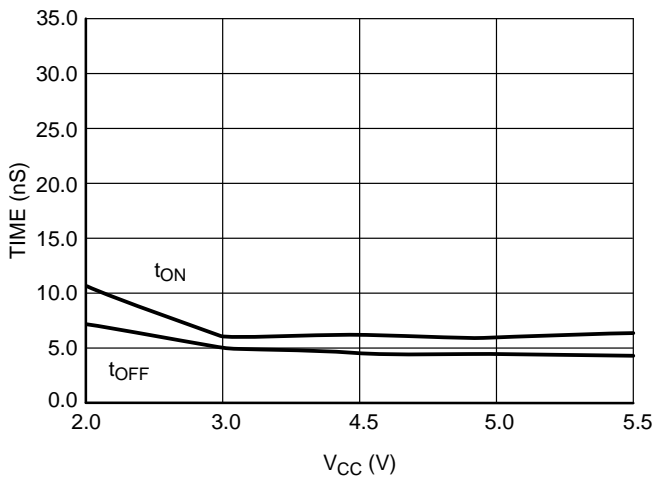


Figure 13. Switching Time vs. Supply Voltage,  $T = 25^\circ\text{C}$

# NLAST4501

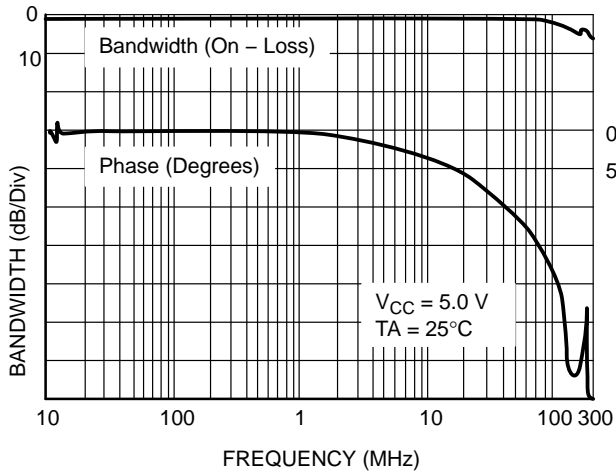


Figure 14. ON Channel Bandwidth and Phase Shift Over Frequency

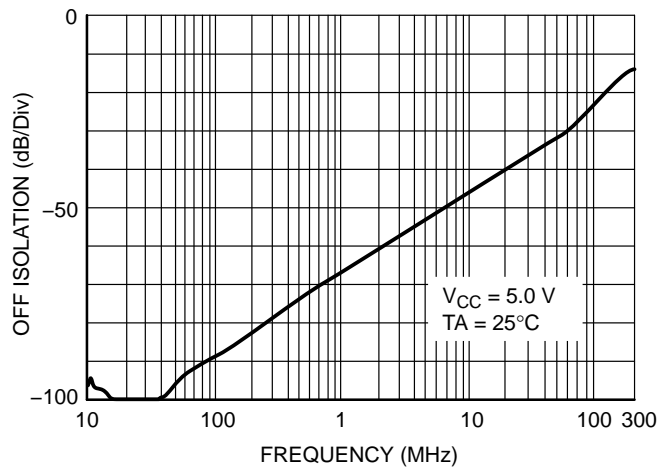


Figure 15. Off Channel Isolation

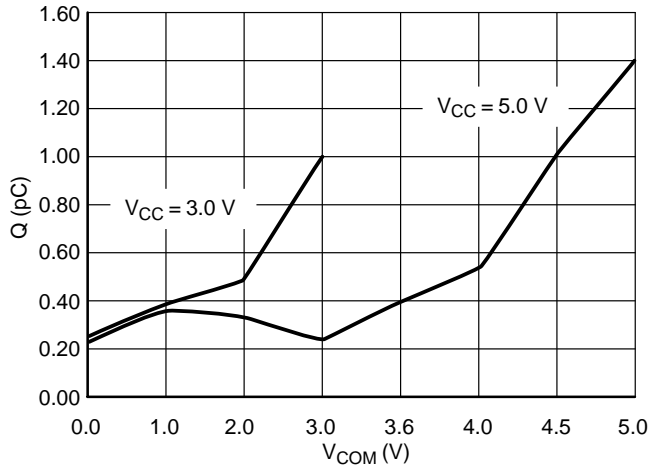


Figure 16. Charge Injection vs.  $V_{COM}$

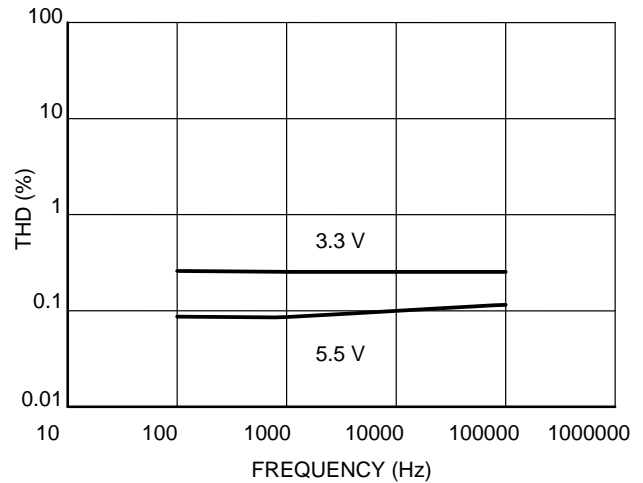


Figure 17. THD vs. Frequency

## ORDERING INFORMATION

Device	Device Nomenclature					Package	Shipping†
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAST4501DFT2	NL	AST	4501	DF	T2	SC-88A/SOT-353/ SC70	3000/Tape & Reel
NLAST4501DFT2G						SC-88A/SOT-353/ SC70 (Pb-Free)	
NLAST4501DFT1				DT	T1	TSOP-5	
NLAST4501DFT1G						TSOP-5 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



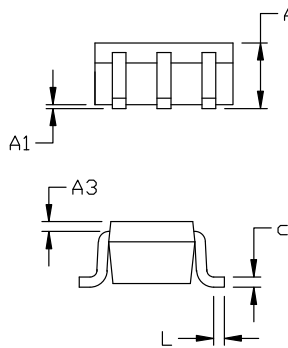
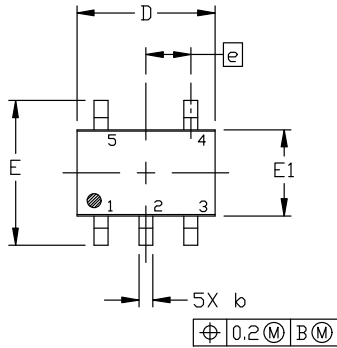
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

## SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



### RECOMMENDED MOUNTING FOOTPRINT

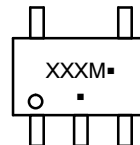
\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

### GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### STYLE 1:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

#### STYLE 2:

1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

#### STYLE 3:

1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

#### STYLE 4:

1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

#### STYLE 5:

1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

#### STYLE 6:

1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

#### STYLE 7:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

#### STYLE 8:

1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

#### STYLE 9:

1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

<b>DOCUMENT NUMBER:</b>	<b>98ASB42984B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SC-88A (SC-70-5/SOT-353)</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

## TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

### SOLDERING FOOTPRINT\*

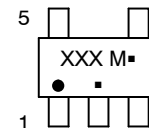


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



Analog



Discrete/Logic

- XXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package
- XXX = Specific Device Code  
 M = Date Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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