

# P-Channel Enhancement Mode Field Effect Transistor

## NDS0610



SOT-23  
CASE 318-08

### General Description

This P-Channel Enhancement Mode Field Effect Transistors are Produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 120 mA DC and can deliver current up to 1 A.

This product is particularly suited to low voltage applications requiring a low current high side switch.

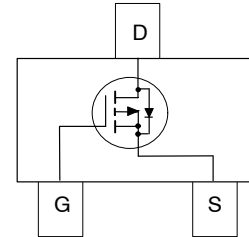
### Features

- -0.12 A, -60 V
  - ◆  $R_{DS(on)} = 10 \Omega @ V_{GS} = -10 V$
  - ◆  $R_{DS(on)} = 20 \Omega @ V_{GS} = -4.5 V$
- Voltage Controlled P-Channel Small Signal Switch
- High Density Cell design for Low  $R_{DS(on)}$
- High Saturation Current

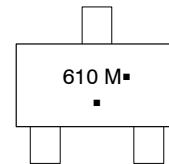
### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	-60	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1)	-0.12	A
	- Pulsed	-1	
$P_D$	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.9	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	°C
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



### MARKING DIAGRAM



610 = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(NOTE: Microdot may be in either location)

\*Date Code orientation and/or location may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NDS0610	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NDS0610

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	350	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -10\ \mu\text{A}$	-60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -10\ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	-53	-	$\text{mV}/^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^{\circ}\text{C}$	-	-	-200	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 10$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -1\text{ mA}$	-1	-1.7	-3.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -1\text{ mA}$ , Referenced to $25^{\circ}\text{C}$	-	-3	-	$\text{mV}/^{\circ}\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -0.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -0.25\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -0.5\text{ A}, T_J = 125^{\circ}\text{C}$	-	1.0 1.3 1.7	10 20 16	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -10\text{ V}$	-0.6	-	-	A
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -0.1\text{ A}$	70	430	-	mS

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	79	-	pF
$C_{oss}$	Output Capacitance		-	10	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	4	-	pF
$R_G$	Gate Resistance	$V_{DS} = -15\text{ mV}, f = 1.0\text{ MHz}$	-	10	-	$\Omega$

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -25\text{ V}, I_D = -0.12\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	-	2.5	5	ns
$t_r$	Turn-On Rise Time		-	6.3	12.6	ns
$t_{d(off)}$	Turn-Off Delay Time		-	10	15	ns
$t_f$	Turn-Off Fall Time		-	7.5	15	ns
$Q_g$	Total Gate Change	$V_{DS} = -48\text{ V}, I_D = -0.5\text{ A},$ $V_{GS} = -10\text{ V}$	-	1.8	2.5	nC
$Q_{gs}$	Gate-Source Change		-	0.3	-	nC
$Q_{gd}$	Gate-Drain Change		-	0.4	-	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	-	-	-0.24	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.24\text{ A}$ (Note 2)	-	-0.8	-1.5	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = -0.5\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 2)	-	17	-	ns
$Q_{rr}$	Diode Reverse Recovery Charge		-	15	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $350\ ^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

TYPICAL CHARACTERISTICS

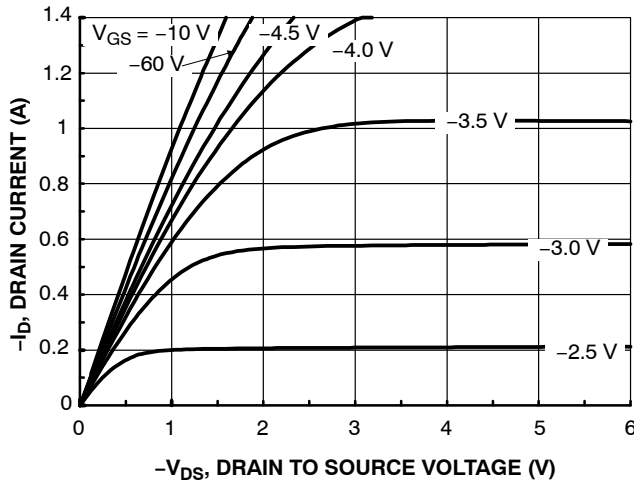


Figure 1. On-Region Characteristics

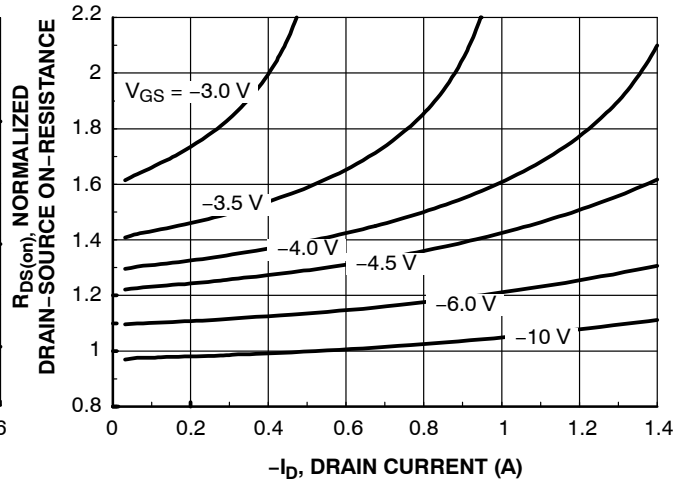


Figure 2. On-Resistance Variation With Drain Current and Gate Voltage

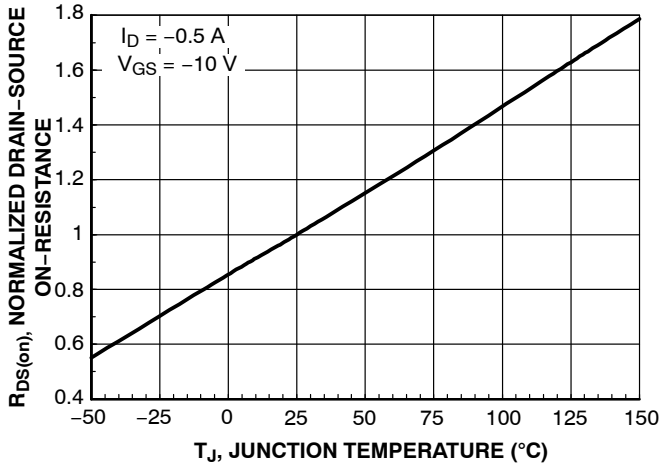


Figure 3. On-Resistance Variation with Temperature

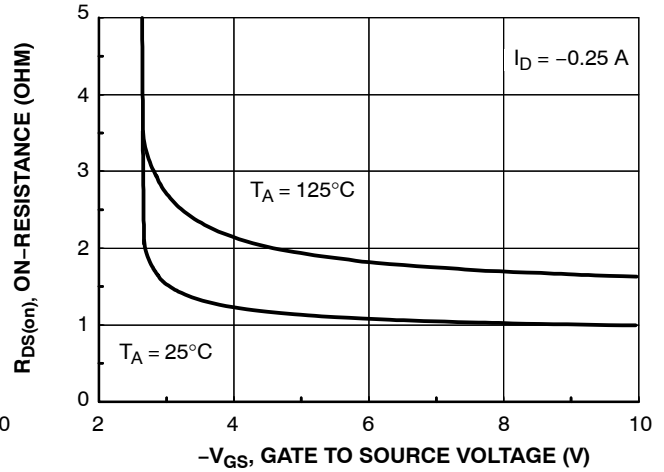


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

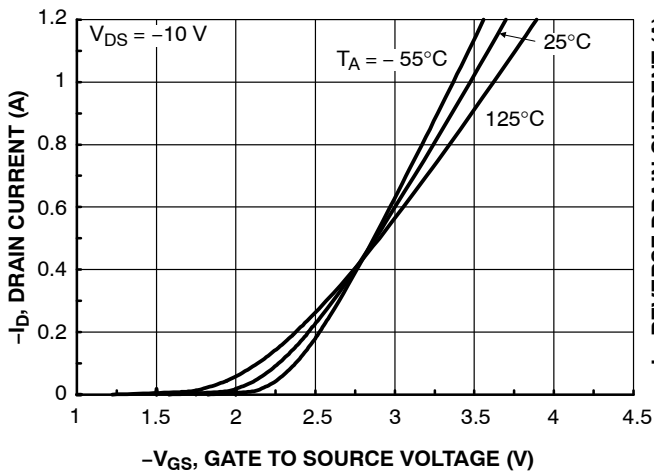


Figure 5. Transfer Characteristics

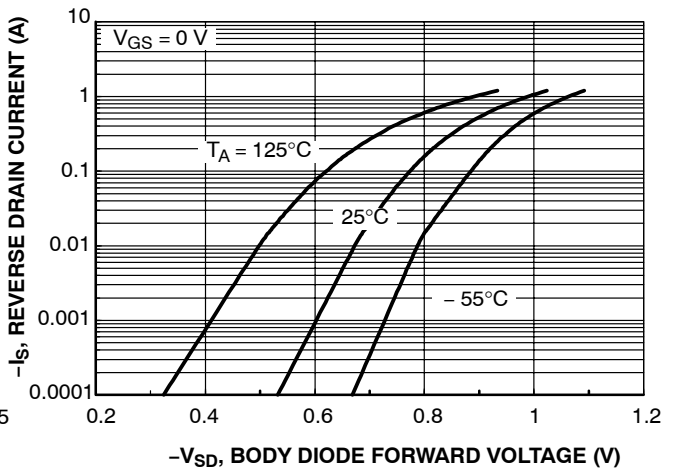


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

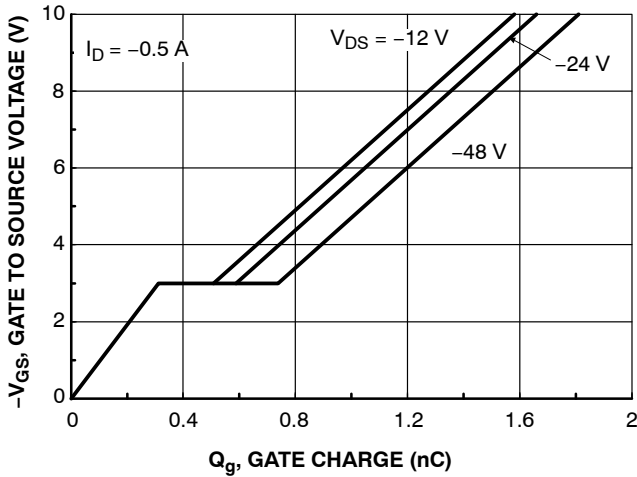


Figure 7. Gate Charge Characteristics

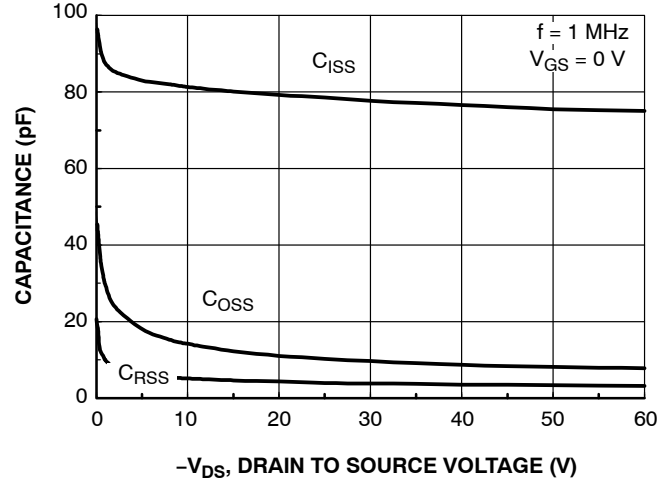


Figure 8. Capacitance Characteristics

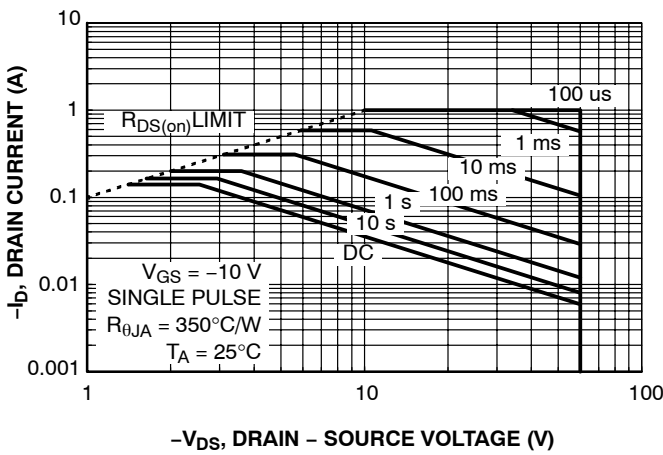


Figure 9. Maximum Safe Operating Area

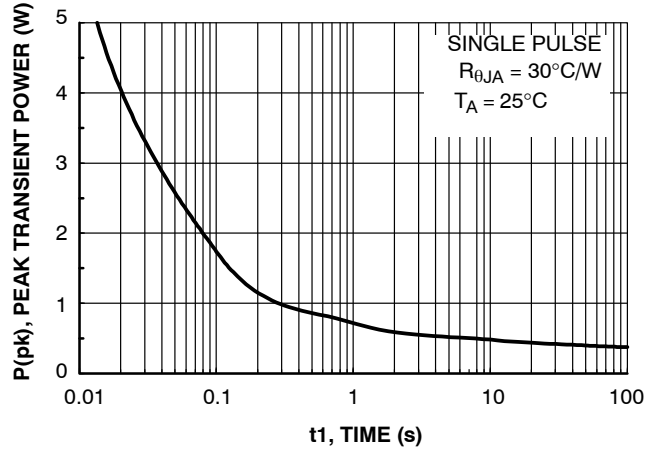


Figure 10. Single Pulse Maximum Power Dissipation

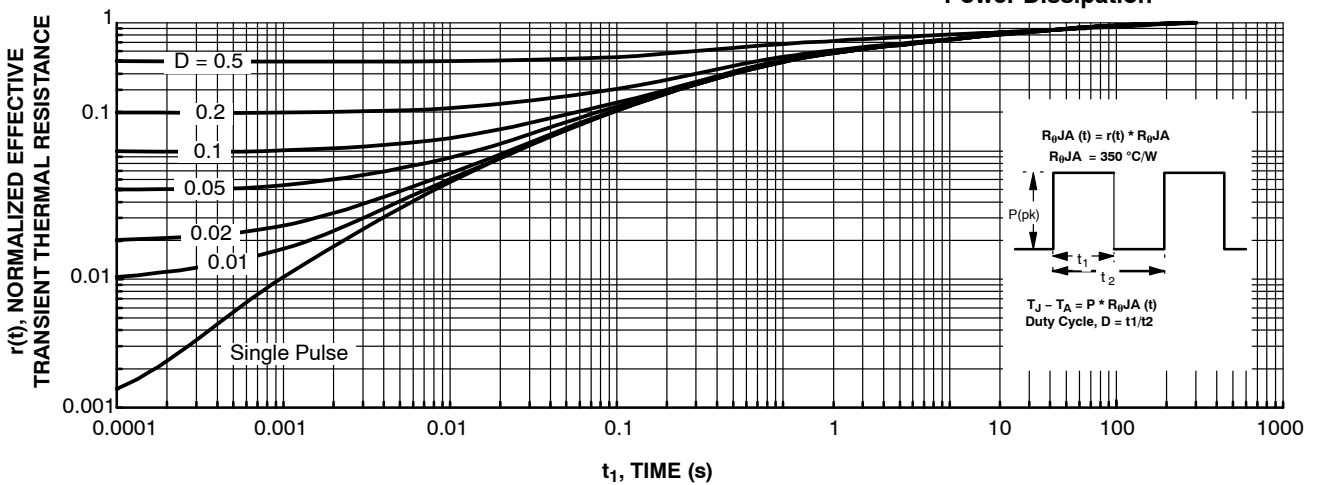


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

<b>DOCUMENT NUMBER:</b>	<b>98ASB42226B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOT-23 (TO-236)</b>	<b>PAGE 1 OF 2</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

- |   |   |   |   |   |   |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |   |   |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |   |   |   |   |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42226B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOT-23 (TO-236)</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)