

# NCV7329

## Stand-alone LIN Transceiver

### Description

The NCV7329 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU–state machine that recognizes and translates the instructions specific to that function.

The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

### Features

- LIN–Bus Transceiver
  - ◆ Compliant to ISO 17987–4 (Backwards Compatible to LIN Specification rev. 2.x, 1.3) and SAE J2602
  - ◆ Bus Voltage  $\pm 42$  V
  - ◆ Transmission Rate 1 kbps to 20 kbps
  - ◆ TxD Timeout Function
  - ◆ Integrated Slope Control
- Protection
  - ◆ Thermal Shutdown
  - ◆ Undervoltage Protection
  - ◆ Bus Pins Protected Against Transients in an Automotive Environment
- Modes
  - ◆ Normal Mode: LIN Transceiver Enabled, Communication via the Bus is Possible
  - ◆ Sleep Mode: LIN Transceiver Disabled, the Consumption from  $V_{BB}$  is Minimized
  - ◆ Standby Mode: Transition Mode Reached after Wake–up Event on the LIN Bus
- Compatibility
  - ◆ Pin–Compatible Subset with NCV7321
  - ◆ K–line Compatible

### Quality

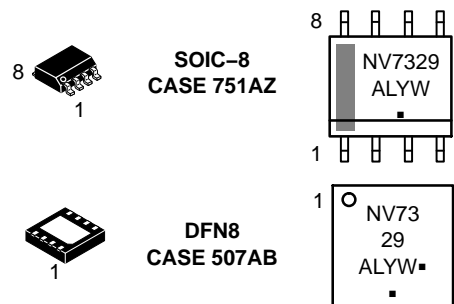
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



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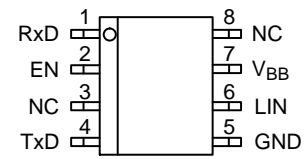
### MARKING DIAGRAMS



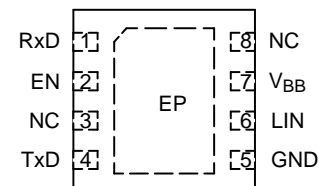
A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb–Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



SOIC–8 (Top View)



DFN8 (Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

# NCV7329

## BLOCK DIAGRAM

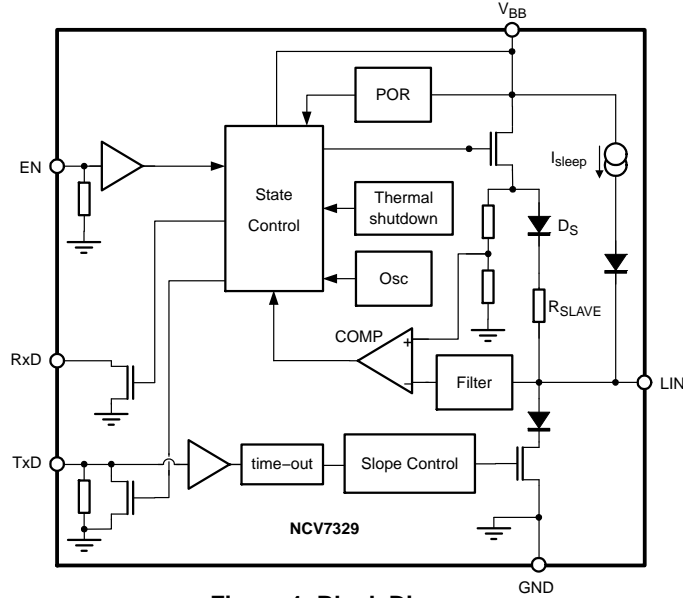


Figure 1. Block Diagram

## TYPICAL APPLICATION

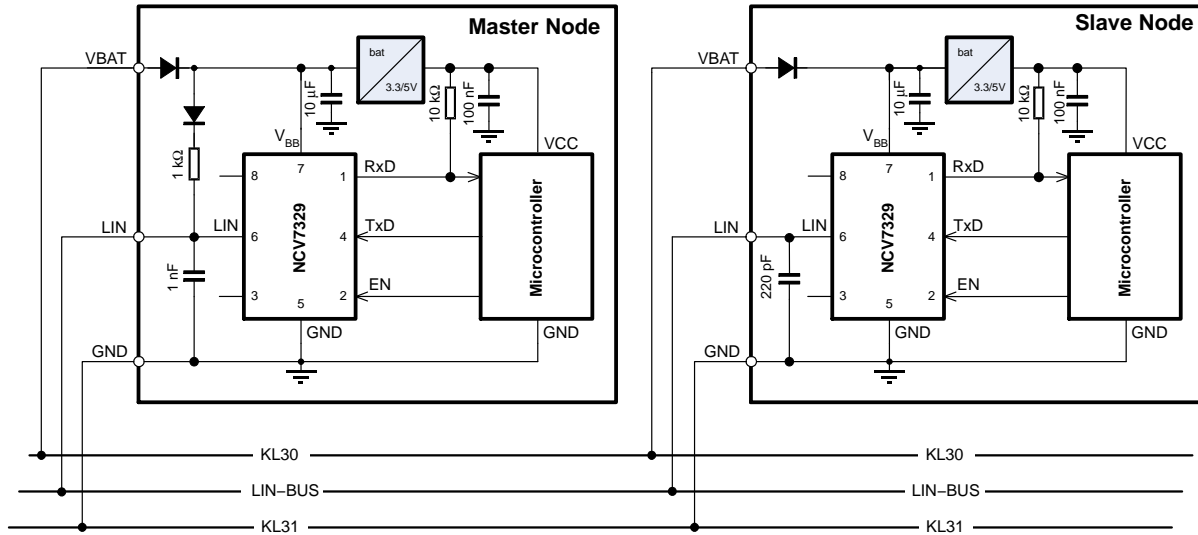


Figure 2. Typical Application Diagram for a Master Node

Table 1. PIN DESCRIPTION

Pin	Name	Description
1	RxD	Receive Data Output; Low in Dominant State; Open-Drain Output
2	EN	Enable Input, Transceiver in Normal Operation Mode when High, Pull-down Resistor to GND
3	NC	Not Connected
4	TxD	Transmit Data Input, Low for Dominant State, Pull-down to GND
5	GND	Ground
6	LIN	LIN Bus Output/Input
7	V <sub>BB</sub>	Battery Supply Input
8	NC	Not Connected
-	EP	Exposed Pad. Recommended to connect to GND or left floating in application (DFN8 package only).

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Min	Max	Unit
V <sub>BB</sub>	Voltage on Pin V <sub>BB</sub>	-0.3	+42	V
V <sub>LIN</sub>	LIN Bus Voltage with respect to GND	-42	+42	V
	LIN Bus Voltage with respect to V <sub>BB</sub>	-42	+42	V
V <sub>Dig_IO</sub>	DC Input Voltage on Pins (EN, RxD, TxD)	-0.3	+7	V
V <sub>ESD</sub>	Human Body Model (LIN Pin) (Note 1)	-8	+8	kV
	Human Body Model (All Pins) (Note 1)	-4	+4	kV
	Charged Device Model (All Pins) (Note 2)	-750	+750	V
	Machine Model (All Pins) (Note 3)	-200	+200	V
V <sub>ESDIEC</sub>	Electrostatic Discharge Voltage (LIN Pin) System Human Body Model (Note 4) Conform to IEC 61000-4-2	-8	+8	kV
T <sub>J</sub>	Junction Temperature Range	-40	+150	°C
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA-JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC-Q100-011.
3. In accordance to JEDEC JESD22-A115. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and 0.75 μH coil.
4. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test-house.

**Table 3. THERMAL CHARACTERISTICS**

Parameter	Symbol	Value	Unit
Thermal characteristics, SOIC-8 (Note 5)			
Thermal Resistance Junction-to-Air, Free air, 1S0P PCB (Note 6)	R <sub>θJA</sub>	131	°C/W
Thermal Resistance Junction-to-Air, Free air, 2S2P PCB (Note 7)	R <sub>θJA</sub>	81	°C/W
Thermal characteristics, DFN8 (Note 5)			
Thermal Resistance Junction-to-Air, Free air, 1S0P PCB (Note 6)	R <sub>θJA</sub>	125	°C/W
Thermal Resistance Junction-to-Air, Free air, 2S2P PCB (Note 7)	R <sub>θJA</sub>	58	°C/W

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. Values based on test board according to EIA/JEDEC Standard JESD51-3, signal layer with 10% trace coverage.
7. Values based on test board according to EIA/JEDEC Standard JESD51-7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (pin 5) unless otherwise specified. Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

**Table 4. DC CHARACTERISTICS** ( $V_{BB} = 5\text{ V to }18\text{ V}$ ;  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ ; Typical values are given at  $V_{BB} = 12\text{ V}$  and  $T_J = 25^\circ\text{C}$  Bus Load =  $500\ \Omega$  ( $V_{BB}$  to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>SUPPLY PIN (<math>V_{BB}</math>)</b>						
$V_{BB}$	Battery Supply		5		18	V
$I_{BB}$	Battery Supply Current	Normal Mode; LIN recessive	0.2	0.55	1.2	mA
$I_{BB}$	Battery Supply Current	Normal Mode; TxD = Low, LIN Dominant	2	3.9	6.5	mA
$I_{BB}$	Battery Supply Current	Sleep and Standby Mode; LIN recessive; $V_{LIN} = V_{BB}$ ; $T_J < 85^\circ\text{C}$		6	10	$\mu\text{A}$
$I_{BB}$	Battery Supply Current	Sleep and Standby Mode; LIN recessive; $V_{LIN} = V_{BB}$		6	15	$\mu\text{A}$
<b>POR AND <math>V_{BB}</math> MONITOR</b>						
PORH_ $V_{BB}$	Power-on Reset; High Level on $V_{BB}$	$V_{BB}$ Rising	2.7	3.5	4.4	V
PORL_ $V_{BB}$	Power-on Reset; Low Level on $V_{BB}$	$V_{BB}$ Falling	1.3	2.1	2.7	V
MONH_ $V_{BB}$	Battery Monitoring High Level	$V_{BB}$ Rising	3.2	4.2	5.0	V
MONL_ $V_{BB}$	Battery Monitoring Low Level	$V_{BB}$ Falling	3.0	4.0	4.8	V
<b>TRANSMITTER DATA INPUT (PIN TxD)</b>						
$V_{IL\_TxD}$	Low Level Input Voltage		-0.3		+0.8	V
$V_{IH\_TxD}$	High Level Input Voltage		2		7	V
$R_{PD\_TxD}$	Pull-down Resistor on TxD Pin		50	125	325	k $\Omega$
<b>RECEIVER DATA OUTPUT (PIN RxD)</b>						
$I_{OL\_RxD}$	Low Level Output Current	$V_{RxD} = 0.4\text{ V}$	2			mA
$I_{OH\_RxD}$	High Level Output Current		-5		+5	$\mu\text{A}$
<b>ENABLE INPUT (PIN EN)</b>						
$V_{IL\_EN}$	Low Level Input Voltage		-0.3		+0.8	V
$V_{IH\_EN}$	High Level Input Voltage		2		7	V
$R_{PD\_EN}$	Pull-down Resistor to Ground		100	250	650	k $\Omega$
<b>LIN BUS LINE (PIN LIN)</b>						
$V_{BUS\_DOM}$	Bus Voltage for Dominant State				0.4	$V_{BB}$
$V_{BUS\_REC}$	Bus Voltage for Recessive State		0.6			$V_{BB}$
$V_{REC\_DOM}$	Receiver Threshold	LIN Bus Recessive – Dominant	0.4		0.6	$V_{BB}$
$V_{REC\_REC}$	Receiver Threshold	LIN Bus Dominant – Recessive	0.4		0.6	$V_{BB}$
$V_{REC\_CNT}$	Receiver Centre Voltage	$(V_{REC\_DOM} + V_{REC\_REC}) / 2$	0.475	0.500	0.525	$V_{BB}$
$V_{REC\_HYS}$	Receiver Hysteresis	$(V_{REC\_REC} - V_{REC\_DOM})$	0.050		0.175	$V_{BB}$
$V_{LIN\_DOM}$	Dominant Output Voltage	Normal mode; $V_{BB} = 7\text{ V}$			1.2	V
		Normal mode; $V_{BB} = 18\text{ V}$			2.0	V
$I_{BUS\_no\_GND}$	Communication not Affected	$V_{BB} = GND = 12\text{ V}$ ; $0 < V_{LIN} < 18\text{ V}$	-1		+1	mA
$I_{BUS\_no\_VBB}$	LIN Bus Remains Operational	$V_{BB} = GND = 0\text{ V}$ ; $0 < V_{LIN} < 18\text{ V}$			5	$\mu\text{A}$

8. Values based on design and characterization. Not tested in production.

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**Table 4. DC CHARACTERISTICS** ( $V_{BB} = 5\text{ V to }18\text{ V}$ ;  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ ; Typical values are given at  $V_{BB} = 12\text{ V}$  and  $T_J = 25^\circ\text{C}$   
Bus Load =  $500\ \Omega$  ( $V_{BB}$  to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>LIN BUS LINE (PIN LIN)</b>						
$I_{BUS\_LIM}$	Current limitation for Driver	Dominant State; $V_{LIN} = V_{BB\_MAX}$	40		200	mA
$I_{BUS\_PAS\_dom}$	Receiver Leakage current; Driver OFF	TxD = High; $V_{LIN} = 0\text{ V}$ ; $V_{BB} = 12\text{ V}$	-1			mA
$I_{sleep}$	Receiver Leakage current; see Figure 1	Sleep mode; $V_{LIN} = 0\text{ V}$ ; $V_{BB} = 12\text{ V}$	-16	-8	-3	$\mu\text{A}$
$I_{BUS\_PAS\_rec}$	Receiver Leakage current; Driver OFF; (Note 8)	TxD = High; $8\text{ V} < V_{BB} < 18\text{ V}$ ; $8\text{ V} < V_{LIN} < 18\text{ V}$ ; $V_{LIN} \geq V_{BB}$			20	$\mu\text{A}$
$V_{SERDiode}$	Voltage Drop on Serial Diode	Voltage drop on $D_S$ , see Figure 1	0.4	0.7	1	V
$R_{SLAVE}$	Internal Pull-up Resistance	see Figure 1	20	30	60	$\text{k}\Omega$
$C_{LIN}$	Capacitance on Pin LIN, (Note 8)			20	30	pF

8. Values based on design and characterization. Not tested in production.

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**Table 5. AC CHARACTERISTICS** ( $V_{BB} = 5\text{ V to }18\text{ V}$ ;  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ ; unless otherwise specified. For the transmitter parameters, the following bus loads are considered:  $L1 = 1\text{ k}\Omega / 1\text{ nF}$ ;  $L2 = 660\ \Omega / 6.8\text{ nF}$ ;  $L3 = 500\ \Omega / 10\text{ nF}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>LIN TRANSCEIVER</b>						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)} / (2xt_{BIT})$ (See Figure 4)	$TH_{REC(max)} = 0.744 \times V_{BB}$ $TH_{DOM(max)} = 0.581 \times V_{BB}$ $t_{BIT} = 50\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$	0.396		0.500	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)} / (2xt_{BIT})$ (See Figure 4)	$TH_{REC(min)} = 0.422 \times V_{BB}$ $TH_{DOM(min)} = 0.284 \times V_{BB}$ $t_{BIT} = 50\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$	0.500		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)} / (2xt_{BIT})$ (See Figure 4)	$TH_{REC(max)} = 0.778 \times V_{BB}$ $TH_{DOM(max)} = 0.616 \times V_{BB}$ $t_{BIT} = 96\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$	0.417		0.500	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)} / (2xt_{BIT})$ (See Figure 4)	$TH_{REC(min)} = 0.389 \times V_{BB}$ $TH_{DOM(min)} = 0.251 \times V_{BB}$ $t_{BIT} = 96\ \mu\text{s}$ $V_{BB} = 5\text{ V to }18\text{ V}$	0.500		0.590	
$t_{TX\_PROP\_DOWN}$	Propagation Delay of TxD to LIN. TxD High to Low (See Figure 7)				14	$\mu\text{s}$
$t_{TX\_PROP\_UP}$	Propagation Delay of TxD to LIN. TxD Low to High (See Figure 7)				14	$\mu\text{s}$
<b>LIN RECEIVER</b>						
$t_{RX\_PD}$	Propagation Delay of Receiver, Rising and falling Edge (See Figure 5)	$R_{RXD} = 2.4\text{ k}\Omega$ ; $C_{RXD} = 20\text{ pF}$	0.1		6	$\mu\text{s}$
$t_{RX\_SYM}$	Propagation Delay Symmetry	$R_{RXD} = 2.4\text{ k}\Omega$ ; $C_{RXD} = 20\text{ pF}$ ; Rising edge with respect to falling edge	-2		+2	$\mu\text{s}$
<b>MODE TRANSITIONS AND TIMEOUTS</b>						
$t_{LIN\_WAKE}$	Duration of LIN Dominant for Detection of Wake-up via LIN Bus (See Figure 6)	Sleep Mode	40	70	150	$\mu\text{s}$
$t_{TXD\_TIMEOUT}$	TxD Dominant Timeout	Normal Mode, TxD = Low	14	25	46	ms
$t_{INIT\_NORM}$	Time From Rising Edge of EN pin to the moment when the transmitter is able to correctly transmit		15	30	75	$\mu\text{s}$
$t_{ENABLE}$	Duration of EN pin in High Level State for transition to Normal Mode		11	20	55	$\mu\text{s}$
$t_{DISABLE}$	Duration of EN pin in Low Level State for transition to Sleep Mode		11	20	55	$\mu\text{s}$
$t_{TO\_STB}$	Delay from LIN Bus Dominant to Recessive Edge to Entering of Standby Mode after Valid LIN Wake-up (See Figure 6)	Sleep Mode	5	10	40	$\mu\text{s}$
<b>THERMAL SHUTDOWN</b>						
$T_{J(sd)}$	Shutdown Junction Temperature	Temperature Rising	160	180	200	$^\circ\text{C}$

9. Values based on design and characterization. Not tested in production.

FUNCTIONAL DESCRIPTION

**Overall Functional Description**

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications.

The NCV7329 contains the LIN transmitter, LIN receiver, power-on-reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for a maximum specified transmission speed of 20 kbps.

**Table 6. OPERATING MODES**

Pin EN	Mode	Pin RxD	LIN bus
x	Unpowered	Floating	OFF; Floating
Low	Sleep	Floating	OFF; Floating
Low	Standby	Low indicates wake-up	OFF; 30 kΩ
High	Normal	LOW: dominant HIGH: recessive	ON; 30 kΩ

**Unpowered Mode**

As long as V<sub>BB</sub> remains below its power-on-reset level, the chip is kept in a safe unpowered state. The LIN transmitter is inactive, the LIN pin is left floating and only a weak pull-down is connected on pin TxD. Pin RxD remains floating.

The unpowered state will be entered from any other state when V<sub>BB</sub> falls below its power-on-reset level (PORL\_V<sub>BB</sub>). When V<sub>BB</sub> rises above the power-on-reset high threshold (PORH\_V<sub>BB</sub>), the NCV7329 switches to a Sleep mode.

**Normal Mode**

In the Normal mode, the full functionality of the LIN transceiver is available. The transceiver can transmit and receive data via the LIN bus with speed up to 20 kbps. Data according the state of TxD input are sent to the LIN bus while pin RxD reflects the logical symbol received on the LIN bus – high-impedant for recessive and Low for dominant. A 30 kΩ resistor in series with a reverse-protection diode is internally connected between LIN and V<sub>BB</sub> pins.

The signal on pin TxD passes through a timer, which releases the bus in case the TxD remains low for longer than t<sub>TxD\_TIMEOUT</sub>. It prevents the LIN bus being permanently driven dominant and thus blocking all subsequent communication due to a failure of the application (e.g. software error). The transmission can continue once the TxD returns to High logical level.

In case the junction temperature increases above the thermal shutdown threshold (T<sub>J(sd)</sub>), e.g. due to a short of the LIN wiring to the battery, the transmitter is disabled and releases the LIN bus to recessive. Once the junction temperature decreases back below the thermal shutdown level, the transmission can be enabled again. However, to avoid thermal oscillations, first a High logical level on TxD must be encountered before the transmitter is enabled.

As required by SAE J2602, the transceiver must behave safely below its operating range – it shall either continue to transmit correctly (according its specification) or remain silent (transmit a recessive state regardless of the TxD signal). A battery monitoring circuit in NCV7329 deactivates the transmitter in the Normal mode if the V<sub>BB</sub> level drops below MONL\_V<sub>BB</sub>. Transmission is enabled again when V<sub>BB</sub> reaches MONH\_V<sub>BB</sub>. The internal logic remains in the normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power-on-reset levels are overlapping, it's ensured by the implementation that the monitoring level never falls below the power-on-reset level.

The Normal mode can be entered from either Standby or Sleep mode when EN Pin is High for longer than t<sub>ENABLE</sub>. When the transition is made from Standby mode, TxD pull-down is set to weak and RxD is put into a high-impedance immediately after EN becomes High (before the expiration of t<sub>ENABLE</sub> filtering time). This excludes signal conflicts between the Standby mode pin settings and the signals required to control the chip in the Normal mode after a local wake-up vs. High logical level on TxD required to send a recessive symbol to the LIN bus.

**Sleep Mode**

Sleep mode provides extremely low current consumption. The LIN transceiver is inactive and the battery consumption is minimized.

This mode is entered in one of the following ways:

- After the voltage level at V<sub>BB</sub> pin rises above its power-on-reset level (PORH\_V<sub>BB</sub>). In this case, RxD Pin remains high-impedant and the pull-down applied on pin TxD remains weak.
- After assigning Low logical level to pin EN for longer than t<sub>DISABLE</sub> while NCV7329 is in the Normal mode.

**Standby Mode**

Standby mode is entered from the Sleep mode when a remote wake-up event occurred. The Low level on RxD pin indicates interrupt flag for the microcontroller.

# NCV7329

## OPERATING STATES

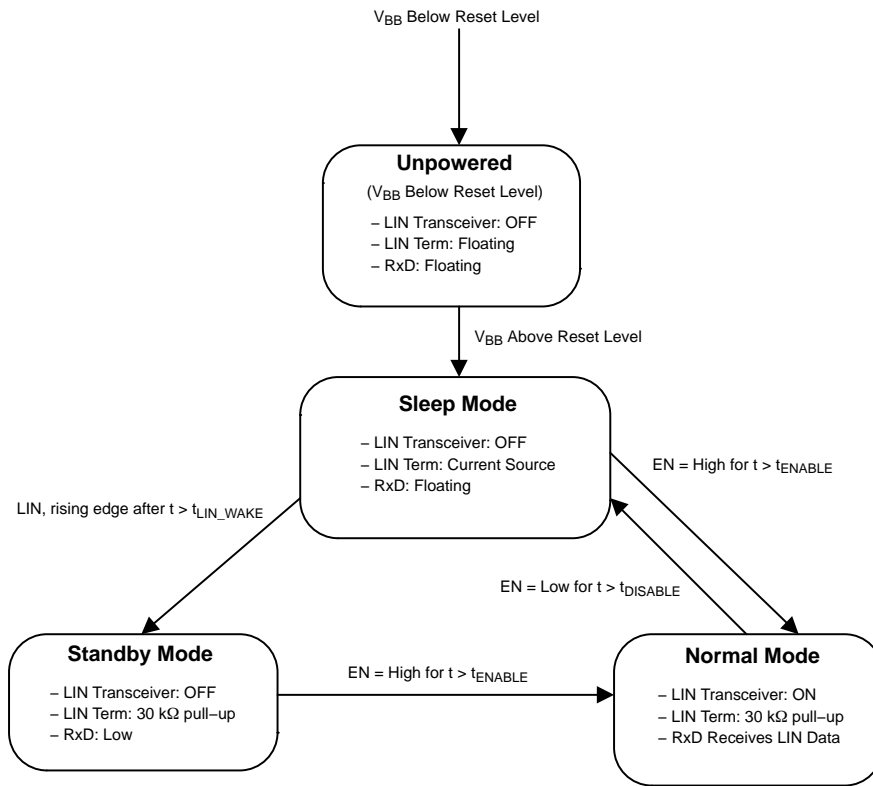


Figure 3. State Diagram



MEASUREMENT SETUPS AND DEFINITIONS

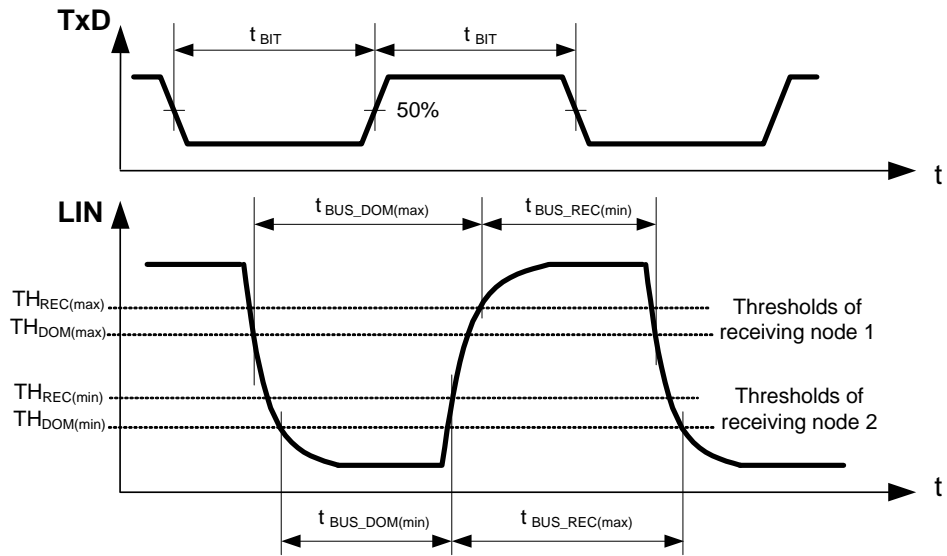


Figure 4. LIN Transmitter Duty Cycle

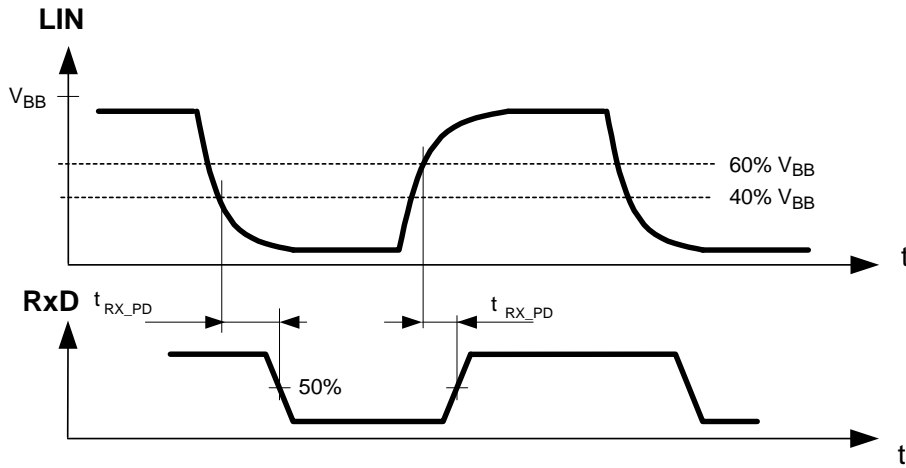


Figure 5. LIN Receiver Timing

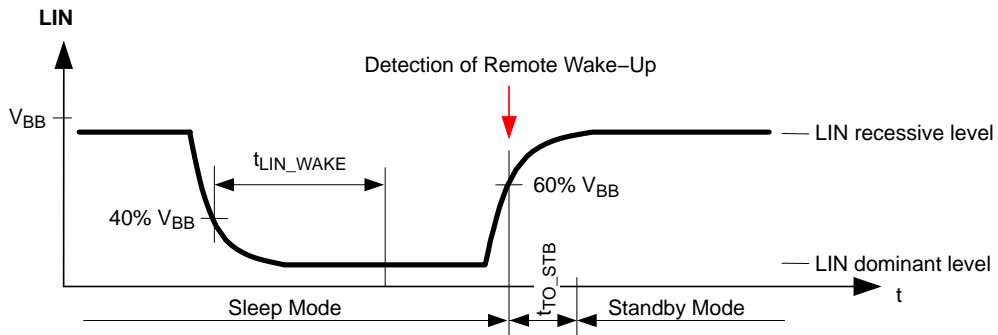


Figure 6. Remote (LIN) Wake-up Detection

# NCV7329

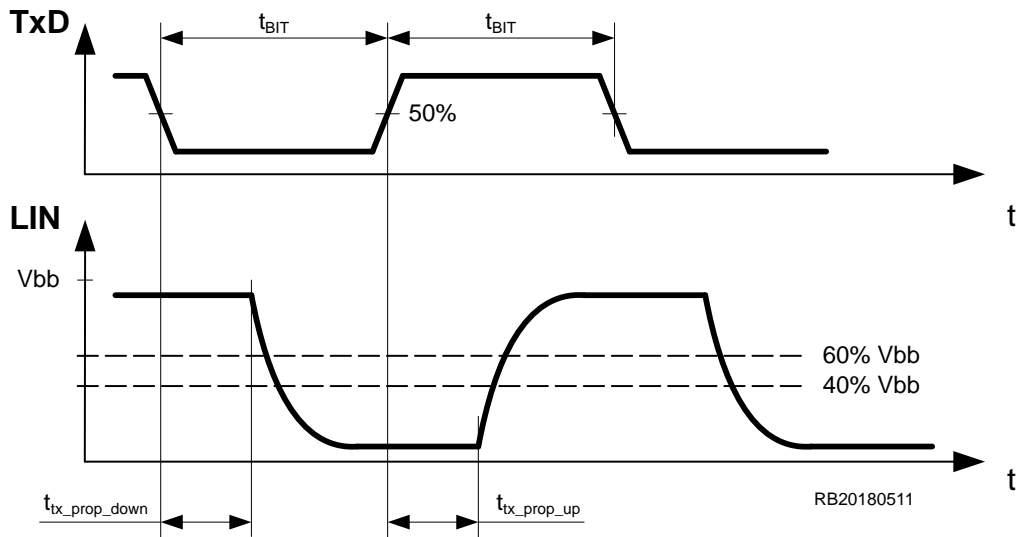


Figure 7. LIN Transmitter Timing

## DEVICE ORDERING INFORMATION

Part Number	Description	Temperature Range	Package	Shipping <sup>†</sup>
NCV7329D10R2G	Stand-alone LIN Transceiver	-40°C to +125°C	SOIC-8 (Pb-Free)	3000 / Tape & Reel
NCV7329MW0R2G	Stand-alone LIN Transceiver	-40°C to +125°C	DFN8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

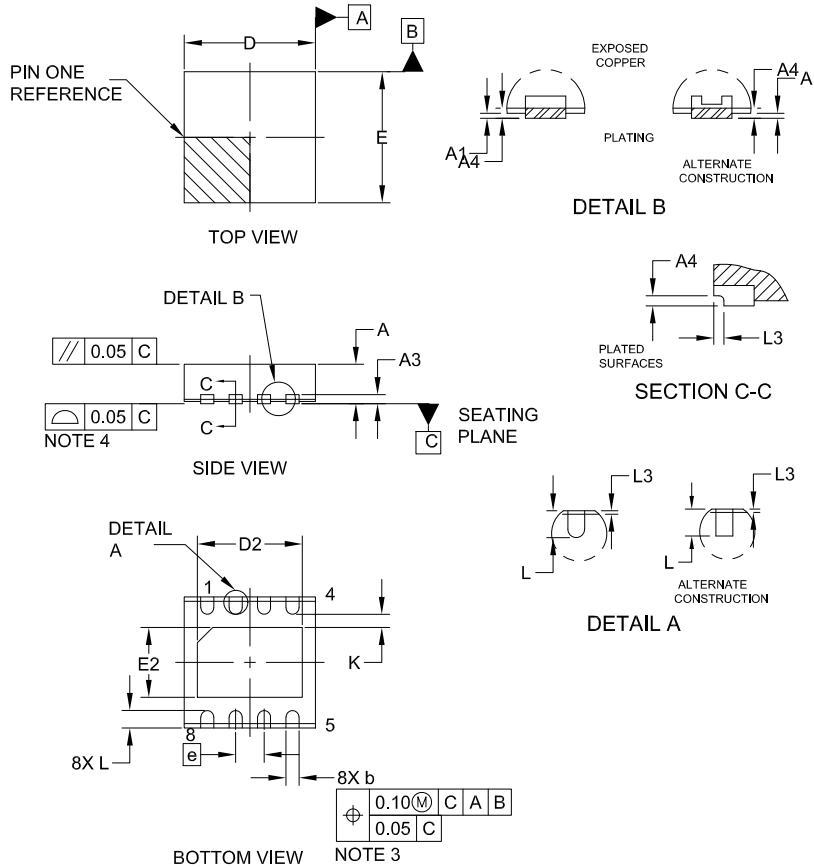
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SCALE 2:1

## DFNW8 3x3, 0.65P CASE 507AB ISSUE E

DATE 02 JUL 2021

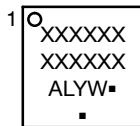


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	—	—	0.05
A3	0.20 REF		
A4	0.10	—	—
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
e	0.65 BSC		
K	0.30 REF		
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

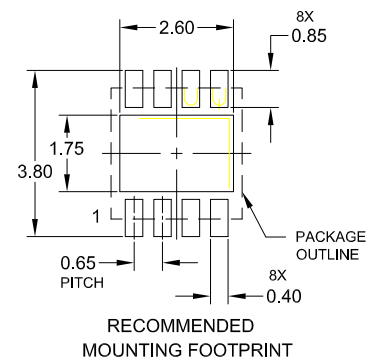
### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



<b>DOCUMENT NUMBER:</b>	<b>98AON14978G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DFNW8 3x3, 0.65P</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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