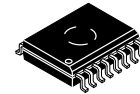


# Isolated High Current IGBT Gate Driver

## NCV57001F



1  
SOIC-16 WB  
CASE 751G-03

NCV57001F is a variant of NCV57001 with reduced Soft-Turn-Off time suited to drive large IGBTs or power modules. NCV57001F is a high-current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, and soft turn-off at DESAT. NCV57001F accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCV57001F provides >5 kVrms (UL1577 rating) galvanic isolation and >1200 V<sub>IORM</sub> (working voltage) capabilities. NCV57001F is available in the wide-body SOIC-16 package with guaranteed 8 mm creepage distance between input and output to fulfill reinforced safety insulation requirements.

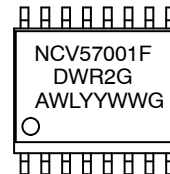
### Features

- High Current Output (+4/-6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- Active Miller Clamp to Prevent Spurious Gate Turn-on
- DESAT Protection with Programmable Delay
- Typ 550 ns Soft Turn Off during IGBT Short Circuit
- IGBT Gate Clamping during Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2
- 3.3 V to 5 V Input Supply Voltage
- 5000 V Galvanic Isolation (to meet UL1577 requirements)
- 1200 V Working Voltage (per VDE0884-10 requirements)
- High transient immunity
- High electromagnetic immunity
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Typical Applications

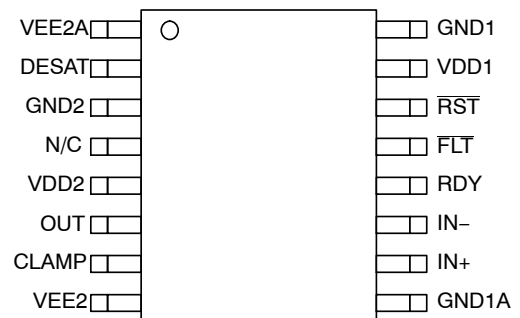
- Automotive Power Supplies
- HEV/EV Powertrain
- BSG Inverter
- PTC Heater

### MARKING DIAGRAM



NCV57001FDWR2G	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

# NCV57001F

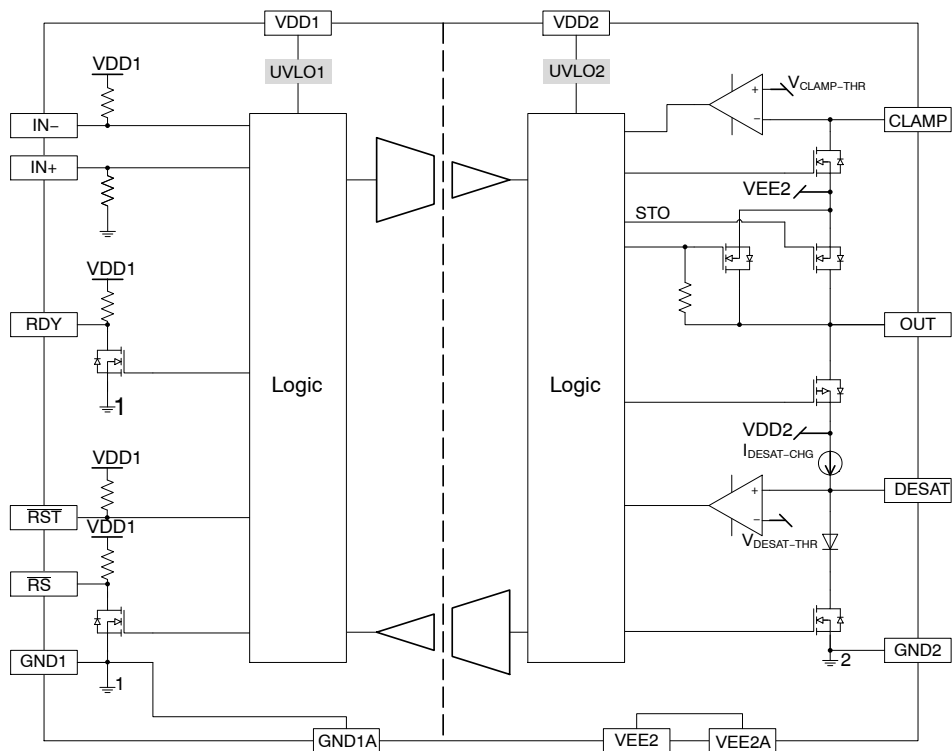


Figure 1. Simplified Block Diagram

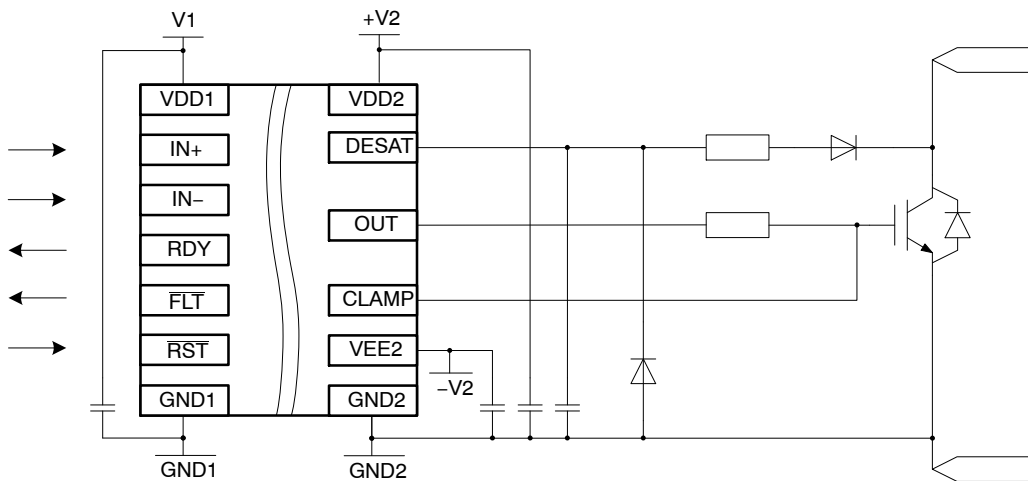


Figure 2. Simplified Application Schematics

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**Table 1. PIN FUNCTION DESCRIPTION**

Pin Name	No.	I/O	Description
V <sub>EE2A</sub>	1	Power	Output side negative power supply. A good quality bypassing capacitor is required from these pins to GND2 and should be placed close to the pins for best results. Connect it to GND2 for unipolar supply application.
V <sub>EE2</sub>	8		
DESAT	2	I/O	<p>Input for detecting the desaturation of IGBT due to a short circuit condition. An internal constant current source I<sub>DESAT-CHG</sub> charging an external capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering. When the DESAT voltage goes up and reaches V<sub>DESAT-THR</sub>, the output is driven low. Further, the <math>\overline{\text{FLT}}</math> output is activated, please refer to Figure 5.</p> <p>A 5 <math>\mu\text{s}</math> mute time apply to IN+ and IN- once DESAT occurs.</p>
GND2	3	Power	Output side gate drive reference connecting to IGBT emitter or FET source.
N/C	4	--	Not connected.
V <sub>DD2</sub>	5	Power	Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.
OUT	6	O	Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. OUT is actively pulled low during start-up and under Fault conditions.
CLAMP	7	I/O	Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn-on. Its internal N FET is turned on when the voltage of this pin falls below V <sub>EE2</sub> + V <sub>CLAMP-THR</sub> . It is to be tied directly to IGBT/FET gate with minimum trace length for best results.
GND1	9	Power	Input side ground reference.
	16		
IN+	10	I	Non inverted gate driver input. It is internally clamped to V <sub>DD1</sub> and has a pull-down resistor of 50 k $\Omega$ to ensure that output is low in the absence of an input signal. A minimum positive going pulse-width is required at IN+ before OUT responds.
IN-	11	I	Inverted gate driver input. It is internally clamped to V <sub>DD1</sub> and has a pull-up resistor of 50 k $\Omega$ to ensure that output is low in the absence of an input signal. A minimum negative going pulse-width is required at IN- before OUT responds.
RDY	12	O	<p>Power good indication output, active high when V<sub>DD2</sub> is good. There is an internal 50 k<math>\Omega</math> pull-up resistor connected to this pin. Multiple of them from different drivers can be "OR"ed together.</p> <p>If a low RDY event is triggered by UVLO2, the maximum low duration for RDY is 200 ns.</p> <p>OUT remains low when RDY is low. Short time delay may apply. See Figure 4 for details.</p>
$\overline{\text{FLT}}$	13	O	Fault output (active low) that allows communication to the main controller that the driver has encountered a desaturation condition and has deactivated the output.
RST	14	I	Reset input with an internal 50 k $\Omega$ pull-up resistor, active low to reset fault latch.
V <sub>DD1</sub>	15	Power	Input side power supply (3.3 V to 5 V).

**Table 2. SAFETY AND INSULATION RATINGS**

Symbol	Parameter	Min	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V <sub>RMS</sub>	I – IV
		< 300 V <sub>RMS</sub>	I – IV
		< 450 V <sub>RMS</sub>	I – IV
		< 600 V <sub>RMS</sub>	I – IV
		< 1000 V <sub>RMS</sub>	I – III
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)	600	
	Climatic Classification	40/100/21	
	Polution Degree (DIN VDE 0110/1.89)	2	
V <sub>PR</sub>	Input-to-Output Test Voltage, Method b, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 s, Partial Discharge < 5 pC	2250	V <sub>pk</sub>
	Input-to-Output Test Voltage, Method a, V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 10 s, Partial Discharge < 5 pC	-	V <sub>pk</sub>
V <sub>IORM</sub>	Maximum Repetitive Peak Voltage	1200	V <sub>pk</sub>
V <sub>IOWM</sub>	Maximum Working Insulation Voltage	870	V <sub>RMS</sub>
V <sub>IOTM</sub>	Highest Allowable Over Voltage	8400	V <sub>pk</sub>
E <sub>CR</sub>	External Creepage	8.0	mm
E <sub>CL</sub>	External Clearance	8.0	mm
DTI	Insulation Thickness	17.3	um
T <sub>Case</sub>	Safety Limit Values – Maximum Values in Failure; Case Temperature	150	°C
P <sub>S,INPUT</sub>	Safety Limit Values – Maximum Values in Failure; Input Power	36	mW
P <sub>S,OUTPUT</sub>	Safety Limit Values – Maximum Values in Failure; Output Power	1364	mW
R <sub>IO</sub>	Insulation Resistance at TS, V <sub>IO</sub> = 500 V	10 <sup>9</sup>	Ω

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**Table 3. ABSOLUTE MAXIMUM RATINGS** (Note 1) Over operating free-air temperature range unless otherwise noted

Symbol	Parameter	Minimum	Maximum	Unit
V <sub>DD1</sub> -GND1	Supply voltage, input side	-0.3	6	V
V <sub>DD2</sub> -GND2	Positive Power Supply, output side	-0.3	25	V
V <sub>EE2</sub> -GND2	Negative Power Supply, output side	-10	0.3	V
V <sub>DD2</sub> -V <sub>EE2</sub> (V <sub>MAX2</sub> )	Differential Power Supply, output side	0	25	V
V <sub>OUT</sub>	Gate-driver output voltage	V <sub>EE2</sub> - 0.3	V <sub>DD2</sub> + 0.3	V
I <sub>PK-SRC</sub>	Gate-driver output sourcing current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V <sub>MAX2</sub> = 20 V)		7.8	A
I <sub>PK-SNK</sub>	Gate-driver output sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V <sub>MAX2</sub> = 20 V)		7.1	A
I <sub>PK-CLAMP</sub>	Clamp sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V <sub>CLAMP</sub> = 3 V)		2.5	A
t <sub>CLP</sub>	Maximum Short Circuit Clamping Time (I <sub>OUT_CLAMP</sub> = 500 mA)		10	μs
V <sub>LIM</sub> -GND1	Voltage at IN+, IN-, RST, FLT, RDY	-0.3	V <sub>DD1</sub> + 0.3	V
I <sub>LIM</sub> -GND1	Output current of FLT, RDY		10	mA
V <sub>DESAT</sub> -GND2	Desat Voltage	-0.3	V <sub>DD2</sub> + 0.3	V
V <sub>CLAMP</sub> -GND2	Clamp Voltage	V <sub>EE2</sub> - 0.3	V <sub>DD2</sub> + 0.3	V
PD	Power Dissipation SOIC-16 wide package			mW
T <sub>J(max)</sub>	Maximum Junction Temperature	-40	150	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
ESDHBM	ESD Capability, Human Body Model (Note 2)		±2	kV
ESDCDM	ESD Capability, Charged Device Model (Note 2)		±2	kV
MSL	Moisture Sensitivity Level		1	-
T <sub>SLD</sub>	Lead Temperature Soldering Reflow, Pb-Free Versions (Note 3)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114).  
ESD Charged Device Model tested per AEC-Q100-011 (EIA/JESD22-C101).  
Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 25°C.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**Table 4. THERMAL CHARACTERISTICS**

Symbol	Parameter	Conditions	Value	Unit
R <sub>JA</sub>	Thermal Resistance, Junction-to-Air	100 mm <sup>2</sup> , 1 oz Copper, 1 Surface Layer	114	°C/W
		650 mm <sup>2</sup> , 1 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers	62	

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm<sup>2</sup> (or 0.16 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate.

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**Table 5. OPERATING RANGES** (Note 6)

Symbol	Parameter	Min	Max	Unit
V <sub>DD1-GND1</sub>	Supply voltage, input side	UVLO1	5.5	V
V <sub>DD2-GND2</sub>	Positive Power Supply, output side	UVLO2	24	V
V <sub>EE2-GND2</sub>	Negative Power Supply, output side	-10	0	V
V <sub>DD2-V<sub>EE2</sub></sub> (V <sub>MAX2</sub> )	Differential Power Supply, output side	0	24	V
V <sub>IL</sub>	Low level input voltage at IN+, IN-, $\overline{RST}$	0	0.3 × V <sub>DD1</sub>	V
V <sub>IH</sub>	High level input voltage at IN+, IN-, $\overline{RST}$	0.7 × V <sub>DD1</sub>	V <sub>DD1</sub>	V
dV <sub>ISO</sub> /dt	Common Mode Transient Immunity (1500 V)	100		kV/μs
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

## ISOLATION CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>ISO, input-output</sub>	Input-Output Isolation Voltage	T <sub>A</sub> = 25°C, Relative Humidity < 50%, t = 1.0 minute, I <sub>L-O</sub> 10 A, 50 Hz (See Note 7, 8, 9)	5000	-	-	V <sub>RMS</sub>
R <sub>ISO</sub>	Isolation Resistance	V <sub>L-O</sub> = 500 V (See Note 7)	-	10 <sup>11</sup>	-	Ω

7. Device is considered a two-terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together

8. 5,000 V<sub>RMS</sub> for 1-minute duration is equivalent to 6,000 V<sub>RMS</sub> for 1-second duration.

9. The input-output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input-output continuous voltage rating. For the continuous working voltage rating, refer to equipment-level safety specification or DIN VDE V 0884-11 Safety and Insulation Ratings Table

**Table 6. ELECTRICAL CHARACTERISTICS** (V<sub>DD1</sub> = 5 V, V<sub>DD2</sub> = 15 V, V<sub>EE2</sub> = -8 V.)

For typical values T<sub>A</sub> = 25°C, for min/max values, T<sub>A</sub> is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### VOLTAGE SUPPLY

V <sub>UVLO1-OUT-ON</sub>	UVLO1 Output Enabled				3.0	V
V <sub>UVLO1-OUT-OFF</sub>	UVLO1 Output Disabled		2.4			V
V <sub>UVLO1-HYST</sub>	UVLO1 Hysteresis		0.125			V
V <sub>UVLO2-OUT-ON</sub>	UVLO2 Output Enabled		13.2	13.5	13.8	V
V <sub>UVLO2-OUT-OFF</sub>	UVLO2 Output Disabled		12.2	12.5	12.8	V
V <sub>UVLO2-HYST</sub>	UVLO2 Hysteresis			1		V
I <sub>DD1-0</sub>	Input Supply Quiescent Current Output Low	IN+ = Low, IN- = Low		1	2	mA
		RDY = High, $\overline{FLT}$ = High				
I <sub>DD1-100</sub>	Input Supply Quiescent Current Output High	IN+ = High, IN- = Low		4.8	6	mA
		RDY = High, $\overline{FLT}$ = High				
I <sub>DD2-0</sub>	Output Positive Supply Quiescent Current, Output Low	IN+ = Low, IN- = Low		3.3	4	mA
		RDY = High, $\overline{FLT}$ = High, no load				
I <sub>DD2-100</sub>	Output Positive Supply Quiescent Current, Output High	IN+ = High, IN- = Low		4	5	mA
		RDY = High, $\overline{FLT}$ = High, no load				
I <sub>EE2-0</sub>	Output Negative Supply Quiescent Current, Output Low	IN+ = High, IN- = Low, no load		0.4	2	mA
I <sub>EE2-100</sub>	Output Negative Supply Quiescent Current, Output High	IN+ = High, IN- = Low, no load		0.2	2	mA

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**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 15\text{ V}$ ,  $V_{EE2} = -8\text{ V}$ ) (continued)

For typical values  $T_A = 25^\circ\text{C}$ , for min/max values,  $T_A$  is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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**LOGIC INPUT AND OUTPUT**

$V_{IL}$	IN+, IN-, RST Low Input Voltage				$0.3 \times V_{DD1}$	V
$V_{IH}$	IN+, IN-, RST High Input Voltage		$0.7 \times V_{DD1}$			V
$V_{IN-HYST}$	Input Hysteresis Voltage			$0.15 \times V_{DD1}$		V
$I_{IN-L}, I_{RST-L}$	IN-, RST Input current (50 k $\Omega$ pull-up resistor)	$V_{IN-}/V_{RST} = 0\text{ V}$		-100		$\mu\text{A}$
$I_{IN+H}$	IN+ Input Current (50 k $\Omega$ pull-down resistor)	$V_{IN+} = 5\text{ V}$		100		$\mu\text{A}$
$I_{RDY-L}, I_{FLT-L}$	RDY, FLT Pull-up Current (50 k $\Omega$ pull-up resistor)	$V_{RDY}/V_{FLT} = \text{Low}$		100		$\mu\text{A}$
$V_{RDY-L}, V_{FLT-L}$	RDY, FLT Low Level Output Voltage	$I_{RDY}/I_{FLT} = 5\text{ mA}$			0.3	V
$t_{ON-MIN1}$	Input Pulse Width of IN+, IN- for No Response at Output				10	ns
$t_{ON-MIN2}$	Input Pulse Width of IN+, IN- for Guaranteed Response at Output		30			ns
$t_{RST-MIN}$	Pulse Width of RST for Resetting FLT		800			ns

**DRIVER OUTPUT**

$V_{OUTL1}$	Output Low State ( $V_{OUT} - V_{EE2}$ )	$I_{SINK} = 200\text{ mA}$		0.1	0.2	V
$V_{OUTL3}$		$I_{SINK} = 1.0\text{ A}, T_A = 25^\circ\text{C}$		0.5	0.8	
$V_{OUTH1}$	Output High State ( $V_{DD2} - V_{OUT}$ )	$I_{SRC} = 200\text{ mA}$		0.3	0.5	V
$V_{OUTH3}$		$I_{SRC} = 1.0\text{ A}, T_A = 25^\circ\text{C}$		0.8	1	
$I_{PK-SNK1}$	Peak Driver Current, Sink (Note 10)	$V_{OUT} = 7.9\text{ V}$		7.1		A
$I_{PK-SRC1}$	Peak Driver Current, Source (Note 10)	$V_{OUT} = -5\text{ V}$		7.8		A

**MILLER CLAMP**

$V_{CLAMP}$	Clamp Voltage	$I_{CLAMP} = 2.5\text{ A}, T_A = 25^\circ\text{C}$		1.3	1.7	V
		$I_{CLAMP} = 2.5\text{ A}, T_A = -40^\circ\text{C to } 125^\circ\text{C}$			2.5	
$V_{CLAMP-THR}$	Clamp Activation Threshold		1.5	2	2.5	V

**IGBT SHORT CIRCUIT CLAMPING**

$V_{CLAMP-OUT}$	Clamping Voltage ( $V_{OUT} - V_{DD2}$ )	IN+ = Low, IN- = High, $I_{OUT} = 500\text{ mA}$ (pulse test, $t_{CLPmax} = 10\ \mu\text{s}$ )		0.9	1	V
$V_{CLAMP-CLAMP}$	Clamping Voltage, Clamp ( $V_{CLAMP} - V_{DD2}$ )	IN+ = High, IN- = Low, $I_{CLAMP-CLAMP} = 500\text{ mA}$ (pulse test, $t_{CLPmax} = 10\ \mu\text{s}$ )		1.4	1.5	V

**DESAT PROTECTION**

$V_{DESAT-THR}$	DESAT Threshold Voltage		8.5	9	9.5	V
$I_{DESAT-CHG}$	Blanking Charge Current	$V_{DESAT} = 7\text{ V}$	0.45	0.5	0.55	mA
$I_{DESAT-DIS}$	Blanking Discharge Current			50		mA

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**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 15\text{ V}$ ,  $V_{EE2} = -8\text{ V}$ ) (continued)

For typical values  $T_A = 25^\circ\text{C}$ , for min/max values,  $T_A$  is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTIC</b>						
$t_{PD-ON}$	IN+, IN- to Output High Propagation Delay	$C_{LOAD} = 10\text{ nF}$ $V_{IH}$ to 10% of output change for $PW > 150\text{ ns}$ . OUT and CLAMP pins are connected together	40	60	90	ns
$t_{PD-OFF}$	IN+, IN- to Output Low Propagation Delay	$C_{LOAD} = 10\text{ nF}$ $V_{IL}$ to 90% of output change for $PW > 150\text{ ns}$ . OUT and CLAMP pins are connected together	40	66	90	ns
$t_{DISTORT}$	Propagation Delay Distortion (= $t_{PD-ON} - t_{PD-OFF}$ )	$T_A = 25^\circ\text{C}$ , $PW > 150\text{ ns}$	-15	-6	15	ns
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $PW > 150\text{ ns}$	-25		25	
$t_{DISTORT\_TOT}$	Prop Delay Distortion between Parts	$PW > 150\text{ ns}$	-30	0	30	ns
$t_{RISE}$	Rise Time (see Figure 3)	$C_{LOAD} = 1\text{ nF}$ , 10% to 90% of Output Change		14		ns
$t_{FALL}$	Fall Time (see Figure 3)	$C_{LOAD} = 1\text{ nF}$ , 90% to 10% of Output Change		19		ns
$t_{LEB}$	DESAT Leading Edge Blanking Time (See Figure 5)			450		ns
$t_{FILTER}$	DESAT Threshold Filtering Time (see Figure 5)			370		ns
$t_{STO}$	Soft Turn Off Time (see Figure 5)	$C_{LOAD} = 10\text{ nF}$ , $R_G = 10\ \Omega$ . $V_{EE2} = 0\text{ V}$		550		ns
		$C_{LOAD} = 10\text{ nF}$ , $R_G = 10\ \Omega$		750		
$t_{FLT}$	Delay after $t_{FILTER}$ to $\overline{FLT}$			450	1000	ns
$t_{MUTE}$	Input Mute Time after $t_{FILTER}$			5		$\mu\text{s}$
$t_{RST}$	RST Rise to $\overline{FLT}$ Rise Delay			23	100	ns
$t_{RDY1O}$	RDY High to Output High Delays (see Figure 4)			55	100	ns
$t_{RDY2O}$						
$t_{RDY1F}$	$V_{UVLO2-OUT-OFF}$ to RDY Low Delays (see Figure 4)		6	8	15	$\mu\text{s}$
$t_{RDY2F}$						

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Values based on design and/or characterization.



# NCV57001F

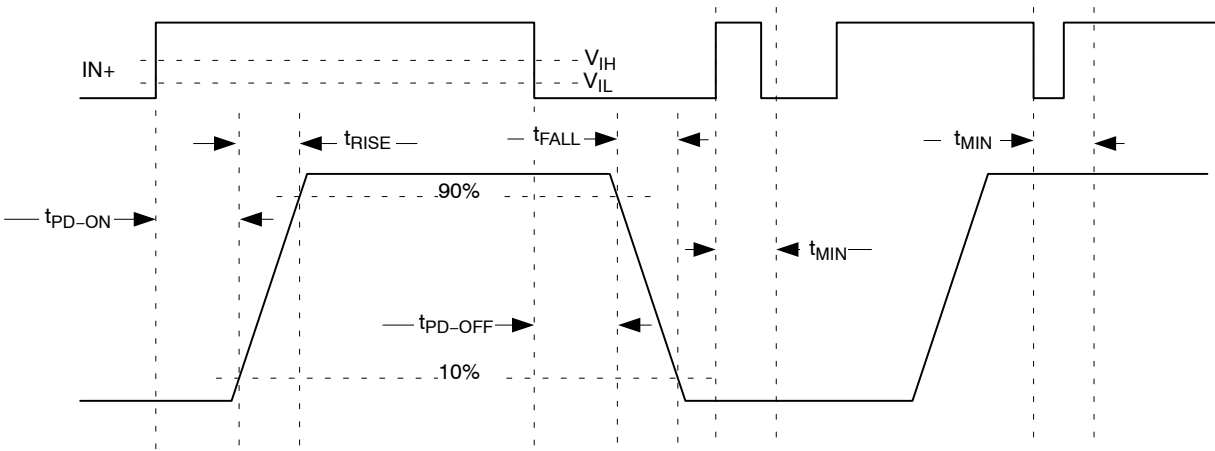


Figure 3. Simplified Block Diagram

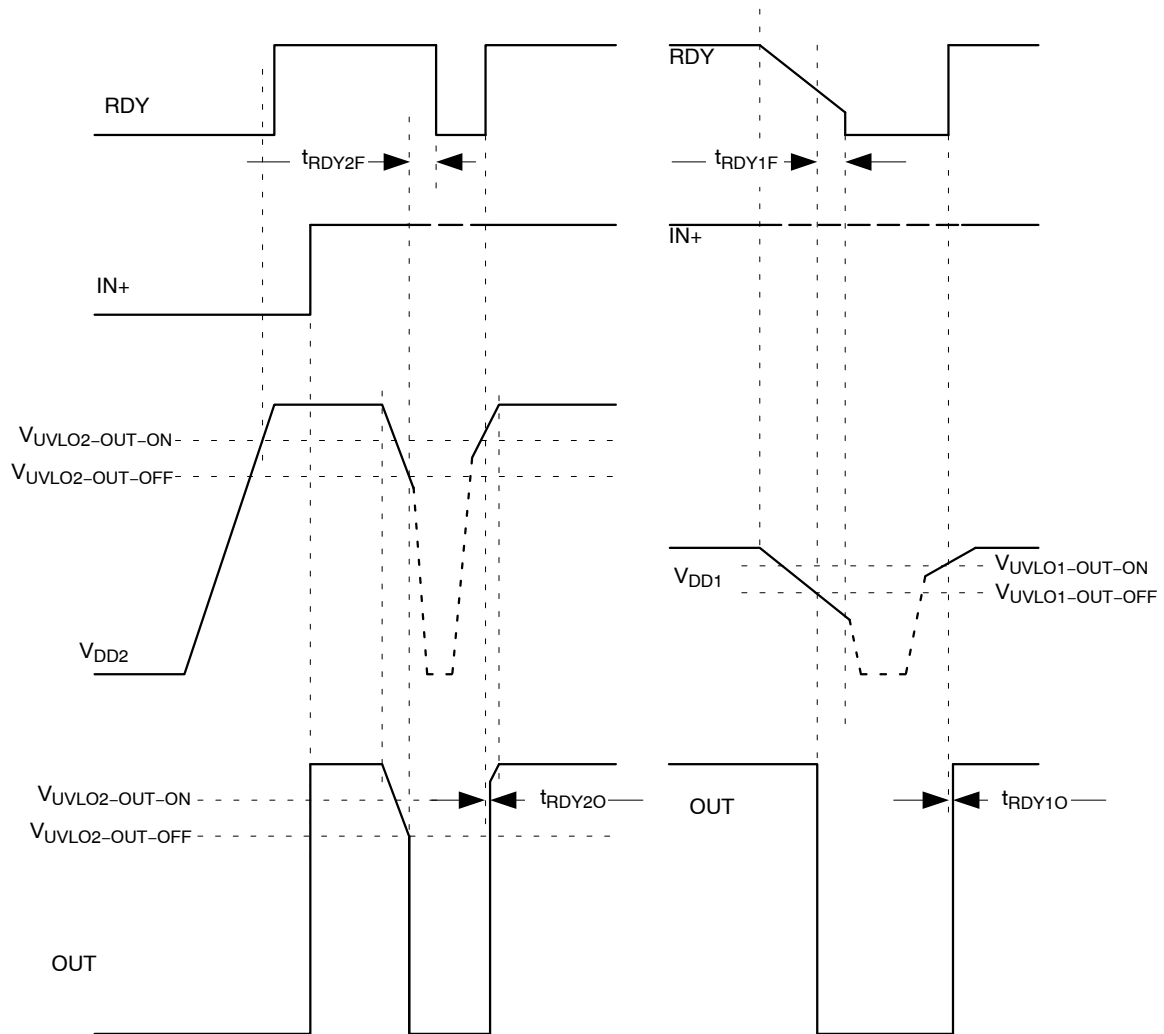


Figure 4. Simplified Block Diagram

NCV57001F

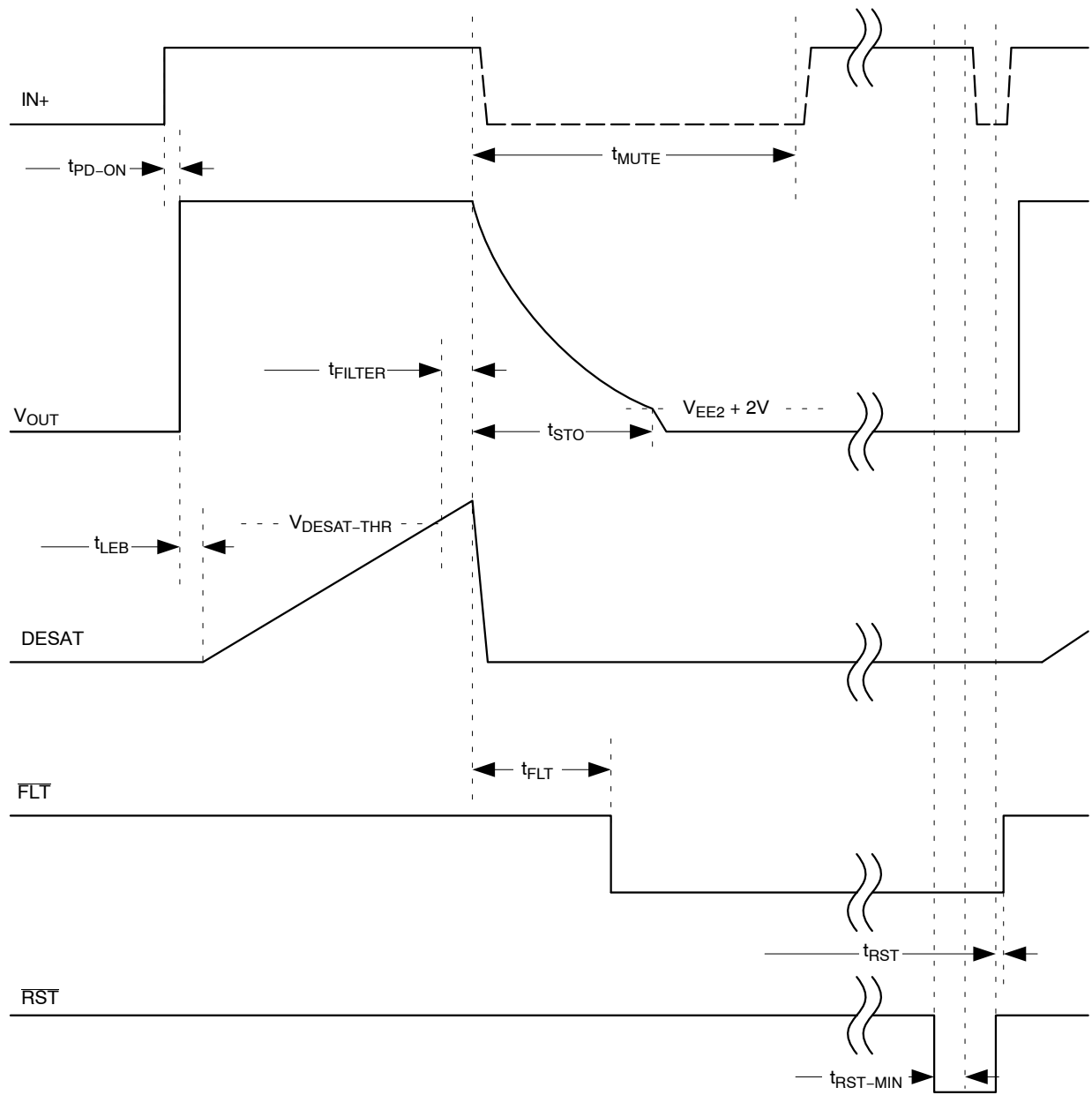


Figure 5. UVLO Waveform

FEATURE DESCRIPTIONS

**Under Voltage Lockout (UVLO)**

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned-off, if the supply  $V_{CC1}$  drops below  $V_{UVLO1-OUT-OFF}$  and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on  $V_{IN}$  until the  $V_{CC1}$  rises above the  $V_{UVLO1-OUT-ON}$  again. If the supply  $V_{CC1}$  increase over  $V_{UVLO1-OUT-ON}$ , the RDY pin output goes to be open-drain and outputs continue to switch IGBT

- The IGBT is turned-off, if the supply  $V_{CC2}$  drops below  $V_{UVLO2-OUT-OFF}$  and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on  $V_{IN}$  until the  $V_{CC1}$  rises above the  $V_{UVLO1-OUT-ON}$  again. If the supply  $V_{DD1}$  increases over  $V_{UVLO1-OUT-ON}$ , the RDY pin output goes to be open-drain and outputs continue to switch IGBT
- VEE2 is not monitored.

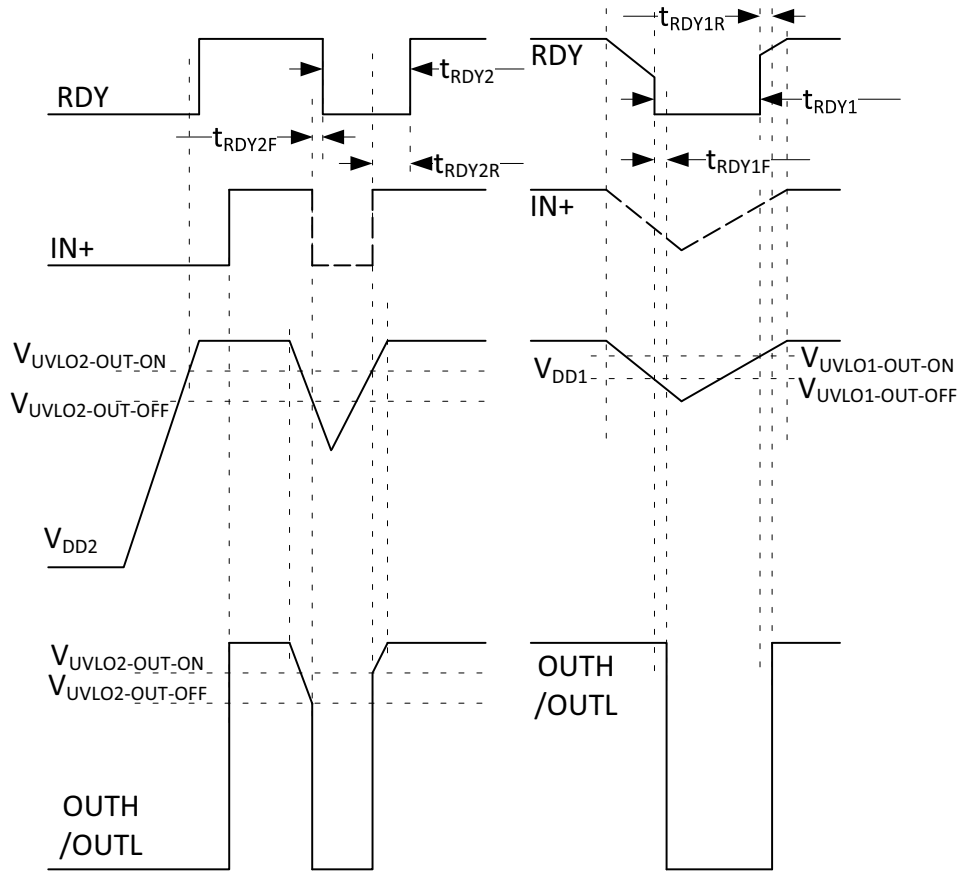


Figure 6. UVLO Diagram

**Active Miller Clamp Protection (CLAMP)**

NCV57001F supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage through OUTL with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output to the IGBT gate is also not an issue. Typical values for bipolar operation are  $V_{DD2} = 15\text{ V}$  and  $V_{EE2} = -5\text{ V}$  with respect to  $GND_2$ .

For operation with unipolar supply, typically,  $V_{DD2} = 15\text{ V}$  with respect to  $GND_2$ , and  $V_{EE2} = GND_2$ . In this case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected directly to IGBT gate and Miller current is sunk through a low impedance CLAMP transistor. When the IGBT is turned-off and the gate voltage transitions below  $V_{CLAMP}$ , the CLAMP current output is activated.

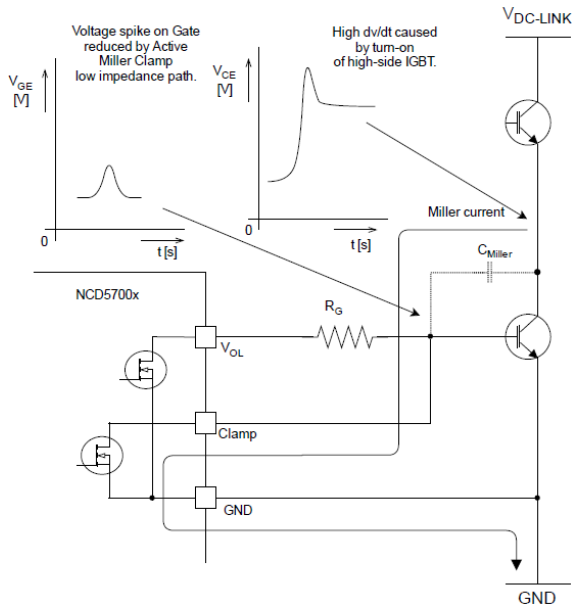


Figure 7. Current Path without Miler Clamp Protection

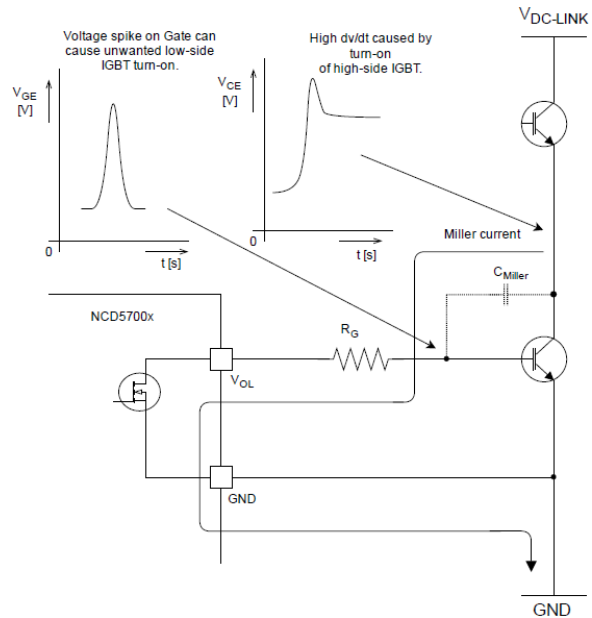


Figure 8. Current Path with Miler Clamp Protection

**Non-inverting and Inverting Input Pin (IN+, IN-)**

NCV57001F has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non-inverting input IN+ controls the driver output while inverting input IN- is set to LOW
- Inverting input IN- controls the driver output while non-inverting input IN+ is set to HIGH

**Warning:** When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

**Desaturation Protection (DESAT)**

Desaturation protection ensures the protection of IGBT at short circuit. When the  $V_{CESAT}$  voltage goes up and reaches the set limit, the output is driven low and /FLT output is activated. Blanking time can be set by internal current source and an external capacitor. To avoid false DESAT triggering and minimize blanking time, fast switching diodes with low internal capacitance are recommended. All DESAT protective diodes internal capacitances builds voltage divider with the blanking capacitor.

**Warning:** Both external protective diodes are recommended for the protection against voltage spikes caused by IGBT transients passing through parasitic capacitances.

**DESAT Circuit Parameters Specification**

$$t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$$

$$V_{DESAT-THR} > R_{S-DESAT} \cdot I_{DESAT-CHG} + V_{FHV\ diode} + V_{CESAT\_IGBT}$$

# NCV57001F

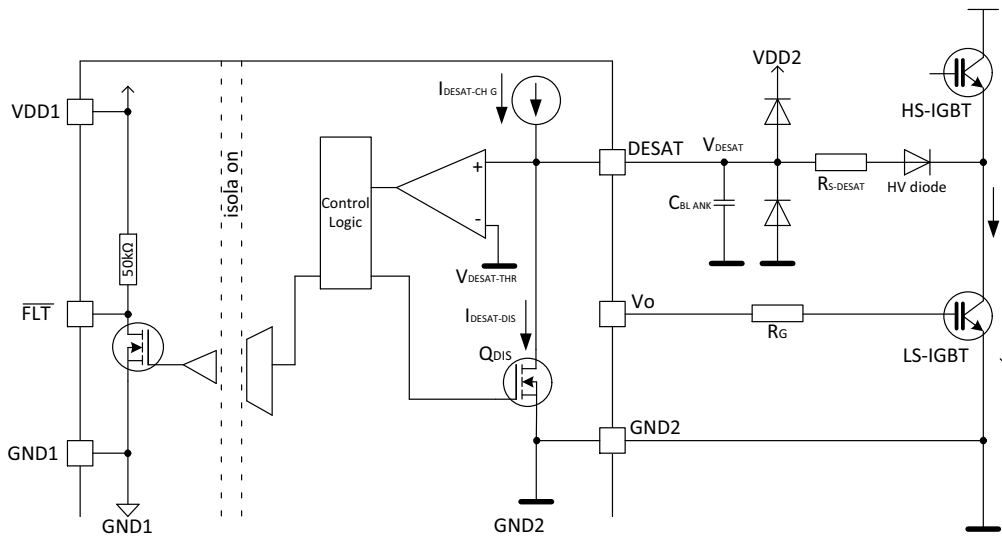


Figure 9. DESAT Protection Schematic

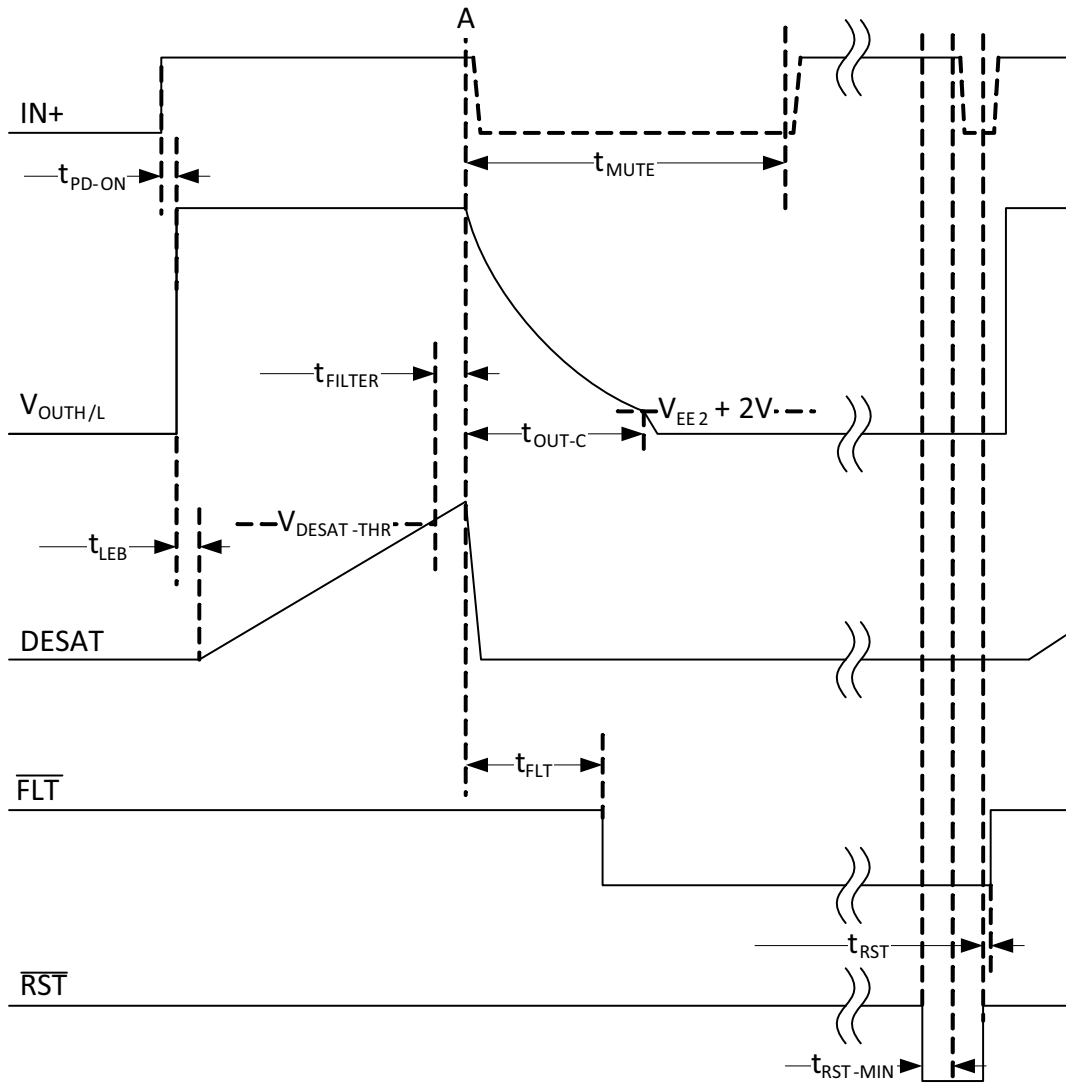


Figure 10. DESAT Switch Off Behavior



# NCV57001F

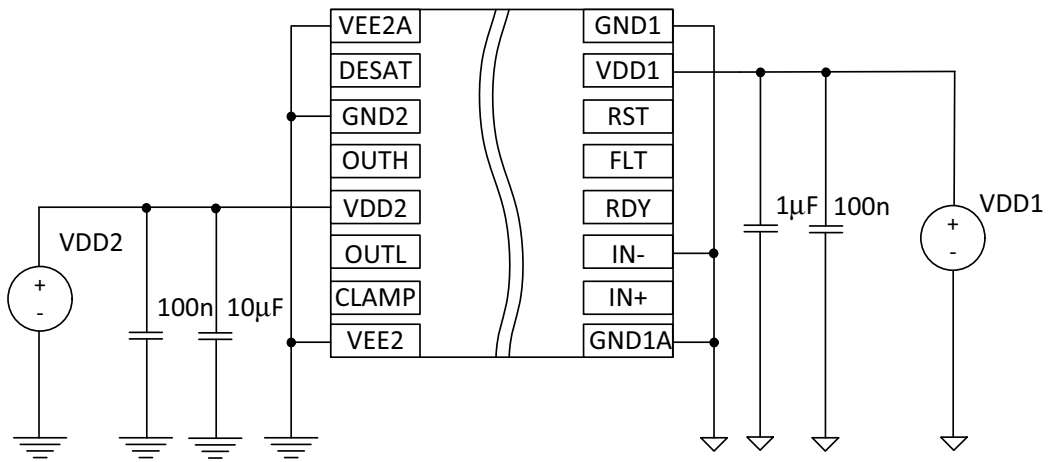


Figure 12. Unipolar Power Supply

## Common Mode Transient Immunity (CMTI)

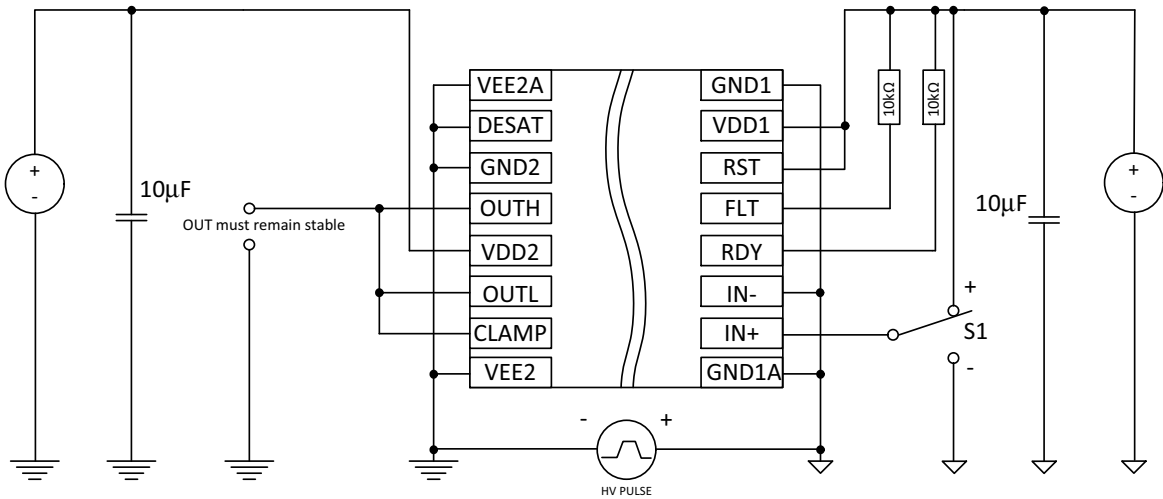


Figure 13. Common-Mode Transient Immunity Test Circuit

# NCV57001F

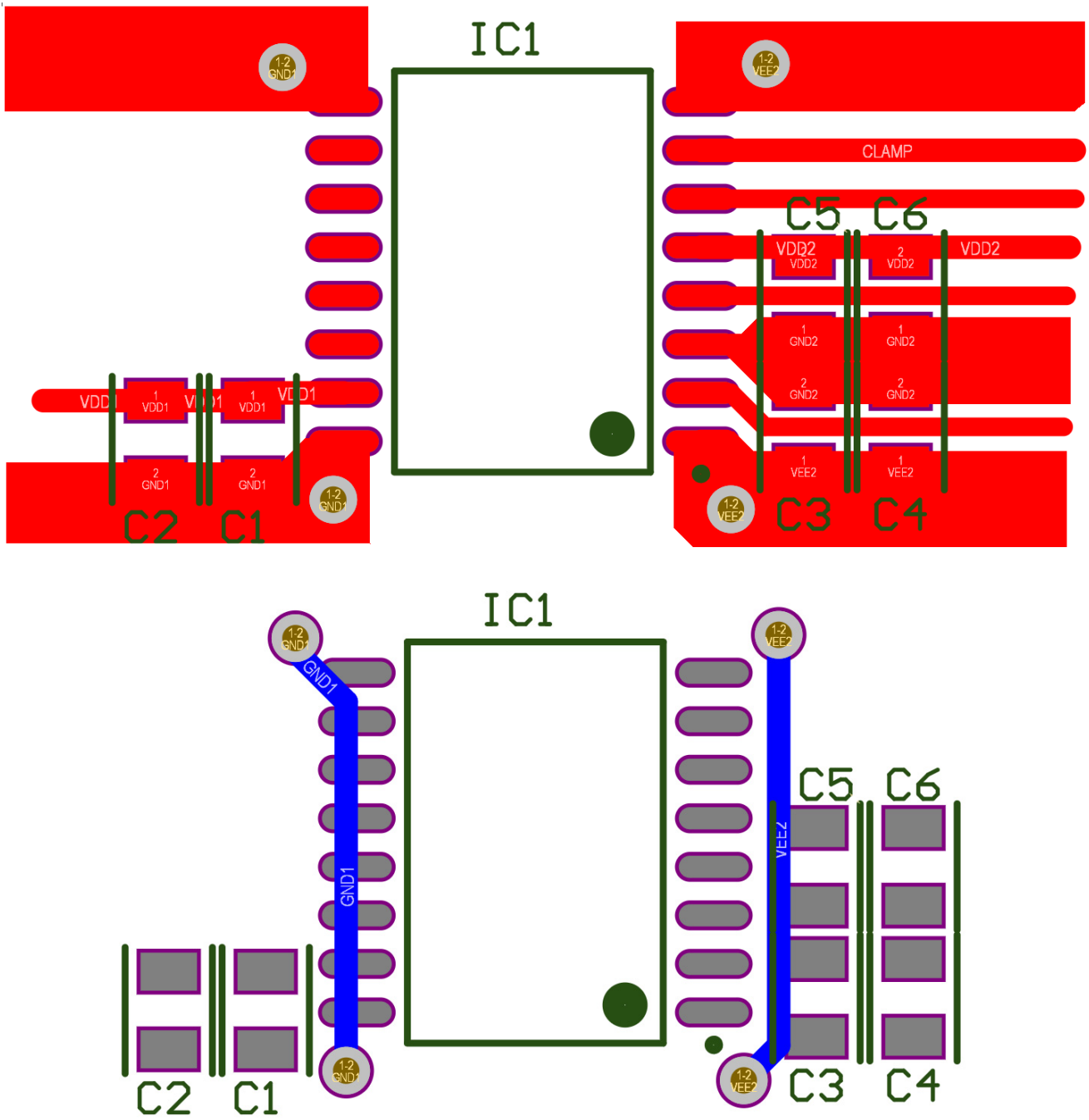
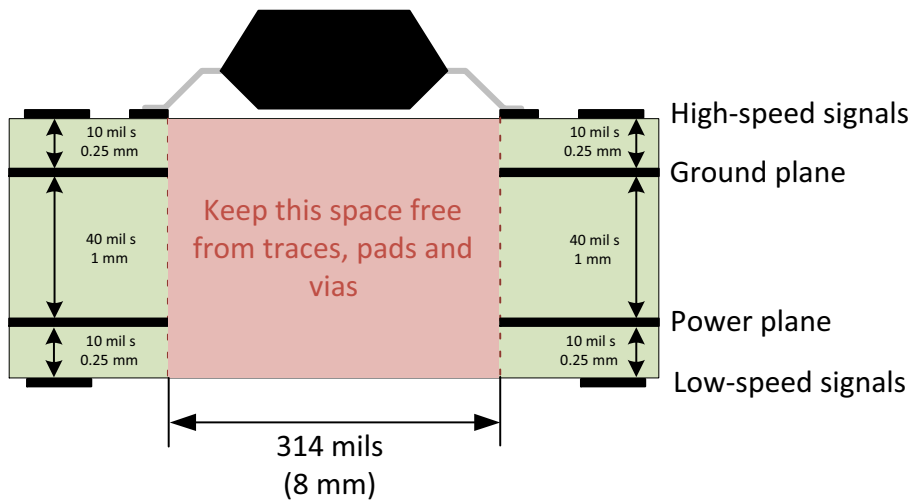


Figure 14. Recommended Basic Bipolar Power Supply PCB Design



# NCV57001F



**Figure 15. Recommended Layer Stack**

## ORDERING INFORMATION

Device	Package	Shipping†
NCV57001FDWR2G*	SOIC-16 Wide Body (Pb-Free)	1,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

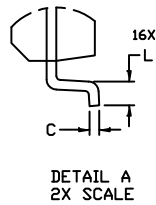
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1  
SCALE 1:1

SOIC-16 WB  
CASE 751G  
ISSUE E

DATE 08 OCT 2021

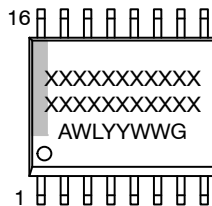


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF *B* DIMENSION AT MAXIMUM MATERIAL CONDITION.
- DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD PROTRUSIONS.
- MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

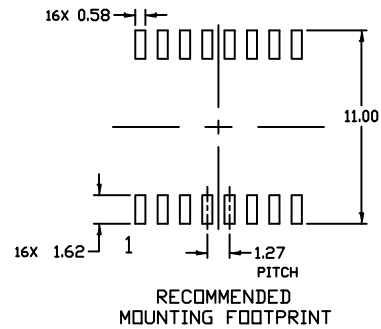
DIM	MILLIMETERS	
	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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